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Investigation on Multi-Phase Zsource Inverter

Thesis submitted in fulfilment of the requirements for the degree of
'Doctorate Es-Sciences' in Electrical Engineering option Automatic

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UNIVERSITY ZIANE ACHOUR OF DJELFA

DOCTORAL THESIS

Investigation on Multi-Phase Zsource Inverter

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Abstract

Faculty of Sciences and Technology
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DOCTOR IN SCIENCE

Investigation on Multi-Phase Zsource Inverter

by Mr Naas CHARRAK

The multiphase inverters and machines have many advantages compared to their counterpart three-phase machines, which are actually used extensively in many industries such as ship propulsion, "more electric aircraft", electric/hybrid vehicles, etc.... On the other side, the qZ-source inverter has also many advantages compared to the conventional inverters, mainly high boosting capability, more freedom degrees of switching states and less voltage and current stresses of switch devices can be obtained. Such advantages among others make it to be a good candidate in many industrial applications. Thus, the present thesis proposes the topology of two level five-phase qZ-source inverter, where the main aim is to be used for driving the five-phase machine and consequently benefiting from the merits of the advantages of both topologies of the machine and the inverter in building one combined topology. The simulations results obtained using MATLAB/SIMULINK prove the quality of the improved performances of the proposed topology in comparison with previous works which can be a promising solution in many industrial applications based on the aforementioned advantages.

Keywords:

Three phase inverter, Three phase machine, Multiphase inverter, Multiphase machine, Zsource inverter, Quasi Zsource inverter, PWM, Modulation index, Voltage gain, Boost factor.

الملخص

تتمتع المموجات و الآلات متعددة الأطوار بالعديد من المزايا مقارنةً بالآلات ثلاثية الطور المماثلة ، والتي تستخدم فعليًا على نطاق واسع في العديد من الصناعات مثل دفع السفن ، "المزيد من الطائرات الكهربائية" ، المركبات الكهربائية / الهجينة ، إلخ ....
من جهة أخرى ، يتمتع المموج qZ source أيضًا بالعديد من المزايا مقارنة بالمموجات التقليدية ، ويمكن الحصول على قدرات تضخيم عالية بشكل أساسي ودرجات حرية أكبر لحالات التبديل وقليل من توتر و تيار الاجهاد لأجهزة التبديل. هذه المزايا من بين مزايا أخرى تجعلها مرشحًا جيدًا في العديد من التطبيقات الصناعية. وبالتالي ، فإن الأطروحة الحالية تقترح طوبولوجيا المموج qZ source خماسي الطور ذي المستوى الثاني ، حيث يكون الهدف الرئيسي هو استخدامهما لتغذية الآلة ذات الخمس أطوار ، وبالتالي الاستفادة من مزايا كل من طبولوجيا الآلة و المموج في بناء طوبولوجيا واحدة مدمجة. تثبت نتائج المحاكاة التي تم الحصول عليها باستخدام MATLAB / SIMULINK جودة الأداء المحسن للطوبولوجيا المقترحة مقارنة بالأعمال السابقة التي يمكن أن تكون حلاً واعدًا في العديد من التطبيقات الصناعية بناءً على المزايا المذكورة أعلاه.

الكلمات المفاتيح:

عاكس ثلاثي الطور ، آلة ثلاثية الطور ، عاكس متعدد الأطوار ، آلة متعددة الأطوار ، عاكس Zsource ، عاكس شبه Zsource، PWM ، مؤشر التضمين ، كسب الجهد ، عامل التعزيز.

Résumé

Les onduleurs et les machines polyphasées présentent de nombreux avantages par rapport à leurs homologues triphasées, qui sont actuellement largement utilisées dans de nombreuses industries telles que la propulsion des navires, les " avions plus électriques", les véhicules électriques/hybrides, etc... D'autre part, l'onduleur qZ-source présente également de nombreux avantages par rapport aux onduleurs conventionnels, notamment une capacité d'amplification élevée, plus de degrés de liberté dans les états de commutation et moins de contraintes de tension et de courant pour les dispositifs de commutation. Ces avantages, parmi d'autres, en font un bon candidat pour de nombreuses applications industrielles. Ainsi, la présente thèse propose la topologie d'un onduleur qZ-source à deux niveaux et cinq phases, dont l'objectif principal est d'être utilisé pour entraîner la machine à cinq phases et par conséquent de bénéficier des avantages des deux topologies de la machine et de l'onduleur en construisant une topologie combinée. Les résultats des simulations obtenus à l'aide de MATLAB/SIMULINK prouvent la qualité des performances améliorées de la topologie proposée par rapport aux travaux précédents, ce qui peut être une solution prometteuse dans de nombreuses applications industrielles basées sur les avantages susmentionnés.

Mots clés :

Onduleur triphasé, machine triphasée, onduleur multiphasé, machine multiphasée, onduleur Zsource, onduleur Quasi Zsource, PWM, indice de modulation, gain de tension, facteur de boost.

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My great thanks go to all my colleagues in Applied Automation and Industrial Diagnostics Laboratory especially to **Prof. Dr. Ahmed Hfaifa, Dr. Ahmed Zohair Djeddi and Mr. Belgacem Said Khldi**.

Naas Charrak
September 2021

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List of Abbreviations

BJT	Bipolar Junction Transistor
CMV	Common Mode Voltage
CqZSI	Cascaded quasi Z-source Inverters
CSC	Current Source Converters
CSI	Current Source Inverter
DF	Displacement Factor
DTC	Direct Torque Control
EMI	Electromagnetic Interference
EZSI	Embedded Z-source Inverter
FOC	Field Oriented Control
GTO	Gate Turn Off Thyristor
IGBT	Insulated Gated Bijunction Transistor
IGCT	Integrated Gate-Commutated Thyristor
IPM	Intelligent Power Modules
MBC	Maximum Boost Control
MCBC	Maximum Constant Boost Control
MOSFET	Field-Effect Transistor
MPC	Model Predictive Control
PWM	Pulse width modulation
qZSI	Quasi Z-Source Inverter
SBC	Simple Boost Control
SCR	Silicon Controlled Rectifier
THD	Total Harmonic Distortion
TqZSI	quasi-Z-Source Inverter
TSI	T-Source Inverter
TZSI	Trans- Z-Source Inverter
UPS	Uninterruptible Power Supplies
VFI	Voltage-Fed Inverter
VSC	Voltage Source Converters
VSI	Voltage Source Inverter
ZSI	Z Source Inverter

List of Symbols

V_c	Peak value of the triangular carrier signal.
V_r	Peak value of the reference or modulating signal.
td	Dead time.
V_0	Output voltage.
I_0	Output current.
PO	Instantaneous power flow.
V_{ao}	Output voltage in square-wave mode.
V_{a01}	Fundamental component of Vao.
V_{a0}	Peak value of the fundamental.
V_{a0rms}	rms value of Vao
V_m	Amplitude of the control signal.
m	Amplitude modulation ratio" or "modulation index".
m_f	Frequency modulation ratio
f_c	Frequency of the triangular carrier
T_c, T	Switching period.
T_0	Interval of the shoot through state.
T_1	Interval of the non-shoot through state.
D	Duty cycle ratio
V_{in}	Input dc voltage.
VPN	Peak dc voltage across the inverter bridge.
B	Boost factor.
$\hat{V}_{ac}$	Output peak phase voltage
M	Modulation index.
G	Gain voltage.
V_{stress}	Stress voltage.

To all my Family for their Courage...

General introduction

The first preliminary investigation on an inverter powered a five-phase induction motor has been introduced in 1969 by Ward and Harer [1] and mentioned that the amplitude of the torque ripples can be reduced and its frequency can be increased by extending the number of stator phases.

Although three-phase machines are the common trend in all electric drive applications, mainly due to the existence of three-phase voltage sources everywhere. The interest of the research community and industrial practitioners has recently focused on multiphase machines that have more than three phases, because of their inherent advantages in terms of capability and continuity of operation even after partial failure. This is the case for safety applications, where the ability to tolerate Multi-phase training breakdowns have attracted much more interest from the scientific community.[2]

With the invention of cheap and fast switching power electronics devices (Thyristors, Mosfets, IGBT's...), not only the control of induction machine became easier and more flexible, but also the number of machine phases has become an important factor in the design, since in a multi-phase drive the energy supplied through each phase of the inverter is less than in a three-phase system, this has advantages for the concept of inverters for high-power machines [1]. It can be seen that multiphase (more than three-phase) machines have several advantages over three-phase machines, such as

- Additional degrees of freedom existing in multiphase machines.
- lower torque pulsation[3-1],
- Increased efficiency results from a potential reduction in stator copper loss, and some reduction in rotor copper loss is expected, although on a much smaller scale. [3]
- If third harmonic currents are injected to reshape the flux distribution in the machine, extra torque production can be gained in these systems (multiphase systems) and thus obtain higher fundamental flux densities without extrapolating the flux limits and forcing the machine into saturation[4,5].

Improved reliability as the machine keeps running with one of its many phases open or shorted and there is not much performance degradation. This feature of the multiphase machine will be advantageous in nuclear power plants for its circulation pumps, and can be used much more in high power applications, such as rail traction, marine propulsion, automotive and aerospace and other applications.

- Lower current per phase with no increase in per phase voltage. This beneficial feature can be useful for electric vehicles and similar applications where lower, upper voltage and current limits are desirable
- The most advantageous property is the increase in power rating of the machine on high phase-order connection within the same framework. In other words, there is a reduction of the power requirements per phase but with an improved modularity and fault tolerance. [6],
- higher torque density.
- fault tolerance .
- The stabilizing effect of the harmonic injection gives rise to a feature of particular interest because the niche where multiphase drive applications are being developed requires enhanced reliability and robustness. [7] and
- Lower current ripple [8].

Thus, multiphase control machines are normally considered for specialized application areas such as ship propulsion, "more electric aircraft", electric/hybrid vehicles, etc..[2]

In order to ensure the power supply and the control of multiphase machines, a multiphase inverter is required. Researchers are therefore faced with a challenge in the field of multiphase two-level inverters, where several control techniques have been proposed to overcome the main problems associated with three-phase two-level inverters, such as switching losses and voltage and current limitations at power electronics switches. A.Iqbal et al [9] have proposed a generalized concept of nth harmonic injection for n-phase inverters, using adequate methods for VSI pulse width modulation (PWM) control. Also Zicheng Liu, et al[10] have introduced many drive techniques for multiphase machines such as drive algorithms, including Field-Oriented Control (FOC), Direct Torque Control (DTC) and Model Predictive Control (MPC). Federico B. and Mario J. D. [11] have presented recent advances in the design, modeling, and control of multiphase machines, including healthy operation, and discusses open challenges and future research on multiphase motor drives.

Thesis organization

This thesis is composed of four chapters:

In the first chapter, We start with a historical review of inverters, and brief presentation of the state of the art of some structures of Half-bridge , Full- bridge , three-phase inverters and their operating modes. Then the multiphase inverters modes are discussed.
In the second chapter, a brief review is given to different topologies of Zsource Inverters, while mentioning some advantages and disadvantages of each topology.
The third chapter deals with the use and some details of different PWM carrier based control techniques, starting by the simple boost control-based, the maximum boost control, the maximum constant boost control, and finally the application of the third harmonic injection with the last one.

The fourth chapter is devoted to the analysis of multi-phase qZ-source inverter with maximum constant boost control technique. Simulations have been carried out to validate the main advantages and performances of the multiphase qZSI inverter which is implemented in SIMULINK / MATLAB as a five phase inverter using the Power System block set. In addition, the thesis ends with a conclusion that summarizes the essence of our contribution and proposes some perspectives for future research.

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Chapter 1

Review of two level inveters

1.1 Introduction

The term rectifier was widely used for more than two decades before 1925. It was meant that any apparatus or rotary switch transforming alternating current to direct current. Rotary converters, known later as synchronous converters, were used by 1892 to convert alternating current to direct current (AC to DC). Rotary converters were manufactured until the 1950s, when germanium diodes were discovered. At that time people were confused to make distinction between rectifier and its inverse conversion. H. Rissiki addresses the issue of terminology in the preface of his book titled ('Mercury-Arc Current convertors'), published in 1935. It provides many German-English equivalents among them the famous term "Inverter". In 1936, Prince's Inverter appeared in literature from all over the world, including Europe and Japan. In 1925 David Prince did publish an article in the GE Review titled "The Inverter" [1]. His article contains nearly all important elements required by modern inverters and is the earliest such publication to use that term in the open literature. Prince defined the inverter as the inverse of the rectifier, and he was not the originator of this idea, but developed it. Today DC-AC converters are referred to as inverters and, depending on the type of power source and the related power circuit topology, they are classified as voltage source inverters (VSI), and current source inverters (CSI). Voltage source inverters are the most common power electronics converters. The DC input voltage of a voltage source inverter can be obtained from a rectifier, usually from the uncontrolled, diode-type or other DC source, such as a battery, fuel cell or solar cell photovoltaic panel. The introduction of the thyristor (GE engineers called it the "Silicon Controlled Rectifier" or SCR) in 1957 was the key stone to the development of the SCR, that really opened up the field to mass applications of power electronics and, in particular, the use of the commutated inverters. First applications (1960) include spinning of textile fibers, mainly associated with the production of nylon.

Inverters can be classified into two types, voltage source and current source inverters. A voltage-fed inverter (VFI) or more generally a voltage source inverter

(VSI) is the one in which the DC source has a low or negligible impedance. The voltage at the input terminals is constant. A current source inverter (CSI) is powered by adjustable current from the DC source of high impedance. A voltage source inverter using thyristors as switches, some type of forced switching is required, whereas VSIs consist of the use of GTOs, BJTs, IGBTs, power MOSFETs, and IGCTs, self-switching with base or gate control signals for their controlled switching turn-on and turn-off. A half-bridge or full-bridge configuration units can be joined together to have three-phase or multiphase topologies.

The inverter output can be single phase or multiphase, and can have square wave, sine wave, PWM wave, stepped wave, or quasi-square wave at the output. Voltage-fed converters are used extensively, and some of their applications may be as follows [2]:

- AC motor drives
- AC uninterruptible power supplies (UPS)
- Induction heating
- AC power supply from battery, photovoltaic array, or fuel cell
- Static VAR generator (SVG) or compensator (SVC)
- Active harmonic filters.

Voltage source inverters (VSI) are characterized on the basis of their design , output voltage and their level of implementation. There are three main types of VSI on the basis of their output voltage as follows:

1.2 Half-Bridge Inverters

One of the most straightforward inverter configurations is the single-phase, half-bridge inverter illustrated in figure 1.1 (a). The circuit consists of a pair of switches S1 and S2 connected in series, parallel to the DC power supply. D1 and D2 called feedback diodes which are always connected across the devices to have free reverse currents flow. And the load is connected between the node A connecting the two switches and the center point O of a split capacitor power supply. The switches S1 and S2 are alternately closed for 180° to generate the square wave output voltage as shown in figure 1.1 (b).

To produce a sinusoidal AC output whose amplitude and frequency can both be controlled, different types of PWM control schemes have been investigated [3]. Among these control schemes, sinusoidal PWM is the most commonly used for a

voltage source inverter where a sinusoidal reference voltage waveform is compared to a triangular carrier voltage waveform to generate gate signals for the Inverter's switches.

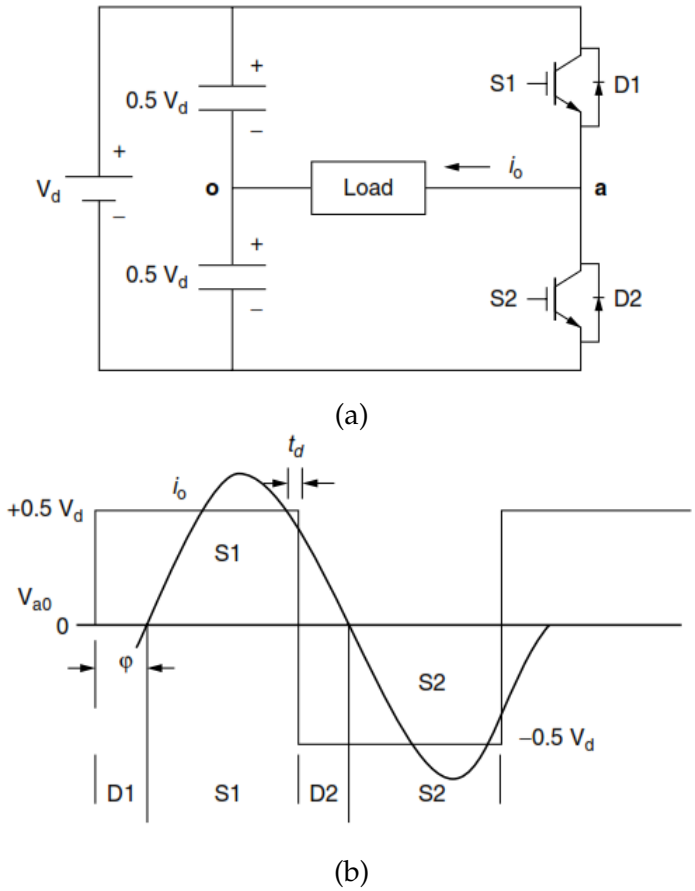

FIGURE 1.1: Single-phase half-bridge inverte (a) Half-bridge inverter (b) Output voltage and current waves in square-wave mode .

In this schematic, the inverter is supplied with a fixed input voltage and controlled ac voltage is obtained by setting the on and off cycles of the inverter switches. The advantages of the PWM control schemes are [4], [5]:

a) Control of the output voltage can be achieved without the addition of external components.

b) PWM minimizes lower order harmonics, while the higher order harmonics can be removed with the use of a filter.

To realize SPWM, a high frequency triangular carrier signal vc is compared to a sinusoidal reference vr of the desired frequency. The intersection of vc and vr determines the switching instants and the switching of the modulated pulse. The PWM scheme is shown in Figure 1.2, where Vc is the peak value of the triangular

carrier signal and Vr is the peak value of the reference or modulating signal. This figure shows the triangle and the modulation signals with arbitrary frequency and amplitude. These signals are compared and mixed via a comparator, resulting in a gating signal according to the following, when the sinusoidal signal has a magnitude greater than the triangular signal, the comparator output is high, otherwise it is low[4].

$$V_r > V_c \qquad S_{11}\ is\ on,\ V_{out} = \frac{V_d}{2} \tag{1.1}$$

and

$$V_r < V_c \qquad S_{12}\ is\ on,\ V_{out} = -\frac{V_d}{2} \tag{1.2}$$

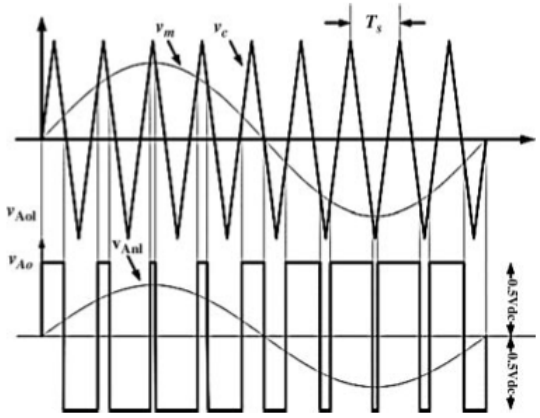

FIGURE 1.2: SPWM illustration, sine-triangle comparison with switching pulse comparison.

During operation, two switches of a leg cannot be gated simultaneously, since they would short the DC supply and consequently causes damage to it. This is the so called shoot-through condition and must be avoided. To overcome this problem a time lag between the switching 'ON' and switching 'OFF' of the two power semiconductor switches of the same leg of an inverter must be introduced, this time is called dead time t_d.

For any inverter, its output voltage must be filtered so that can be assumed sinusoidal. And if the load is inductive such as the AC motor, the load current I_0 will lag V_0, as shown in Figure 1.3. The output waveform of figure 1.3 shows that during intervals 1 and 3 v_o and i_o are both positive, and both negative respectively. Therefore, during intervals 1 and 3, the instantaneous power flow P_O is from the DC side to the AC side, corresponding to an operating mode of the inverter. Whereas, V_0 and I_0 are of opposite signs during intervals 2 and 4, so P_O flows from the AC side to the DC side of the inverter, corresponding to the operating mode of the rectifier, which means the diode is forward biased and the power is fed back to the source, .

However, average power will flow from the source to the load.

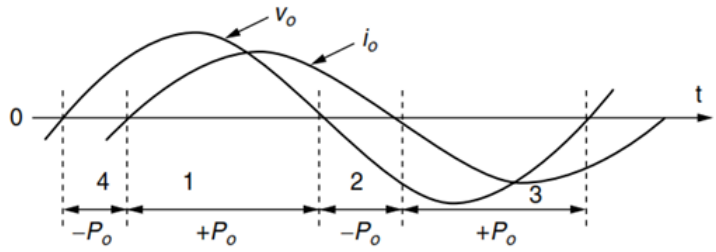

FIGURE 1.3: The filtred output waveform on an inverter.

The output fundamental frequency of the inverter can be adjusted by varying the switching period and the voltage can be regulated by changing the value of the DC link voltage.

The output voltage is a square wave, as shown in Figure 1.1(b), and the Fourier analysis gives :

$$V_{ao}(t) = \sum_{n=1}^{\infty} \frac{4}{n\pi} (0.5V_{dc}) \sin(nwt) \tag{1.3}$$

Where :
$w = 2\pi/T$ and $T = 1/f$ T is the output period and f is the output fundamental Frequency.

$V_{a01} = (4/\pi)(0.5V_{dc})\, sin(wt)$ is the fundamental component of V_{ao}.

$V_{a0} = (4/\pi)(0.5V_{dc})$ is the peak value of the fundamental.

$V_{a0rms} = (4/\pi)(0.5V_{dc})/sqr(2)$ is the rms value of V_{ao}.

A graphical representation of the harmonics contained in the output phase voltage is shown in Figure 1.4. This figure shows that the output contains a large amount of low order harmonics such as 3rd, 5th,7th, etc. and the magnitude of the harmonics varies as the inverse of its order.

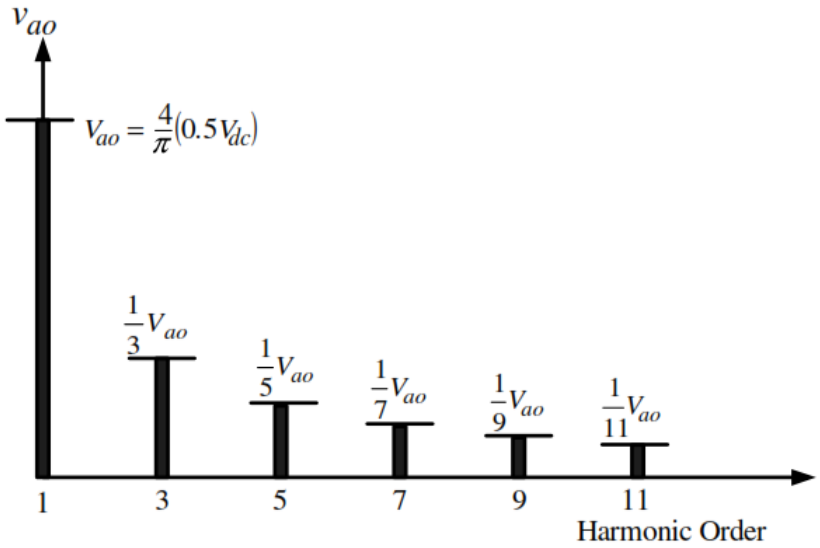

FIGURE 1.4: Atypical harmonic spectrum of output voltage in a half-bridge inverter.

In the literature [6], [7] and [8], it is reported that, the triangular carrier support is the most commonly used, because it offers a good harmonic performance. The ratio between the amplitude of the control signal and the carrier signal is called the "amplitude modulation ratio" or "modulation index".

$m = V_m / V_c$

A second parameter defined by the SPWM is called the 'frequency modulation ratio' and is given as

$m_f = f_c / f_m$

This is also an important parameter that decides the harmonic performance of the output voltage.

The inverter leg switching frequency is equal to the frequency of the triangular carrier signal and the switching period is $T_c = 1/f_c$.

During an inverter switching period T, the amplitude of the modulation signal can be assumed to be almost constant, because the switching frequency of the triangular carrier signal is high in relation to the modulation signal. The duration of S_1 being On is denoted $\delta 1$ and the On period of S_1' is denoted by $\delta' 1$, using the homothetic transformation of the triangles in the following Figure 1.5.

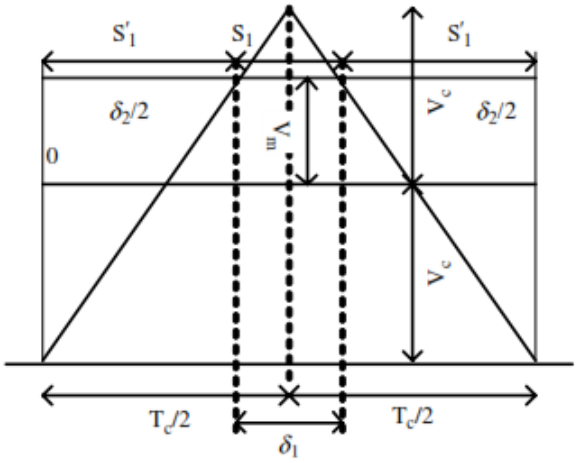

FIGURE 1.5: One switching cycle in SPWM.

The following relation can be written:

$$\frac{\delta_2'/2}{T_c/2} = \frac{V_c + V_m}{V_c + V_c}$$

$$\delta_2' = T_c \left(\frac{V_c + V_m}{2V_c} \right) \tag{1.4}$$

and

$$\delta_1 = T_c - \delta_2' = T_c \left(1 - \left(\frac{V_c + V_m}{2V_c} \right) \right) \tag{1.5}$$

By applying the equal volt-second principle (the product of voltage and time should be equal for the two switches and the average output), to determine the average voltage during one switching period;

$$\delta_1 \frac{V_{dc}}{2} - \delta_2' \frac{V_{dc}}{2} = T_c V_{A0} \tag{1.6}$$

$$V_{A0} = \frac{1}{T} \frac{V_{dc}}{2} \left(\delta_1 - \delta_2' \right) = \frac{V_m}{V_c} \frac{V_{dc}}{2} \tag{1.7}$$

$$V_{A0} = m \frac{V_{dc}}{2} \tag{1.8}$$

One can see that the average leg voltage of the inverter is proportional to the modulation index (m) and the maximum value is $V_d/2$ when the modulation index

is 1.

In the SPWM method, the harmonics in the inverter output voltage waveform appear as side bands centered on the switching frequency and its multiples, i.e. around $f_c, f_{2c}, f_{3c}, etc...$ A general form for the frequency at which harmonics appear is [9].

$$f_h = \left(m\frac{f_c}{f_m} \mp k \right) f_m \tag{1.9}$$

And the harmonic order h is

$$h = \frac{f_h}{f_m} = \left(j\frac{f_c}{f_m} \mp k \right) \tag{1.10}$$

Note that for all odd j, the harmonics will appear for even values of k and vice-versa. Indeed, the following points must be taken into account in designing inverters:

1. The frequency modulation ratio is chosen to be an odd integer, to avoid even harmonics appearing in the output voltage.
2. The switching frequency should be as low as possible to avoid losses due to the switching of the power switches.
3. The switching frequency for the medium power motor drive system is kept between $4kHz$ and $10kHz$.(Because low switching frequency results in poor output voltage quality).
4. For low values of the frequency modulation ratio, usually for $mf > 21$, Vc and Vr signal are synchronized with each other, called synchronous PWM.
5. The frequency modulation ratio is chosen as an integer number to facilitate the proper synchronization, and to avoid the production of sub-harmonics.
6. For higher values of the frequency modulation ratio, $mf > 21$, the synchronization of the carrier wave and modulating signals are not necessary and the result is asynchronous PWM.
7. In high power applications, even small sub-harmonics may lead to appreciable losses. Thus it is recommended to use synchronous PWM for high power applications.

1.3 Full-bridge Inverters :

The single phase full bridge (also called H-bridge) VSI topology is shown in Figure 1.6 . This inverter includes two half-bridge inverter legs which provide the neutral point to the load. In full bridge inverter, when S_1, S_3 conduct the output voltage is Vs and when S_2, S_4 conducts the output voltage is $-V_s$. The switches S_1, S_3 conducts for period of 0 to $T/2$ and the switches S_2, S_4 conducts for period of $T/2$ to T where T is the time period of the gate pulses to the devices. And therefore an alternating current is obtained at the output side while the input side is DC. The frequency of output *ac* voltage can be varied by varying the T of the gate signal, and the voltage magnitude can be changed by changing the DC link voltage.

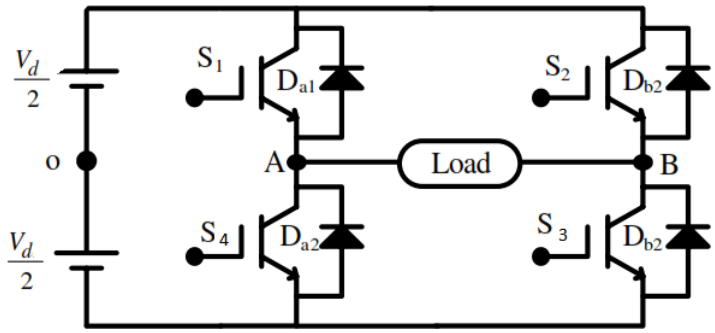

FIGURE 1.6: A single phase full bridge.

To describe the operation of the circuit with zero dead time, and to get the expression of the output voltage, a switching variables a and b can be introduced and assigned to individual legs of the inverter defined as

$$a = \begin{cases} 1 \text{ if } S_1 \textit{ is } \text{ on and } S_4 \textit{ is } \text{ off} \\ 0 \text{ if } S_1 \text{ is off and } S_4 \textit{ is } \text{ on} \end{cases} \quad b = \begin{cases} 1 \text{ if } S_2 \textit{is} \text{ on and } S_3 \textit{ is } \text{ off} \\ 0 \text{ if } S_2 \text{ is off and } S_3 \textit{ is } \text{ on} \end{cases} \tag{1.11}$$

When a given switching variable takes the value of 1, the positive terminal of the DC source is connected to the corresponding output terminal of the inverter. A value of 0 means the connection of the negative terminal of the source to the terminal of the inverter. Therefore, the output voltage, v_0, of the inverter can be expressed as

$$v_0 = V_d\,(a - b) \tag{1.12}$$

In this inverter configuration, there are $22(=4)$ states, and can be arranged from 0 to 3, the output voltage can take only three values ; 0, $+V_{dc}$, and $-V_{dc}$ as shown in

TABLE 1.1: Operation of single phase inverter.

Swiches Closed	**Output Voltage,**v_a	**States**
S_1 **and** S_3	$+V_d$	2
S_2 **and** S_4	$-V_d$	1
S_1 **and** S_2	0	0
S_3 **and** S_4	0	3

the following table :

The output voltage and current waveforms for an R-L load are shown in Figure 1.7.[6]
The currents do not change direction instantaneously due to the inductive load. Polar voltages vary between $0.5V_{dc}$ and $-0.5V_{dc}$, while the load voltages vary between V_{dc} and $-V_{dc}$. It is shown that the switching signals are applied at 180 degrees, but in practice a certain dead band is given between the application of firing pulses for the upper and lower power switch. The output voltage is the same as that of the half-wave bridge inverter, except that the amplitude of the phase voltage is doubled in this case. Therefore, the harmonic spectrum remains the same as that of a half-bridge inverter output, except with a double fundamental voltage.

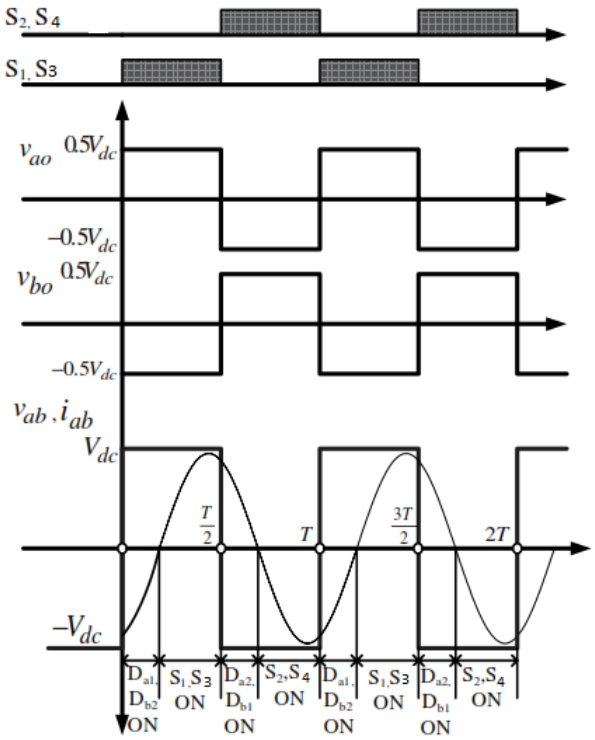

FIGURE 1.7: Switching signal and the output voltage current in a half–bridge inverter.

The purpose of the inverter is to use a DC voltage source to power a load that requires AC voltage and current. It is useful to describe the quality of the AC voltage or current. The quality of the non-sinusoidal wave can be expressed in terms of total harmonic distortion (THD). THD is the ratio of the RMS values of the entire non-fundamental frequency terms to the RMS value of the fundamental frequency term.

Assuming no DC component in the output,

$$THD = \frac{\sqrt{\left(V_{rms}^2 - V_{1,rms}^2\right)}}{V_{1,rms}} \tag{1.13}$$

Where V_{rms} = total rms value of voltage and $V_{1,rms}$ = rms value of fundamental voltage.
The THD of the load current is often more interesting than that of output voltage.

$$DF = \frac{I_{1,rms}}{I_{rms}} = \sqrt{\frac{1}{1 + (THD)^2}} \tag{1.14}$$

The performance of the inverter can be analysed by basic components of voltage

and current waveforms. The performance terms used for inverters are presented as:

- Power efficiency, γ , of the converter , defined as

$$\gamma = \frac{P_0}{P_i} \tag{1.15}$$

  where P_i and P_o denotes the input power and output power of the converter, respectively.

- Conversion efficiency, , γ_c for AC output converters, defined as

$$\gamma_c = \frac{P_{0,1}}{P_i} \tag{1.16}$$

  for AC output converters.
  Symbol $P_{o,1}$ is the AC output power carried by fundamental components of the output voltage and current.

- Input power factor, F_p of the converter, defined as

$$F_P = \frac{P_i}{S_i} \tag{1.17}$$

  where S_i is the apparent input power. The power factor can also be expressed as

$$F_P = k_d k_\varphi \tag{1.18}$$

  Here, k_d denotes the so-called distortion factor, as defined in Equation 1.14. k_φ is the displacement factor, that is, cosine of the phase shift, θ , between the fundamentals of input voltage and current.

The operating quality of the inverter can be further improved by pulse width modulation. These PWM techniques are dealt within the control diagram.[2]

1.4 Three-phase Inverters

A three-phase inverter is defined as a device that converts DC voltage to three-phase AC voltage. This three phase inverter can be obtained by assembling three single

phase inverters (poles or legs same name) to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable.
The circuit diagram topology of a three-phase inverter is shown in figure 1.8, it consists of three basic single phase inverters each one includes two power switches, these switches can be transistors or IGBT's with anti-parallel diodes.

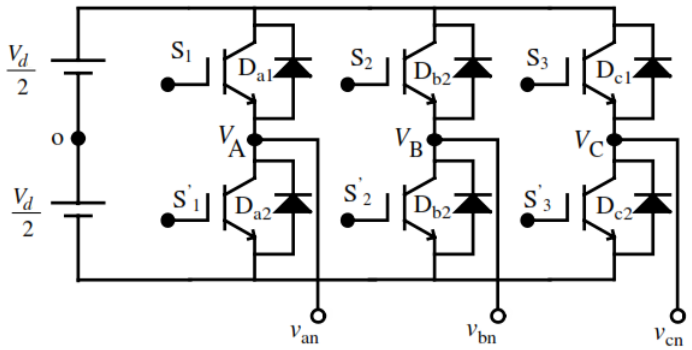

FIGURE 1.8: Power circuit topology of a three-phase voltage source inverter.

The eight valid switching states (=8 states) are shown in table 1.2. As in single-phase VSIs, the switches on any of the inverter legs (S_1 and S_4, S_3 and S_6, or S_5 and S_2) cannot be gated on simultaneously because this would cause a short circuit across the DC link voltage supply. Similarly, in order to avoid unwanted states in the VSI, and thus undefined AC output line voltages, the power switches on any leg of the inverter cannot be gated off simultaneously as this will result in voltages that will depend on the polarity of the respective line current. Within the eight valid states, two of them (7 and 8 in table 1.2) produce zero AC line voltages. In this case, free-wheeling AC line currents through the upper or lower components.
The remaining states (1 to 6 in Table 1.2) produce non-zero AC output voltages. In order to generate a given voltage waveform, the inverter toggles from one state to another. Thus, the resulting AC output line voltages consist of discrete voltage values that are vi, 0 and $-vi$ for the topology shown in Figure 1.8. The selection of the states to produce the given waveform is done by the modulation technique, which must ensure that only valid states are used.

TABLE 1.2: Operation of single phase inverter.

State	State	v_{ab}	v_{bc}	v_{ca}
S_1,S_2, and S_6 are on S_4,S_5, and S_3 are off	1	v_i	0	$-v_i$
S_2,S_3, and S_1 are on S_5,S_6, and S_4 are off	2	0	v_i	$-v_i$
S_3,S_4, and S_2 are on S_6,S_1, and S_5 are off	3	$-v_i$	v_i	0
S_4,S_5, and S_3 are on S_1,S_2, and S_6 are off	4	$-v_i$	0	v_i
S_5,S_6, and S_4 are on S_2,S_3, and S_1 are off	5	0	$-v_i$	v_i
S_6,S_1, and S_5 are on S_3,S_4, and S_2 are off	6	v_i	$-v_i$	0
S_1,S_3, and S_5 are on S_4,S_6, and S_2 are off	7	0	0	0
S_4,S_6, and S_2 are on S_1,S_3, and S_5 are off	8	0	0	0

Voltages are designated by a capital suffix letter VA, VB, VC and can reach the value $+0.5V_dc$ when the upper switch is on and $-0.5V_dc$ when the lower switch is on. The phase voltage applied to the load is designated by the letters v_an, v_bn, v_cn. The operation of the upper and lower switches is complementary (a small dead band is provided in the real-time implementation).

The relationship between the leg voltage and switching signals are:

$$V_k = S_k V_{dc}; \qquad k \in A, B, C \tag{1.19}$$

where $S_k = 1$ when the upper power switch is 'ON' and $S_k = 0$ when the lower switch is 'ON.'
If the load is supposed to be a three-phase wye connected load, then the relationship between phase-to-neutral load voltage and leg voltages can be written as follows:

$$\begin{aligned} V_A(t) &= v_a(t) + v_{nN}(t) \\ V_B(t) &= v_b(t) + v_{nN}(t) \\ V_C(t) &= v_c(t) + v_{nN}(t) \end{aligned} \tag{1.20}$$

Where v_{nN} is the voltage difference between the wye point n of the load and the negative rail of the DC bus N, called "common mode voltage". This common mode voltage or neutral voltage is responsible for leakage currents and their subsequent failure.

By adding each term in equation (1.20) and defining the sum of the phase-to-neutral voltage as zero (assuming a balanced three-phase voltage whose instantaneous sum is always zero), the following is obtained:

$$v_{nN}(t) = \frac{1}{3}\left[V_A(t) + V_B(t) + V_C(t)\right] \tag{1.21}$$

Substituting equation (1.21) back into equation (1.20), the following expressions for the phase-to-neutral voltage are obtained:

$$\begin{aligned} v_a(t) &= \tfrac{2}{3}V_A(t) - \tfrac{1}{3}\left[V_B(t) + V_C(t)\right] \\ v_b(t) &= \tfrac{2}{3}V_B(t) - \tfrac{1}{3}\left[V_A(t) + V_C(t)\right] \\ v_C(t) &= \tfrac{2}{3}V_C(t) - \tfrac{1}{3}\left[V_A(t) + V_B(t)\right] \end{aligned} \tag{1.22}$$

Equation (1.22) can also be written using the switching function definition of equation (1.19):

$$\begin{aligned} v_a(t) &= \left(\tfrac{V_{dc}}{3}\right)\left[2S_A - S_B - S_C\right] \\ v_b(t) &= \left(\tfrac{V_{dc}}{3}\right)\left[2S_B - S_A - S_C\right] \\ v_c(t) &= \left(\tfrac{V_{dc}}{3}\right)\left[4S_C - S_B - S_A\right] \end{aligned} \tag{1.23}$$

Equation (1.23) can be used to model a three-phase inverter in MATLAB/Simulink.[5]

1.5 Multiphase inverters

Electrical power generation, transmission and distribution are already available in three phases, and almost all loads are developed in three phase systems, and due to the rapid growing of power demands in the last decades with some limitations presented when using three phase drives such as the need of power semiconductors devices of large voltage and current rating in high power applications, as steel rolling, mine hoisting, locomotive traction and electric ship propulsion, higher voltage and larger current of the drive system are preferred. These power semiconductors are generally more expensive or unavailable which requires the reduction of the power per phase. This can be achieved by increasing the number of phase legs. Which yields a multiphase machines fed by a multiphase inverters [10].
The multiphase machine provides some advantages such as: ability to start and run even on one or two or more of its open or short-circuited stator phases, lower current per phase without increasing the voltage per phase, lower DC link current harmonics, higher reliability and increased power within the same framework [11] [12].
It is believed that the first tentative proposal for a variable speed five-phase induction motor was made in 1969 [1]. The five-phase inverter initially used operated in square mode. Within the last decades many researchers have been proposed a large number of multiphase machine, multiphase converters topologies and their corresponding control methods. Based on the types of power sources, converters are divided into Voltage Source Converters (VSC) and Current Source Converters

(CSC).

Zicheng L. et al [10] are classified the existing multiphase converter topologies as shown in Figure 1.9. Firstly, depending on the power conversion process, multiphase topologies can be divided into AC-DC-AC and AC-AC modes. AC-AC converters are also called matrix converters, which include direct and indirect types. Secondly, depending on the connection of the neutral points, multiphase topologies can be divided into open-winding and single-sided modes. Without connection to the neutral point, both ends of the open-winding topologies can be powered by one or two independent DC sources. In addition, single-sided topologies can contain one or more neutral points.

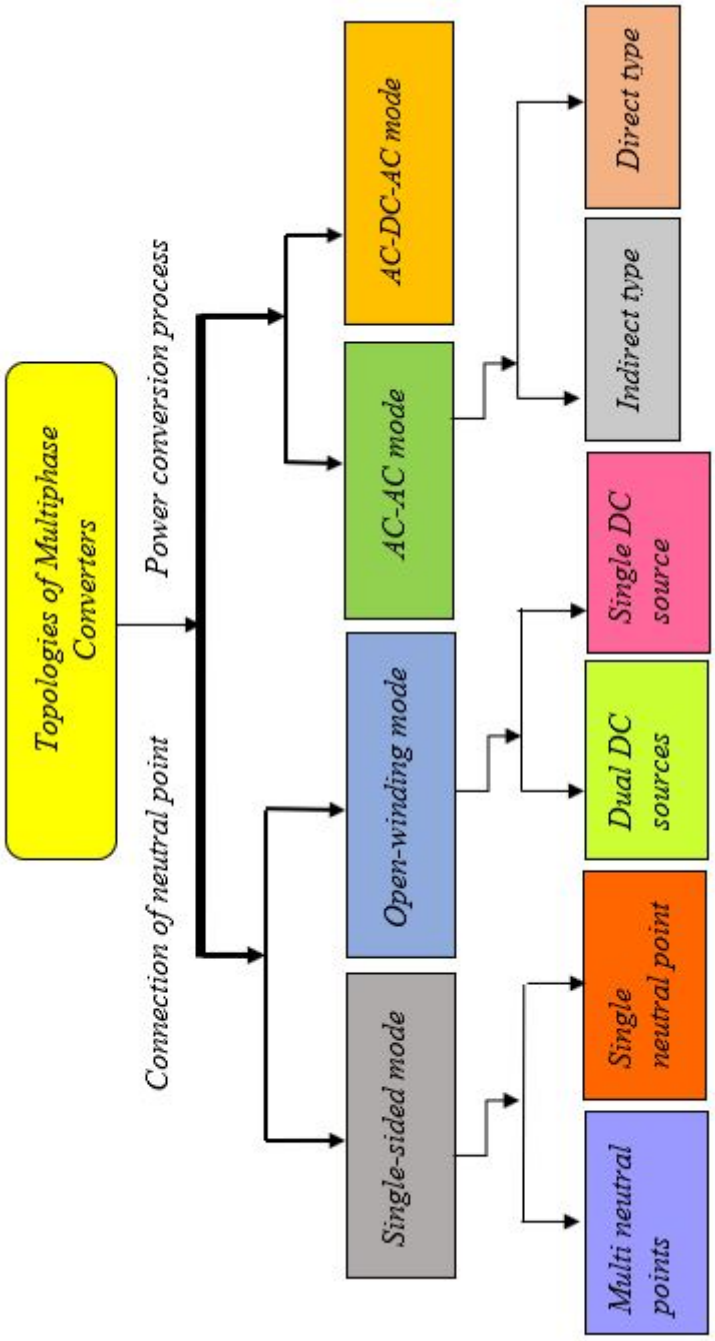

FIGURE 1.9: Classification of multiphase converter topologies.

1.5.1 AC-DC-AC mode

Figure 1.10 shows a multiphase two level converters, In this mode AC-DC-AC, as it is named, a successive conversion of power from AC power supplies to DC power, and then DC power is inverted into multiphase AC power, which finally feeds the multiphase machines. Here a DC link inserted between rectification and inversion. This topology can be extended to the multilevel topology, such as multiphase NPC converters [13][10].

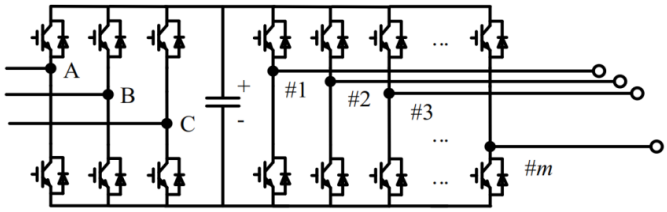

FIGURE 1.10: The topology of AC-DC-AC multiphase converters.

1.5.2 AC-AC mode

Figure 1.11 shows the AC-AC direct type multiphase two level converter and also named matrix converters, which achieve power conversion from AC to AC without additional link DC circuits. Direct matrix converters perform voltage and current conversion in one single stage [14],
Figure 1.12 shows the indirect type multiphase two level converter also known as indirect matrix converters, which act like the AC-DC-AC converters, and perform voltage/current rectification and inversion without intermediate energy storage elements [15].

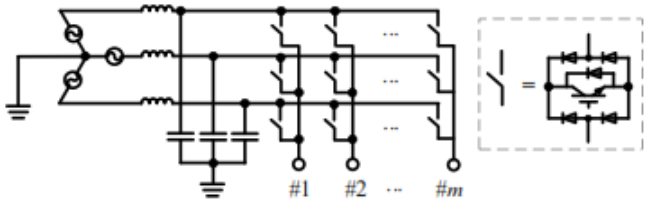

FIGURE 1.11: The topology of direct matrix multiphase converters.

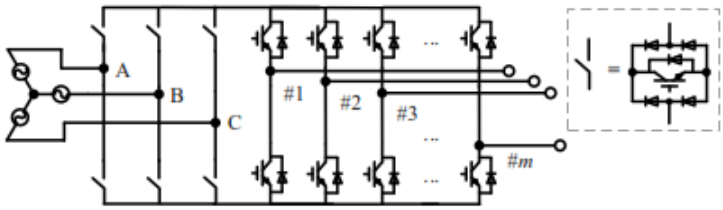

FIGURE 1.12: The topology of indirect matrix multiphase converters.

1.5.3 Open-winding mode

Figure. 1.13. shows the topology of open-winding multiphase converters with one DC voltage source. This means that both ends of the stator windings are connected to the converters. In this case for single DC source topology zero-sequence current could be very large even with very low CMV, which leads to additional copper loss in the machine windings. Therefore, many modified PWM methods are proposed to suppress the zero-sequence current. However, these methods usually reduce the utilization of DC bus [16][17].
Figure. 1.14. Shows the topology of open-winding multiphase converters with two DC voltage sources. This requires two isolated power sources, which further increases the cost but blocks the circulation of zero-sequence current. Additionally, two DC voltages can be set at different voltage levels, such as 2:1, to produce four-level output voltage [18].

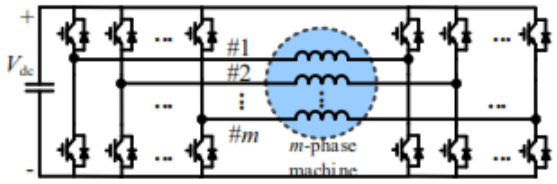

FIGURE 1.13: The topology of open-winding multiphase converters with one DC voltage source.

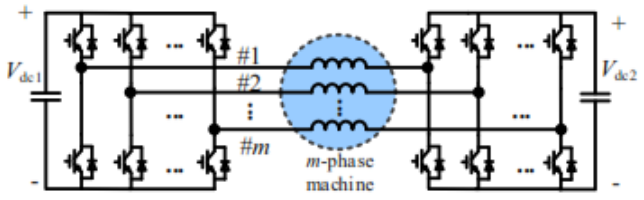

FIGURE 1.14: The topology of open-winding multiphase converters with two DC voltage sources.

1.5.4 Single-sided mode

Figure 1.15. Shows the topology of one-sided multiphase converters with one neutral point. Whereas Figure 1.16. Shows the topology of one-sided multiphase converters with multiple neutral points. This topology is widely used in multiphase applications, ranging from several kilowatts to hundreds of kilowatts [19, 20]. In reality it has two main disadvantages:

- Compared to open-winding topology, it loses control flexibility and fault-tolerant ability.
- PWM could lead to harmful bearing currents [62], and causes EMI problems [63].

The topology of one-sided multiphase converters with one neutral point.

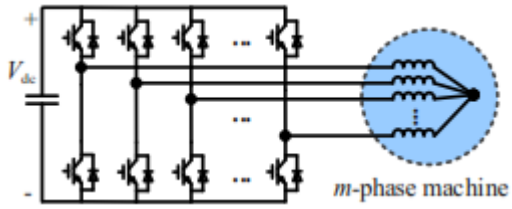

FIGURE 1.15: The topology of one-sided multiphase converters with one neutral point.

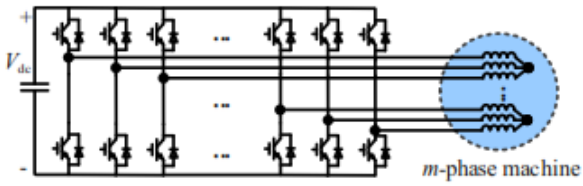

FIGURE 1.16: The topology of one-sided multiphase converters with multiple neutral points.

To simplify the notations, the output (polar) voltages for an n-phase inverter are denoted by V_1; V_2; V_3...V_m. We present here a simplified model of the n-phase inverter of Figure 1.15 feeding a star-balanced load. In this topology we distinguish three types of voltages, namely the (polar) voltage at the output of each arm, the simple phase voltage at the terminals of the load (voltage between the output of the arm and the neutral , v_{1n}, v_{2n}, v_{3n}...v_{mn}), and the line or composite voltage (between phases, either adjacent or non-adjacent phases, V_{12},V_{13},..., V_{25},...,etc.). In addition, there is a unique voltage V_{nN} characterizing the common mode voltage (CMV) between the neutral point of the load and the effective neutral representing the midpoint between the two DC input sources, its potential is considered equal to zero.

This common mode voltage or neutral voltage is responsible for leakage currents and their subsequent failure.

$$V_k(t) = S_K(t)\, V_{dc} \tag{1.24}$$

We use m number of phases instead of n to avoid confusion between n neutral and n legs).
Where $S_k = 1$ when the upper power switch is 'ON' and $S_k = 0$ when the lower switch is 'ON.'
If the load is supposed to be a three-phase wye connected load, then the relationship between phase-to-neutral load voltage and leg voltages can be written as follows:

$$\begin{aligned} V_1(t) &= v_1(t) + v_{nN}(t) \\ V_2(t) &= v_2(t) + v_{nN}(t) \\ V_3(t) &= v_3(t) + v_{nN}(t) \\ &\cdots\cdots \\ &\cdots\cdots \\ &\cdots\cdots \\ V_m(t) &= v_m(t) + v_{nN}(t) \end{aligned} \tag{1.25}$$

By adding each term in equation (3.12) and defining the sum of the phase-to-neutral voltage as zero (assuming a balanced three-phase voltage whose instantaneous sum is always zero), the following is obtained:

$$V_{nN}(t) = (\frac{1}{m})[(V_1(t) + V_2(t) + \ldots + V_m(t)] \tag{1.26}$$

Substituting equation (3.13) back into equation (3.12), the following expressions for the phase-to-neutral voltage are obtained:

$$\begin{aligned}
v_1(t) &= V_1(t) - \left(\tfrac{1}{m}\right)\left[V_1(t) + V_2(t) + V_3(t) \ldots + V_m(t)\right] \\
v_2(t) &= V_2(t) - \left(\tfrac{1}{m}\right)\left[V_1(t) + V_2(t) + V_3(t) \ldots + V_m(t)\right] \\
v_3(t) &= V_3(t) - \left(\tfrac{1}{m}\right)\left[V_1(t) + V_2(t) + V_3(t) \ldots + V_m(t)\right] \\
&\ldots\ldots \\
&\ldots\ldots \\
&\ldots\ldots \\
v_m(t) &= V_m(t) - \left(\tfrac{1}{m}\right)\left[V_1(t) + V_2(t) + V_3(t) \ldots + V_m(t)\right] \\
&\ldots\ldots \\
&\ldots\ldots \\
&\ldots\ldots \\
v_1(t) &= \left(\tfrac{1}{m}\right)\left[(m-1)\,V_1(t) - \left(V_2(t) + V_3(t) \ldots + V_m(t)\right)\right] \\
v_2(t) &= \left(\tfrac{1}{m}\right)\left[(m-1)\,V_2(t) - \left(V_1(t) + V_3(t) \ldots + V_m(t)\right)\right] \\
v_3(t) &= \left(\tfrac{1}{m}\right)\left[(m-1)\,V_3(t) - \left(V_1(t) + V_2(t) \ldots + V_m(t)\right)\right] \\
&\ldots\ldots \\
&\ldots\ldots \\
&\ldots\ldots \\
v_m(t) &= \left(\tfrac{1}{m}\right)\left[(m-1)\,V_m(t) - \left(V_1(t) + V_2(t) \ldots + V_{(m-1)}(t)\right)\right]
\end{aligned} \tag{1.27}$$

Equation (1.27) can also be written using the definition of the switching function from equation (1.24):

$$\begin{aligned}
v_1(t) &= \tfrac{Vdc}{m}\left[(m-1)\,S_1 - S_2 - S_3 - \ldots - S_m\right] \\
v_2(t) &= \tfrac{Vdc}{m}\left[(m-1)\,S_2 - S_1 - S_3 - \ldots - S_m\right] \\
v_3(t) &= \tfrac{Vdc}{m}\left[(m-1)\,S_3 - S_1 - S_2 - \ldots - S_m\right] \\
&\ldots\ldots\ldots\ldots \\
&\ldots\ldots\ldots\ldots \\
&\ldots\ldots\ldots\ldots \\
v_m(t) &= \tfrac{Vdc}{m}\left[(m-1)\,S_m - S_1 - S_2 - \ldots - S_{(m-1)}\right]
\end{aligned} \tag{1.28}$$

The simple phase voltages can be deduced in function of the leg (or line or pole) voltages or using the definition of the switching function, for any system.

For three phase system:

$$\begin{aligned}
v_1(t) &= \left(\tfrac{1}{3}\right)\left[2V_1(t) - V_2(t) - V_3(t)\right] \\
v_2(t) &= \left(\tfrac{1}{3}\right)\left[2V_2(t) - V_1(t) - V_3(t)\right] \\
v_3(t) &= \left(\tfrac{1}{3}\right)\left[2V_3(t) - V_1(t) - V_2(t)\right]
\end{aligned} \tag{1.29}$$

$$\begin{aligned} v_1(t) &= \tfrac{Vdc}{3}\left[2S_1 - S_2 - S_3\right] \\ v_2(t) &= \tfrac{Vdc}{3}\left[2S_2 - S_1 - S_3\right] \\ v_3(t) &= \tfrac{Vdc}{3}\left[2S_3 - S_1 - S_2\right] \end{aligned} \tag{1.30}$$

And for five system

$$\begin{aligned} v_1(t) &= \left(\tfrac{1}{5}\right)\left[4V_1(t) - V_2(t) - V_3(t) - V_4(t) - V_5(t)\right] \\ v_2(t) &= \left(\tfrac{1}{5}\right)\left[4V_2(t) - V_1(t) - V_3(t) - V_4(t) - V_5(t)\right] \\ v_3(t) &= \left(\tfrac{1}{5}\right)\left[4V_3(t) - V_1(t) - V_2(t) - V_4(t) - V_5(t)\right] \\ v_4(t) &= \left(\tfrac{1}{5}\right)\left[4V_4(t) - V_1(t) - V_2(t) - V_3(t) - V_5(t)\right] \\ v_5(t) &= \left(\tfrac{1}{5}\right)\left[4V_5(t) - V_1(t) - V_2(t) - V_3(t) - V_4(t)\right] \end{aligned} \tag{1.31}$$

$$\begin{aligned} v_1(t) &= \tfrac{Vdc}{5}\left[4S_1 - S_2 - S_3 - S_4 - S_5\right] \\ v_2(t) &= \tfrac{Vdc}{5}\left[4S_2 - S_1 - S_3 - S_4 - S_5\right] \\ v_3(t) &= \tfrac{Vdc}{5}\left[4S_3 - S_1 - S_2 - S_4 - S_5\right] \\ v_4(t) &= \tfrac{Vdc}{5}\left[4S_4 - S_1 - S_2 - S_3 - S_5\right] \\ v_5(t) &= \tfrac{Vdc}{5}\left[4S_5 - S_1 - S_2 - S_3 - S_4\right] \end{aligned} \tag{1.32}$$

1.6 Conclusion

As a conclusion, in this chapter we have discussed the two level inverters by focusing on the basic structure of these inverters starting from half-bridge to full-bridge and then three-phase inverter are elaborated on. In addition, and, due to the need of multiphase inverters a classification of the existing multiphase converter topologies are presented.

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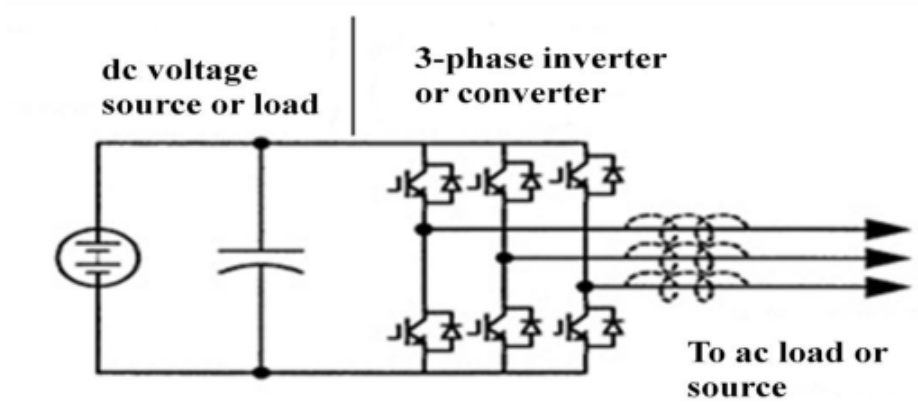
Chapter 2

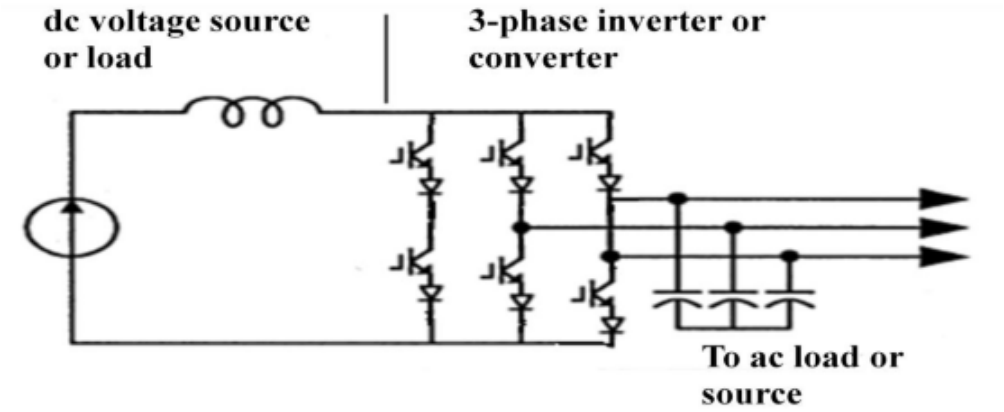
Different topologies of Zsource Inverters.

2.1 Traditional three phase voltage source inverter

Figure 2.1(a) shows the traditional three phase voltage source inverter (VSI) structure. And Figure 2.1(b) shows the traditional three phase curren source inverter (CSI) structure. The VSI is fed by a DC voltage source supported by a relatively large capacitor connected in parallel to the input terminals tending to smooth the DC input voltage. The DC voltage can be a battery,fuel-cell stack, diode rectifier or capacitor. Whereas the (CSI) is fed by DC current source, which can be a large inductor connected in series with a battery,fuel-cell stack, diode rectifier. For both VSI and CSI the main circuit inverter bridge composed of six switches, each consisting of a power transistor and an anti-parallel diode (i.e. self-commutated device like MOSFET, IGBT, GTO, etc.) to provide bidirectional current flow and unidirectional voltage blocking capability. It has eight switching states, among these eight states, six are active states and two are zero states, while the short circuit of at least one leg of a three phase inverter are seven forbidden states. VSI can be operated as a stepped-wave inverter or a pulse width modulation (PWM) inverter. When the voltage source inverter is operated as a stepped-wave inverter, then the transistor is switched in the sequence of their number with a time difference of T/6.



(a)



(b)

FIGURE 2.1: Traditional inverter (a) VSI , (b) CSI.

These conventional inverters have many limitations and drawbacks such as for :

1. Voltage source inverter;
    - The AC output voltage is limited below, and cannot exceed the DC rail voltage.
    - Needs additional DC-DC converter stage, leads to increased system cost and lowers efficiency.
    - The upper and lower devices of each phase leg cannot be gated simultaneously, otherwise a shoot through state would occur, causes a short circuit to the DC supply, and hence destroying the devices.
    - The shoot-through problem by electromagnetic interference (EMI) noise's miss-gating-on is one of the main problems in terms of reliability of the inverter.
    - An output LC filter is required to provide a sinusoidal voltage compared to the CSI, which results in additional power loss and control complexity.

2. Current source inverter;

    - The current source inverter is a boost inverter for DC-to-AC power conversion, and the current source converter is a buck converter for AC-to-DC conversion. An additional DC-DC converter(buck or boost) is required for special applications. The insertion of the DC-DC stage increases system cost and lowers efficiency.
    - At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the DC inductor would occur and destroy the devices. The open-circuit problem by EMI noise's misgating off is a major concern of the converters reliability. Overlap time for safe current commutation is needed in the current source converter, which also causes waveform distortion.
    - The main switches of the current source converter must block the reverse voltage that needs the use of a series diode in a conjunction with high-speed, high-performance transistors such as insulated gate bipolar transistors (IGBTs). This precludes the direct use of low-cost, high-performance IGBT modules and intelligent power modules (IPMs).

In addition, both voltage source and current source converters have the following common drawbacks:

- They are only either boost or buck converters.
- They are vulnerable to EMI noise in terms of reliability.
- In VSI two switches cannot be gated on at the same time, and in CSI one of the upper switches and one of the lower switches must be gated on at any time, these require dead time for VSI and overlap time for CSI to provide safe commutation but causes waveform distortion.
- The main switching device of VSI and CSI are not interchangeable.

During the last four decades of the twentieth century, researchers have spent a lot of time to overcome limits and problems that are faced in the traditional voltage source inverter (VSI) and current source inverter (CSI), especially, the short circuit of at least one leg, and the buck-boost mode problems. For applications where over drive is required and the available dc voltage is not sufficient then an additional DC-DC boost converter is required to get the desired ac output Figure 2.2. These additional converter stages raise the system cost and lower down the efficiency.

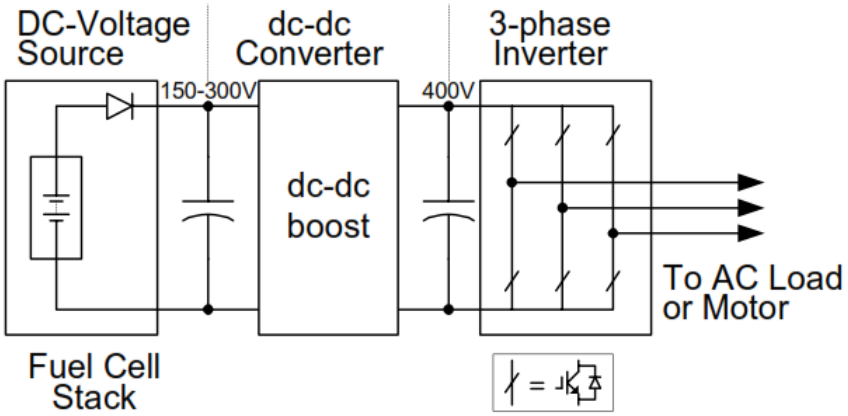


FIGURE 2.2: Traditional two-stage inverter.

2.2 Review of Z- Source Inverter

To overcome the above mentioned problems of the traditional VSI and CSI converters, by the end of 2002 F. Z. Peng [1] was introduced an impedance source power converter (abbreviated as Z-source) and its control method for implementing DC to AC, AC to DC, AC to AC and DC to DC conversion. Figure 2.3 shows the proposed general Z-source converter structure. It uses a single impedance network to couple the main circuit of the converter to the DC power source, load, or another converter, to provide unique functionality that cannot be seen in traditional VSI and CSI converters. The impedance network consists of two inductors and two capacitors connected to each other in X-shape that forms a symmetrical second order filter network. The values of the two inductors and the two capacitors are equal (L1=L2 & C1=C2). The shoot through can no longer destroy the device and the efficiency of the inverter is high.

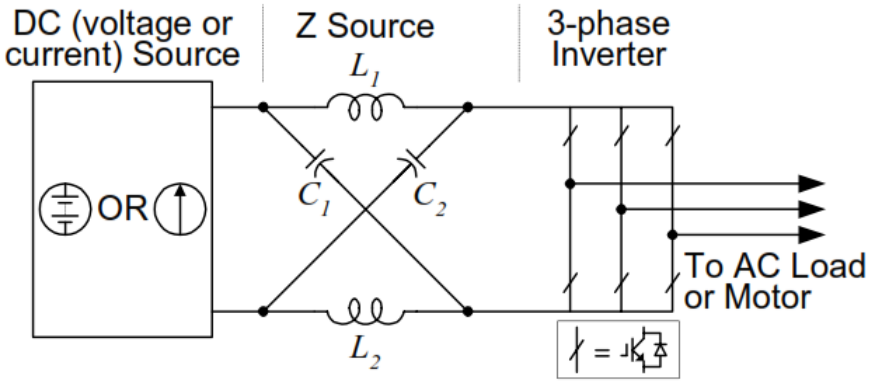


FIGURE 2.3: A general structure of the Z-source converter.

2.2.1 Operation of ZSI

The unique feature of the Z-source inverter is that the output AC voltage can be any value between zero and infinity, regardless of the fuel cell voltage. In other words, the Z-source inverter is a buck-boost inverter that has a wide achievable voltage range. Traditional V- and I-source inverters cannot offer such functionality. [1][2].
The three-phase ZSI bridge as shown in figure 2.4 has nine allowed switching states unlike the traditional VSI, which has eight switching states. The ZSI has six active states when DC voltage is applied across the three-phase load, and two zero states when the load terminals are shorted by the three lower or upper switching devices, respectively. The ninth state, the shoot through state occurs when the load terminals are shorted by the top and bottom switching devices of any phase leg (this state is prohibited in traditional inverters to avoid the shoot through state). This shoot through state sometimes also called "third zero state" can be achieved in seven different ways: ST through any phase leg, combinations of every two-phase legs and every three-phase legs [3, 4, 5].

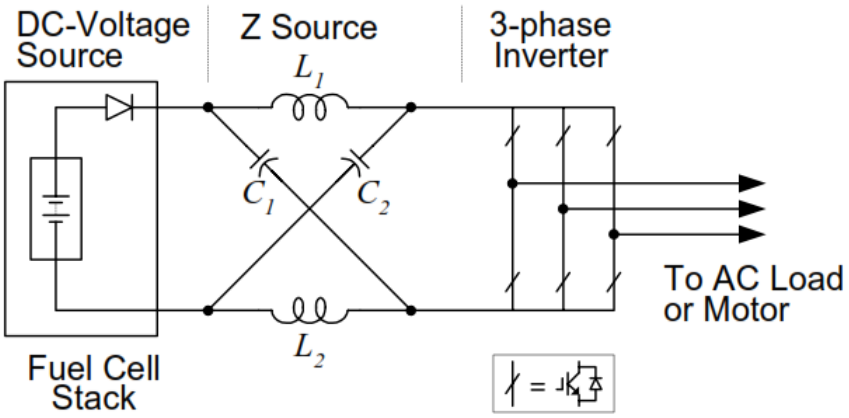


FIGURE 2.4: A Z-source inverter for fuel cell applications.

2.2.2 Circuit Analysis

The equivalent circuit of a Z-source inverter is shown in Figure 2.5. For one switching cycle, T, the interval of the shoot through state is $T0$, the interval of the non-shoot through state is $T1$, and the shoot through duty cycle ratio is defined as $D = T0/T$. The two inductances and capacitances are assumed to be identical(i.e ; $L = L1 = L2$ and $C = C1 = C2$) The inverter acts as a constant current source when viewed from the impedance source to the inverter side, as shown in Figure 2.6, where the inverter is operating in 'non-shoot-through' mode. In "shoot-through" mode Figure 2.7, the inverter is a short circuit and the equivalent diode at the DC input is open circuit.

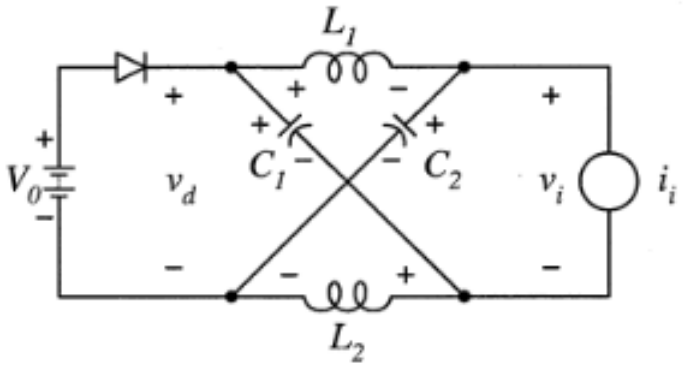


FIGURE 2.5: The equivalent circuit of a Z-source inverter.

2.2.2.1 Non-shoot-through state

During the interval of non-shoot-through state T1, the switching scheme of the ZSI is similar to that of a VSI. The inverter bridge, seen from the DC side, is equivalent to a current source. The input DC voltage is available as DC link voltage input to the inverter, making the ZSI behaves like a conventional VSI.
Figure 2.6 shows the equivalent circuit of Z-source inverter viewed from the dc link when the inverter bridge is in the non-shoot-through state.

The equivalent circuit of a Z-source inverter, viewed from the DC link when the inverter bridge is in the non-shoot-through state

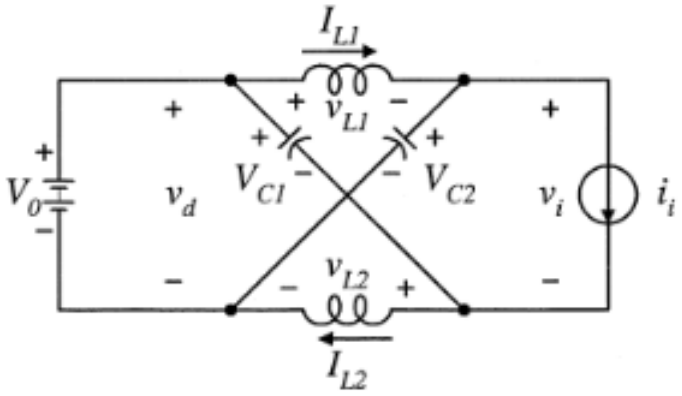


FIGURE 2.6: The equivalent circuit of a Z-source inverter, viewed from the DC link when the inverter bridge is in the non-shout through state.

In this equivalent circuit of Z-source inverter, the following equations are valid:

$$v_{L-nsh} = \quad V_{L2} \ = V_{in} - V_{C1} \tag{2.1}$$

$$V_{PN} = V_{C1} - V_{L1} \tag{2.2}$$

$$V_d = V_{in} \tag{2.3}$$

Due to the symmetrical impedance network, the following relations are true :

$$V_{L1} = V_{L2} = VL \tag{2.4}$$

$$V_{C1} = V_{C2} = VC \tag{2.5}$$

Equation (2) can be written as :

$$V_{PN} = 2V_{C1} - V_{in} \tag{2.6}$$

2.2.2.2 The shoot-through state

In this case during T0, the switches of the same leg in the inverter bridge are switched on simultaneously for a very short time. The DC source is not bypassed, because of the presence of the LC network that links the DC source and the input of the inverter compared to the conventional topology of VSI, while increasing the output voltage. The DC link voltage of the LC network during transient states is increased by a boost factor, of which depends on the shoot through duty ratio for a given modulation index.

The equivalent circuit of Z-source inverter, during shoot-through state is shown in figure 2.7.

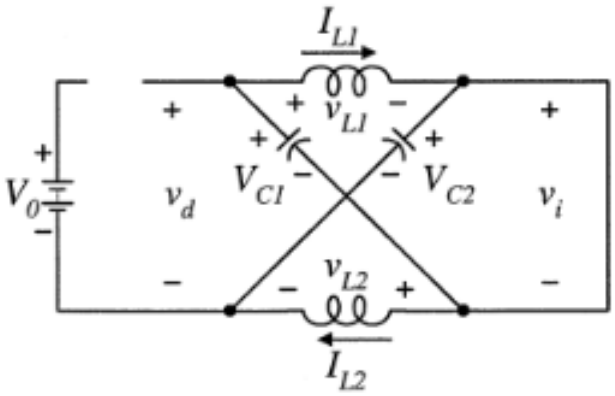


FIGURE 2.7: The equivalent circuit of a Z-source inverter viewed from the DC link when the inverter bridge is in the shoot through state.

So we have:

$$V_d = 2V_C \tag{2.7}$$

$$v_{L-sh} = V_L = V_C \tag{2.8}$$

$$V_{PN} = 0 \tag{2.9}$$

At steady state, the average voltage of inductors over one switching period is zero.Then from equations (1) and (5), this average voltage across the two inductance of the qZ-source can be rewritten as:

$$\begin{aligned} V_L T &= v_{L-sh} T_{sh} + v_{L-nsh} T_{nsh} = 0 \\ V_L T &= V_C T_{sh} + (V_{in} - V_C)\, T_{nsh} = 0 \end{aligned} \tag{2.10}$$

his equation can be solved for voltages across the capacitors, using the input voltage and the periods of times of shoot-through and non-shoot-through periods, the following equation is obtained:

$$\frac{V_C}{V_{in}} = \frac{T_{nsh}}{T_{nst} - T_{st}} \tag{2.11}$$

The peak dc voltage across the inverter bridge can be calculated using equations (2.6) and (2.11) :

$$\begin{aligned} V_{PN} = 2V_C - V_{in} = \tfrac{2V_C - V_{in}}{V_{in}} V_{in} &= \left(2\tfrac{V_C}{V_{in}} - 1\right) V_{in} \\ &= \left(2\tfrac{T_{nsh}}{T_{nsh} - T_{sh}} - 1\right) V_{in} = \tfrac{T_s}{T_{nsh} - T_{sh}} V_{in} = B V_{in} \end{aligned} \tag{2.12}$$

The ratio between the output voltage of the impedance Z-source V_{PN} and the input dc voltage V_{in} represents the boost factor, such as :

$$B = \frac{T_s}{T_{nsh} - T_{sh}} = \frac{1}{1 - 2\frac{T_{sh}}{T_s}} = \frac{1}{1 - 2D} \tag{2.13}$$

Where D is the duty cycle, and the output peak phase voltage of the Zsource inverter $\widehat{V_{ac}}$ can be expressed as:

$$\hat{V}_{ac} = M\frac{V_{PN}}{2} = MB\frac{V_{in}}{2} = G\frac{V_{in}}{2} \tag{2.14}$$

Where M is the modulation index, and G is the voltage gain of the inverter.

2.3 Zsource Inverter topologies

Different control approaches have been utilized to solve some of the aforementioned difficulties, such as reducing the voltage stress across the switches and capacitors while increasing the boost [9]-[11]. In the following chapter, these techniques are discussed in further depth, especially the simple boost, maximum boost and maximum constant boost controls. Other approaches, such as switched-inductor (SL), hybrid SC/SL, switched-capacitor (SC), voltage-lift (VL) techniques and voltage multiplier cells, have been widely employed to increase the step-up capacity in transformerless and cascade configurations [12]-[18].
As a result, by incorporating these modification circuits into the Z-Source inverters, various ideas for enhancing impedance-type inverters are provided.
The most of Z-Source topologies are covered in this part, along with their advantages and disadvantages based on power circuit change.

2.3.1 Classical Z-Source Inverter [16]-[23]

Figure 2.8 depicts a basic Z-Source Inverter (ZSI). To save cost, with this configuration DC-AC inverters should just have one stage. The following are some of ZSI's characteristics:

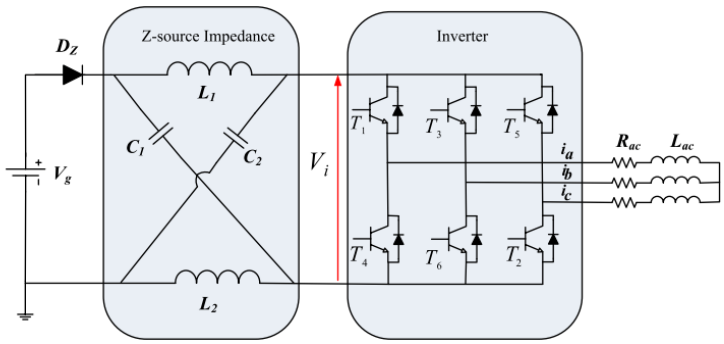


FIGURE 2.8: Classical Z-Source Inverter.

Advantages:

- ➢ Provides the buck-boost function by one stage conversion;
- ➢ Miss-gating on and off by EMI noise does not destroy the converter;
- ➢ Has the advantages of both traditional converters: V- and I- converters;
- ➢ Has low common-mode noise.

Disadvantages:

- ➢ Inrush current at start up;
- ➢ Low boost factor;
- ➢ High voltage stress on switches and capacitors;
- ➢ There is a diode at input which makes the current discontinuous;
- ➢ Need snubber circuit to reduce the losses during shoot-through state and to reduce the overshot voltage.
- ➢ Light load problems (over boosting);
- ➢ There is no common DC rail between the source and inverter.

Following on, all listed topologies below are reviewed and compared into the classical Z-Source.

2.3.1.1 The Bidirectional Z-Source Inverter [24]-[28]

A bi-directional Z-Source inverter is shown in Figure 2.9. The input diode D_z is replaced with a bidirectional switch $T7$, which has the following characteristics when compared to the traditional Z-Source inverter depicted in Figure 2.8:

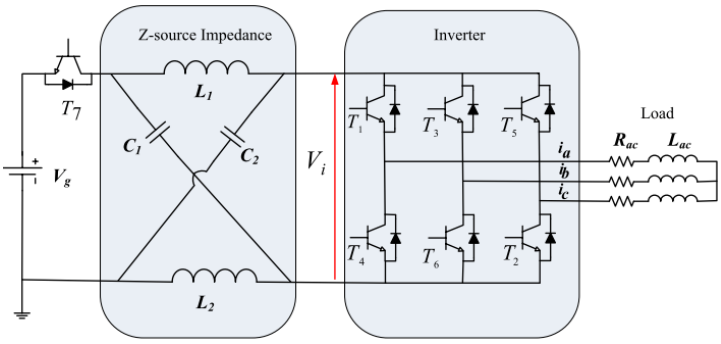


FIGURE 2.9: The Bidirectional Z-Source Inverter.

Advantages:

- ➢ Bidirectional topology (makes it suitable for storage application).

Disadvantages:

- ➢ Require special design with single renewable energy source like photovoltaic and fuel cell (bi-direction issue).

2.3.1.2 High Performance Z-Source Inverter [29]-[30]

To overcome the limitations of standard Z-Source inverters, a high-performance Z-Source inverter is presented. Figure 2.10 depicts a high-performance Z-Source with the following features:

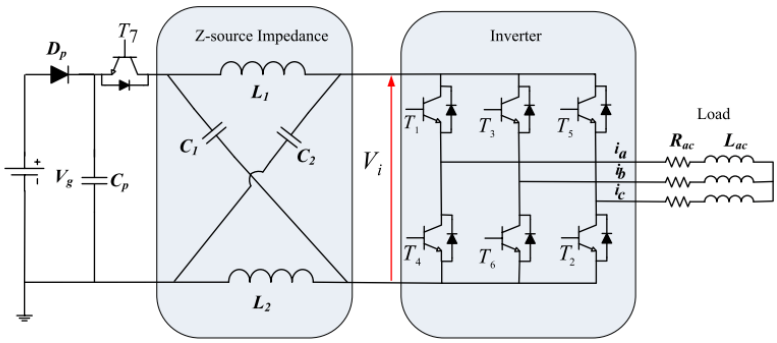


FIGURE 2.10: High performance Z-Source inverter.

Advantages:

- ➢ Operate at wide load range (even no-load) with small inductor;
- ➢ Eliminate the possibility of the DC-link voltage drops (named sometimes over boosting) at light load.

2.3.1.3 Novel Four-Switch Z-Source Three-Phase Inverter [31]-[32]

The advantages of a typical four-switch three-phase inverter are combined with the advantages of the Z-Source inverter in this topology. Figure 2.11 depicts the four Z-Sources, which have the following characteristics:

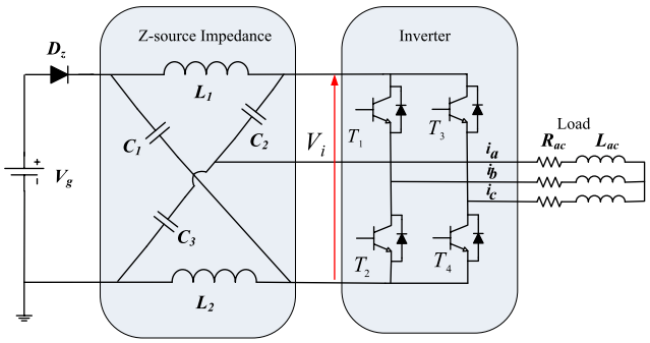


FIGURE 2.11: Four-Switch Z-Source.

Advantages:

- ➢ Less number of switches.

Disadvantages:

➢ The load and voltage current are not symmetrical due to the connection of one phase to the common node of capacitors.

2.3.1.4 Embedded Z-Source inverter [33],[34]

In traditional Z-Source, the discontinuous mode is a disadvantage. The embedded Z-Source, as illustrated in Figure 2.12, is presented as a solution to this problem. This topology's benefits and drawbacks may be summarized as follows:

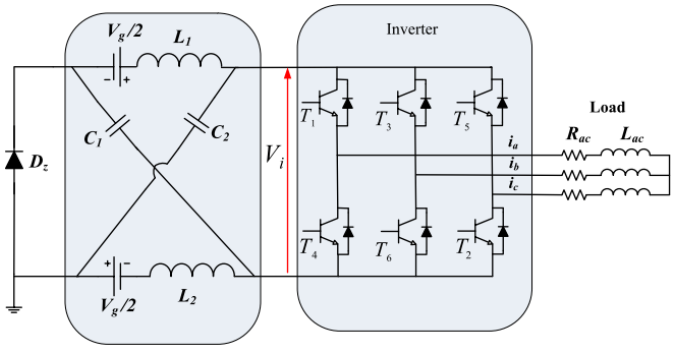


FIGURE 2.12: Embedded Z-Source inverter.

Advantages:

➢ The DC input current flows smoothly during the whole switching period;

➢ Passive and active components used have lower-voltage/current stress.

Disadvantages:

➢ The DC sources must be equal so it not suitable for PV sources.

2.3.1.5 Quasi Z-Source Inverter [35]-[42]

Figure 2.13 depicts the Quasi Z-Source inverter. The issue of discontinuous mode functioning is resolved. The benefits and drawbacks are outlined as follows:

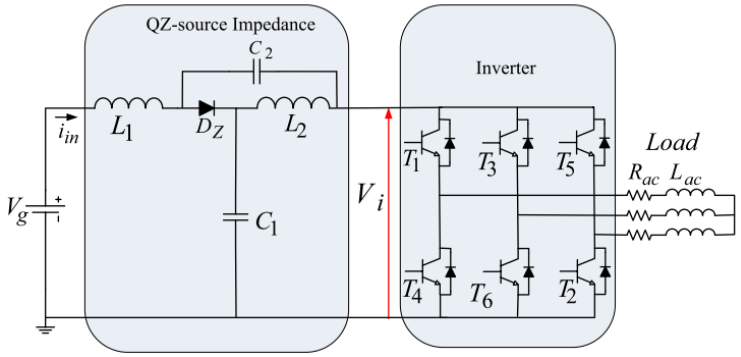


FIGURE 2.13: Quasi Z-Source Inverter.

Advantages:

- ➢ Continuous input current;
- ➢ Does not require input capacitance;
- ➢ Common DC rail between the source and inverter;
- ➢ Remove inrush current.

Disadvantages:

- ➢ High DC Voltage on capacitors.

2.3.1.6 Improved Z-Source/Series Z-Source [43],[44]

The traditional topology is hampered by excessive capacitor stress and inrush current. The topology depicted in Figure 2.14 overcomes these issues, and its characteristics can be summarized as follows:

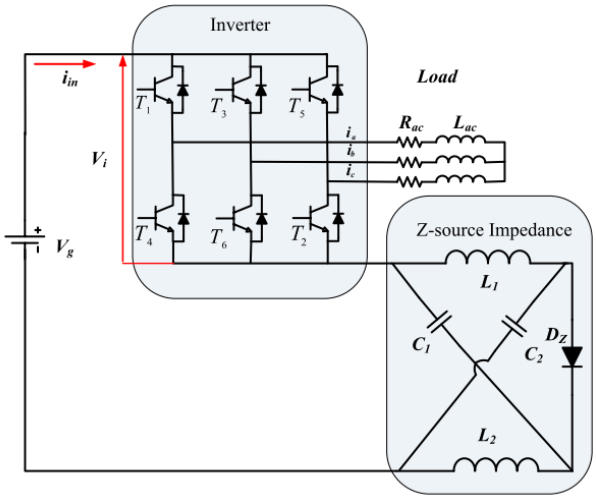


FIGURE 2.14: Improved Z-Source Inverter (IZSI).

Advantages:

- ➢ Decrease the voltage stress across the capacitors;
- ➢ Reduce the inrush current;
- ➢ Soft starting.

2.3.1.7 Trans-Z-source/ Trans-quasi-Z-Source [45]-[49]

Figure 2.15 illustrates a Trans-Quasi Z-Source, which consists of a transformer and one capacitor. It does, however, keep the main aspects of the previously disclosed Z-Source network. Its characteristics are as follows:

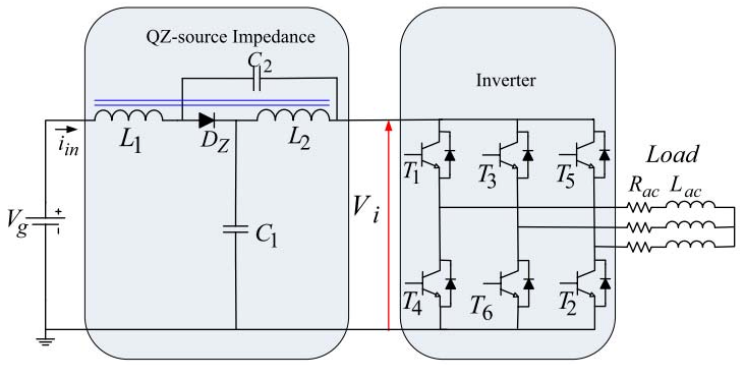


FIGURE 2.15: Trans-Quasi Z-source.

Advantages:

- ➢ High boost factor.

Disadvantages:

➢ Use transformer which has a negative impact on efficiency.

2.3.1.8 Improved Trans-Z-Source/Quasi Z-Source Inverter [50]

This architecture is part of a novel family of high boosting voltage inverters that improves on common trans-Z-Source and trans-quasi-Z-Source inverters, as seen in Figure 2.16. It has the following characteristics:

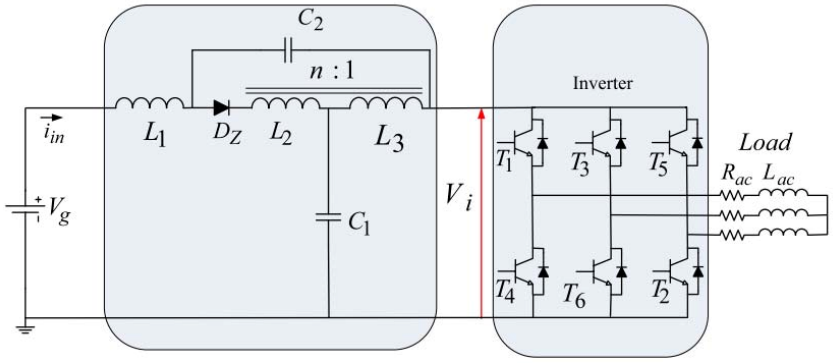


FIGURE 2.16: Improved Trans Quasi Z-Source Inverter.

Advantages:

➢ Continuous input current;

➢ High boost factor.

Disadvantages:

➢ Use transformer which has a negative impact on the efficiency.

2.3.1.9 Switched Inductor Z-Source, Switched Inductor Quasi Z-Source, Generalized Multi-Cell Switched-Inductor and Switched-Capacitor Z-Source Inverters [51]-[61]

As illustrated in Figure 2.17, the switched inductor may be inserted in both the conventional Z-Source and the quasi Z-Source. When compared to the typical switched-inductor ZSI, this class of inverters has higher boost voltage inversion capability and reduced voltage stress across the active switching components. Other characteristics of this family include:

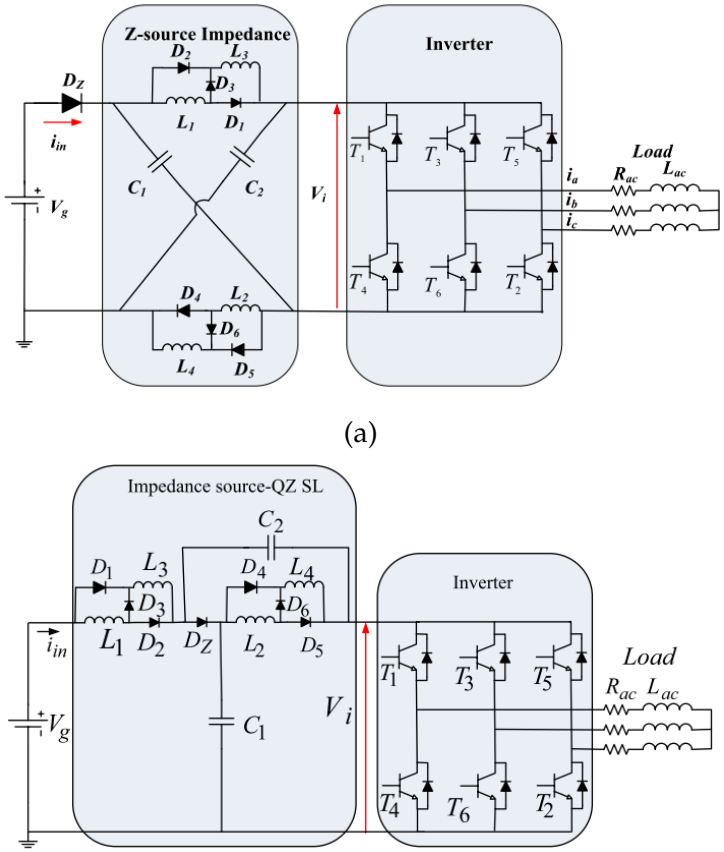


FIGURE 2.17: a) Switched Inductor Z-Source b) Switched Inductor Quasi Z-Source Inverter.

Advantages:

- ➢ Continuous input current in quasi topologies;
- ➢ High boost factor.

Disadvantages:

- ➢ High component counts;

2.3.1.10 Tapped-Inductor Z-Source Inverters [62]

The idea behind the new tapped inductor (TL) Z-Source impedance network for developing Z-Source inverters is to replace the original two inductors in the classical impedance network with two modified 2-terminal TL cells, as illustrated in figure 2.18. Only five diodes and two TL cells are required to provide voltage gains that are much higher than those of conventional approaches. This leads to improved weight, size, complexity, and cost. The benefits and drawbacks of this topology can

be outlined as follows:

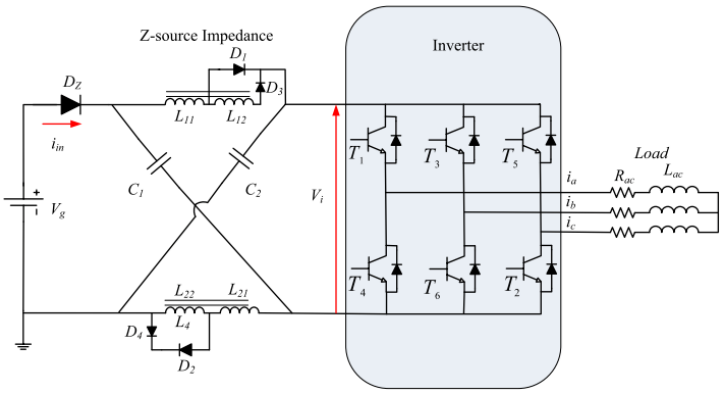


FIGURE 2.18: Tapped-Inductor Z-Source Inverters.

Advantages:

- ➢ Less number of switches;
- ➢ High voltage gain;
- ➢ Compared with the SL cell, the proposed TL cell is more compact;
- ➢ Flexibility as turn ratio freely adjustable to produce any desired voltage gain.

Disadvantages:

- ➢ Use tap-inductor which has a negative impact on the efficiency.

2.3.1.11 (Inductor-Capacitor-Capacitor-Transformer)-Z-Source Inverters LCCT ZSI [63]-[64]

As illustrated in Figure 2.19, this topology offers the integration of a quasi-Z-Source inverter (QZSI) with a built-in high frequency transformer.

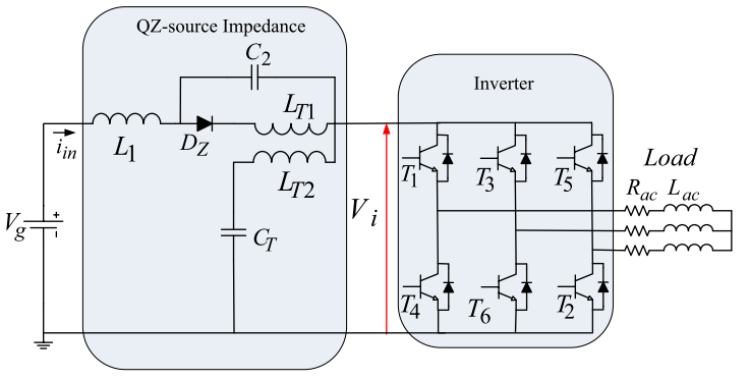


FIGURE 2.19: LCCT-Z-Source Inverter.

Advantages:

- ➢ Continuous input current.
- ➢ Improved relationship between boost coefficient and modulation index and improved EMI performance.
- ➢ There is no core saturation.

Disadvantages:

- ➢ Use transformer which has a negative impact on the efficiency.

As a conclusion to this analysis of the various Z-source inverter topologies[65], some modifications to the fundamental ZSI structure have recently been implemented. These enhancements may be classified into five categories:

- ➢ Rearrangement of the basic LC Z-network structure introduces the continuous input current feature and so the improvement in electromagnetic interference (EMI) performance [embedded Z-source inverter (EZSI) and quasi-Z-source inverter (qZSI)].
- ➢ Replacement of basic LC Z-network with equivalent three port transformer-capacitor network introduces other features of reduction in the component count and improved relationship between boost factor B and modulation index M when the transformer voltage-turns ratio n>1 is applied [T-source inverter (TSI), trans- Z-source inverter (TZSI) and trans quasi-Z-source inverter (TqZSI)].
- ➢ Series connection of several LC qZ-networks combines the previous features of continuous input current, improved EMI performance and improved dependence between voltage gain and modulation index MB-M [cascaded quasi Z-source inverters (CqZSI)].

- ➢ Replacement of two inductors of basic LC Z-network with switched inductor (SL) circuits introduces higher voltage gain and so improved the MB-M relation [switched inductor ZSI (SL ZSI)].
- ➢ Series connection of LC impedance with the inverter introduces a reduced voltage stress on capacitor and a reduced inrush current [improved/series Z-Source inverter].

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Chapter 3

PWM Schemes for Z Source Inverter Topology

3.1 Introduction

Efficient and fast control of electrical energy is one of the key technologies of modern power electronics. It is achieved with the help of electronic power converters. The converters transfer energy from a source to a controlled process in a quantized manner, using solid-state switches that are turned on and off at rapid repetition rates. Many switching functions are generated via different proposed algorithms using the so called - pulse width modulation techniques [1]. They range from simple timing schemes to involved real-time optimization methods. In contrast to the traditional inverter, all Z-source inverter topologies have an additional state beside the eight states for three-phase applications. The main idea of PWM control is how to insert this state. This state occurs when two of one leg or all switches are turned on at the same time. The output voltage in the shoot-through state is zero, which corresponds to the zero states in traditional inverters. The three main different control techniques are discussed below.

3.2 Simple boost control

This was the first PWM control proposed by F.Z.Peng with a new feature of ZSC. Basically, this control consists of two straight lines upper line V_p and lower line V_n used as shoot-through modulating signals, and reference signals Va, Vb, Vc that compare with the carrier signal V_tr as shown in Figure 3.1. This control strategy inserts shoot through in all the PWM traditional zero states during one switching period. When the triangular carrier signal is greater than the upper envelope, V_p or less than the lower envelope, V_n, the circuit turns into a shoot through state. Otherwise, the six active states are kept unchanged as in conventional carrier-based PWM [2]. Since the value of the positive straight line is equal to the maximum of the sinusoidal reference signals and the value of the negative straight line is equal to the minimum of the sinusoidal reference signal, then the modulation index (M) and the duty cycle (

D_o) are interdependent on each other. The relationship between these two parameters is expressed in equation (3.1). We can see from the equation that the duty cycle (D_o) decreases with increasing modulation index (M).

$$D_0 = 1 - M \tag{3.1}$$

In early studies, this control proves a z-source design capable of buck and boost power conversion under an open-loop system. However, under this control, the voltage stress across the power devices is high because a certain zero state condition is not used.

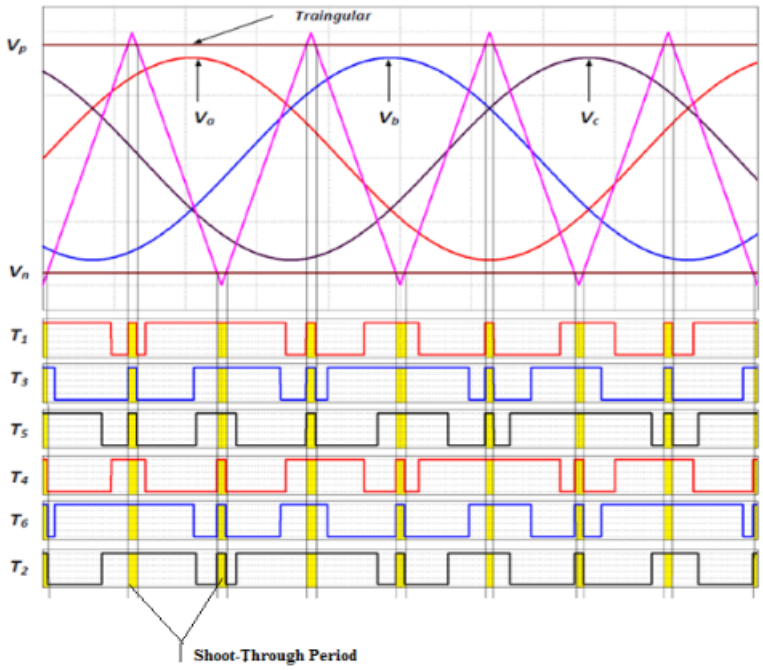


FIGURE 3.1: Simple Boost Control signals.

And we have the voltage gain given by:

$$G = BM = \frac{M}{1 - 2D_0} \tag{3.2}$$

Since $D_0 = 1 - M$, thus

$$G = \frac{M}{1 - 2D_0} = \frac{M}{1 - 2(1 - M)} = \frac{M}{2M - 1} \tag{3.3}$$

Equation (3.3) states that the gain of the inverter (G) can be controlled by adjusting the modulation index (M). If we rearrange the AC output voltage equation in the

original form of PWM output voltage equation, we get

$$\widehat{V}_{out} = M\frac{\mathrm{BV}_{dc}}{2} \tag{3.4}$$

When we compare equation (4) to the maximum sinusoidal inverter output voltage of the traditional VSI we can deduce that the voltage applied to the inverter is :

$$V_{inv} = BV_{dc} \tag{3.5}$$

Also represents the voltage stress applied to the switches.

Using equations (3.2) and (3.3), one can get

$$B = 2G - 1 \tag{3.6}$$

Substitute (3.6) to (3.5), the voltage stress across the switches is

$$V_{stress} = V_{inv} = (2G - 1)\, V_{dc} = \frac{1}{2M - 1} V_{dc} \tag{3.7}$$

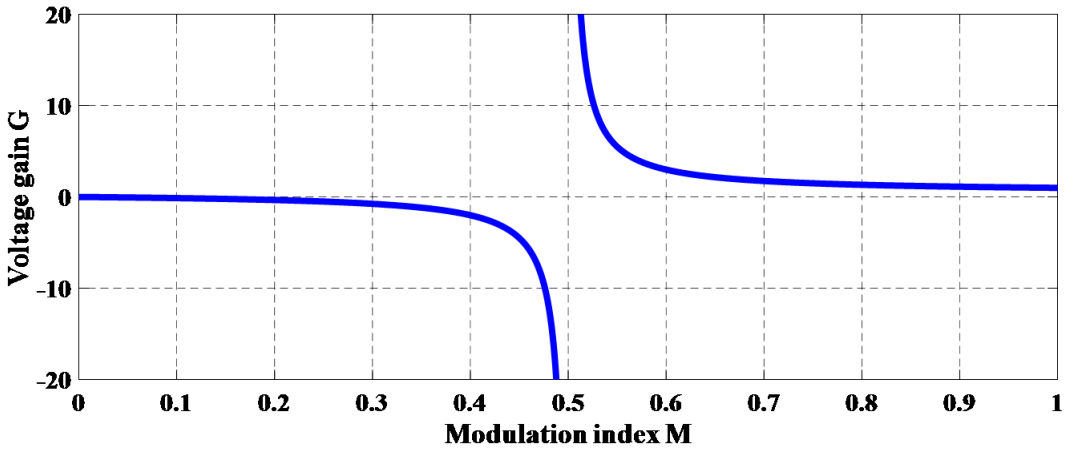


FIGURE 3.2: Voltage Gain of Simple Boost Control.

The curve of voltage gain versus modulation index is shown in Figure 3.2 As can be seen, the voltage gain approaches infinity when M is reduced to 0.5.

3.2.1 Implementation, simulation, and results of three phase ZSI using SBC

The Z-source inverter's operational concept using SBC has been confirmed through simulations. An LC filter is placed between the inverter bridge and the load to clearly indicate the output voltage obtained from the inverter. The following are the simulation parameters:

1. Input Dc voltage: 2x125 V ;
2. Z-source network: Lz of 10 mH , and Cz of 100 µF
3. Output filter LC: L_f of 100 mF and C_f of 1mf;
4. Three-phase RL load: L of 1e-3 mH and R of 40 ?;
5. Switching frequency: 10 kHz.

The overall circuit bloc diagram of the three phase two level inverter is shown in Figure 3.3 below :

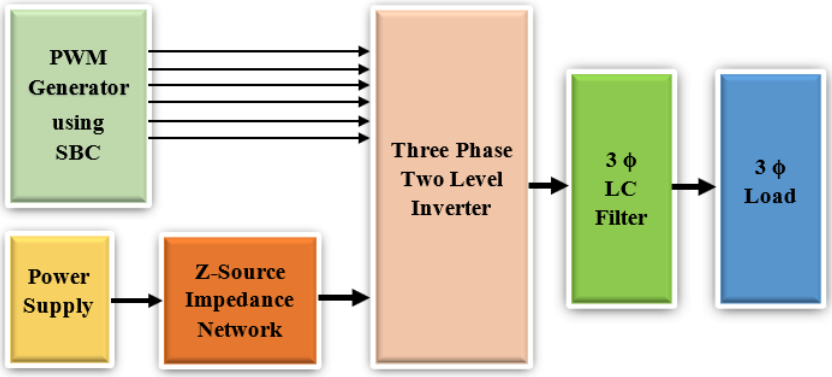


FIGURE 3.3: Bloc diagram of three phase two level inverter using SBC method.

The bloc diagram of PWM generating signals using SBC method is shown in figure 3.4 , this control approach inserts shoot through in all of the PWM typical zero states, during one switching cycle, As with classic carrier-based PWM, the six active states are preserved.

The first is equal to the three-phase sinusoidal reference voltages' peak value m1, while the second is the inverse of the first – m1. The inverter will work in shoot-through mode whenever the triangle carrier signal is greater than the positive straight line or lower than the negative straight line. Otherwise, it works as a standard PWM inverter.

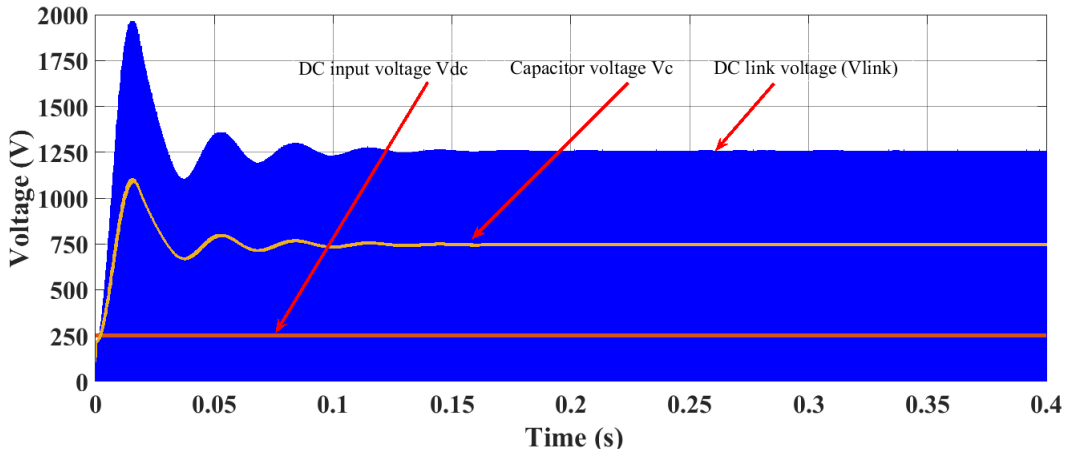


FIGURE 3.5: Simulation SBC. DC-link voltage (V_{link}), Capacitor voltage (V_c) and DC-source voltage (V_{dc}).

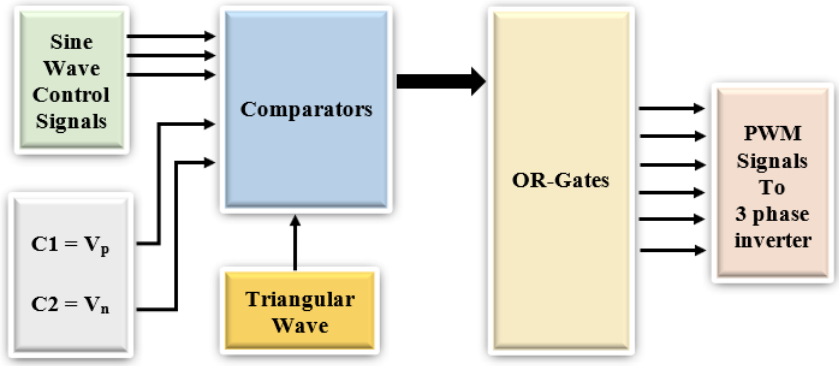
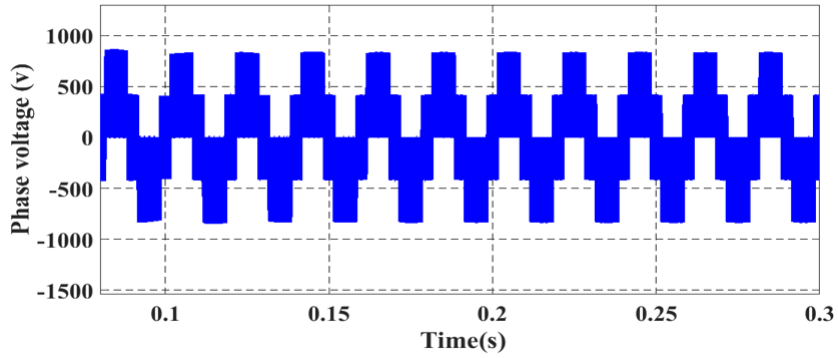


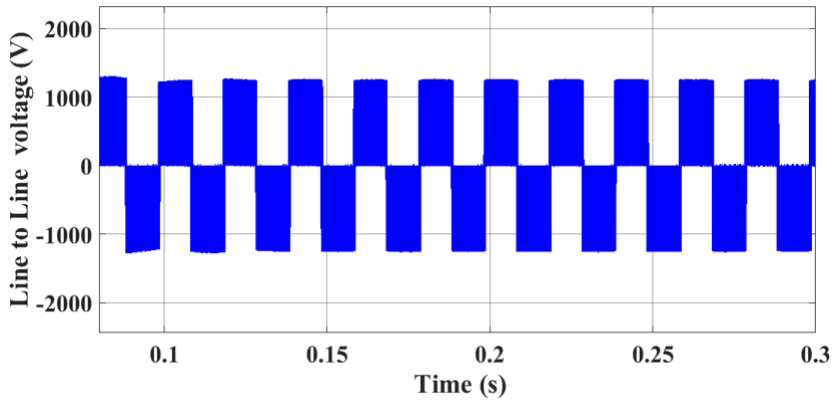
FIGURE 3.4: Bloc diagram of PWM generating signals using SBC method.

Figure 3.5 depicts the inverter's dc link voltage, the ZSI's capacitor voltage, and a comparison with the DC-maximum source's output voltage. The inverter's dc link voltage is increased to (1250V) larger than the DC-maximum source's output voltage (250 V), as seen in the diagram (1000 V).

The switching output line voltage and phases voltage waveforms of ZSI using SBC method are shown in Figure (3.6, a and b). Figure (3.7, a and b) depicts the load output phase voltage and load phase current sine waveforms of ZSI, using the SBC techniques.



(a)



(b)

FIGURE 3.6: Switching output line voltage and phases voltage waveform of ZSI using SBC .(a) Switching output phase voltage; (b) Switching output line voltage.

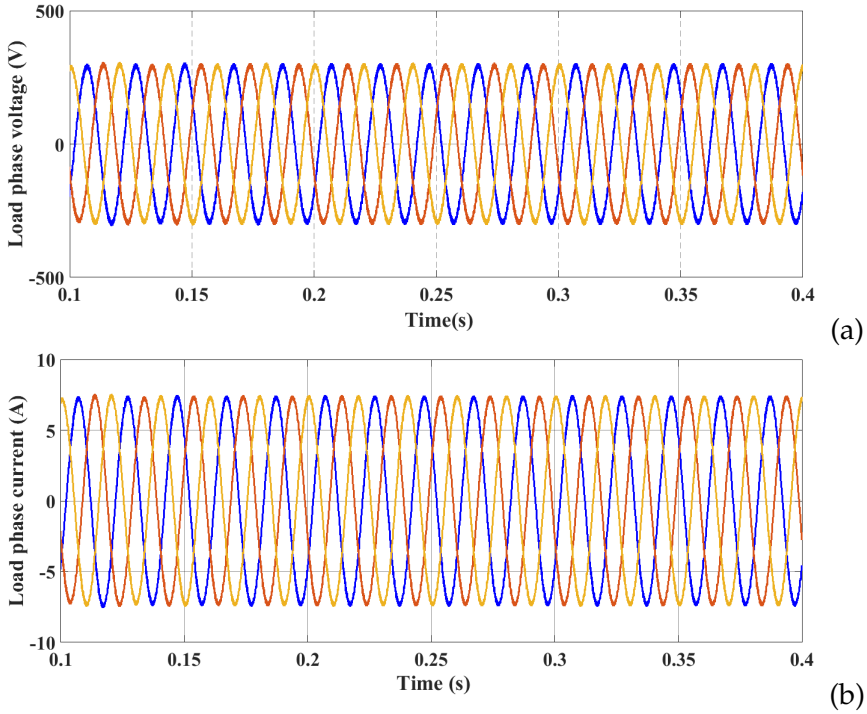


FIGURE 3.7: load output phase voltage and load phase current waveform of ZSI using SBC .(a) load output phase voltage; (b) load phase current.

The first prototype of impedance-source power converter was presented in this section for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc (we have taken only the first one as a case study) power conversion. The Z-source converter uses a special impedance network (or circuit) to connect the main circuit of the converter to the power supply, resulting in unique characteristics not seen in traditional voltage-source and current-source converters. In this case, a capacitor and an inductor are utilized. The Z-source converter overcomes the classic voltage-source and current-source converter's conceptual and theoretical hurdles and restrictions, resulting in a revolutionary power conversion concept. Almost all power conversions can benefit from the Z-source basics.
As a conclusion . Figures (3.7, a and b), depict simulation waveforms at 300 Vac nominal phase voltage and 7.5 A phase current. With a modulation index of m=0.6, the output inverter voltage is a pure sinusoidal voltage which is identical to that of a typical PWM waveform. Which proves the concept of ZSI.

3.3 Maximum Boost Control[3]

Maximum Boost PWM control is an alternative that can overcome the drawbacks faced with the simple boost PWM control, which increases the voltage stress, and limiting the voltage gain due to the limitation of the nominal voltage of the power

device rating. There are two types: maximum boost PWM and maximum boost with third harmonic injection. Figure 3.8 shows the maximum boost control in an open-loop system. It is similar to traditional carrier-based PWM control. The difference is the periodically repeating shoot through state.

In this control strategy, there is no need to use straight lines because only the same signals are used as in the conventional triangular carrier-based PWM. The only difference is that the shoot through occurs during the time when the maximum of the reference voltages of the three phases are all lower than the triangular signal and the minimum of the reference voltages are all higher than the triangular signal as shown in figure 3.8. Otherwise, it operates in traditional PWM mode. With this control strategy, the duty cycle of the boost varies with each cycle. On the other hand, it is clear that the shooting time is variable, which is not the same as in the simple boost control strategy [2]. The relationship between the modulation index M and the average duty ratio of the shoot-through D can be obtained In the interval $\left(\frac{\pi}{6}, \frac{\pi}{2}\right)$, as follows[4]:

$$D_0 = \frac{\overline{T_0}}{T} = \int_{\pi/6}^{\pi/2} \frac{(2 - M\sin\theta) - M\sin(\theta - 2\pi/3)}{2} d\theta = \frac{2\pi - 3\sqrt{3\pi}}{2\pi} \tag{3.8}$$

From equation (3.2) and (3.8),

$$B = \frac{1}{1 - 2D_0} = \frac{\pi}{3\sqrt{3}\,M - \pi} \tag{3.9}$$

The inverter voltage gain (G) is obtained as

$$G = BM = \frac{\pi}{3\sqrt{3}\,M - \pi}\,M = \frac{\pi M}{3\sqrt{3}\,M - \pi} \tag{3.10}$$

Also, as with the simple boost control method, the voltage gain can be controlled by adjusting the modulation index.

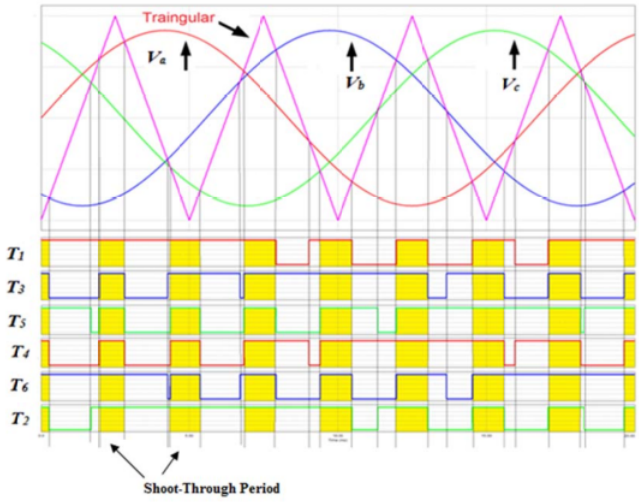


FIGURE 3.8: Sketch Map of Maximum Boost Control.

It is evident that the voltage on the inverter's devices is

$$V_{stress} = BV_{dc} = \frac{\pi}{3\sqrt{3}\,M - \pi} V_{dc} \tag{3.11}$$

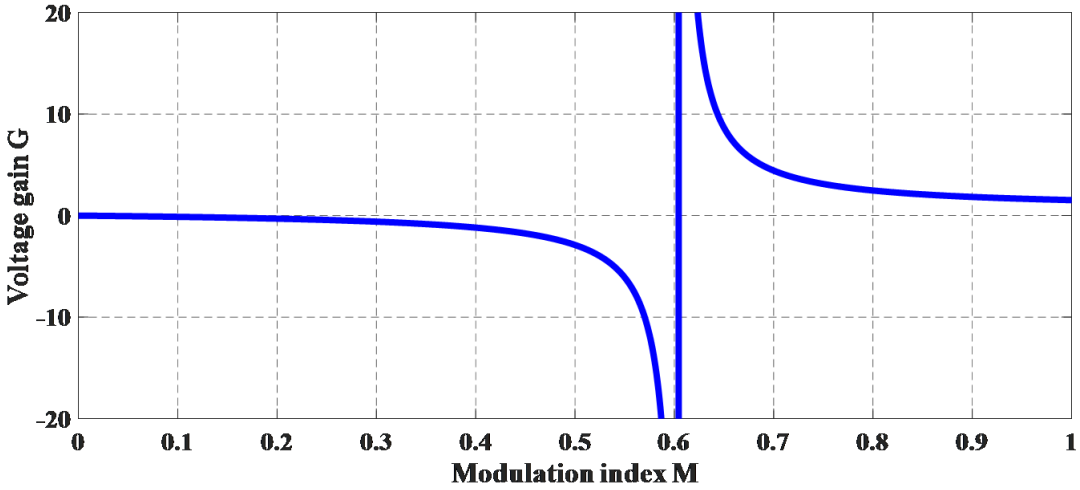


FIGURE 3.9: Voltage Gain of Maximum Boost Control.

The curve of voltage gain versus modulation index is shown in Figure 3.9 As can be seen, the voltage gain approaches infinity when M is reduced to 0.60459

3.3.1 Implementation, simulation, and results of three phase ZSI using MBC

The design of the Z source inverter now revolves around reducing voltage stress while maintaining a specified voltage gain. As previously discussed, the voltage

gain is defined as MB, while the voltage stress across the switches is BV_{dc}. To reduce the voltage stress for any given voltage gain, we should always minimize B and maximize M, with the constraint that their product equals the desired value.
The overall circuit bloc diagram of the three phase two level impedance source inverter (ZSI) using MBC is very similar to the previous one of Figure 3.3 including the simulation parameters, except that the PWM circuit bloc diagram must be changed according to the control mode Figure 3.10.

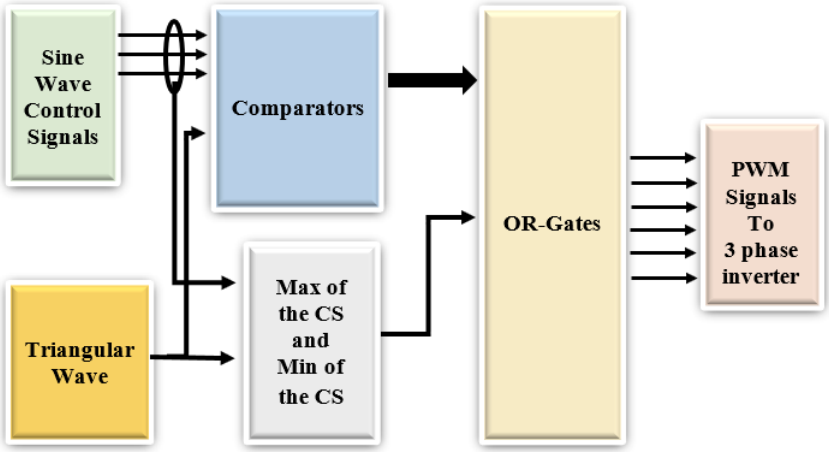


FIGURE 3.10: Bloc diagram of PWM generating signals using MBC method.

Figure 3.11 shows the inverter's dc link voltage, the ZSI's capacitor voltage, and a comparison with the DC-maximum source's output voltage. The inverter's dc link voltage is increased to (1625V) larger than the DC-maximum source's output voltage (250 V), as seen in the figure a difference of (1375 V). With a modulation index of 0.7.

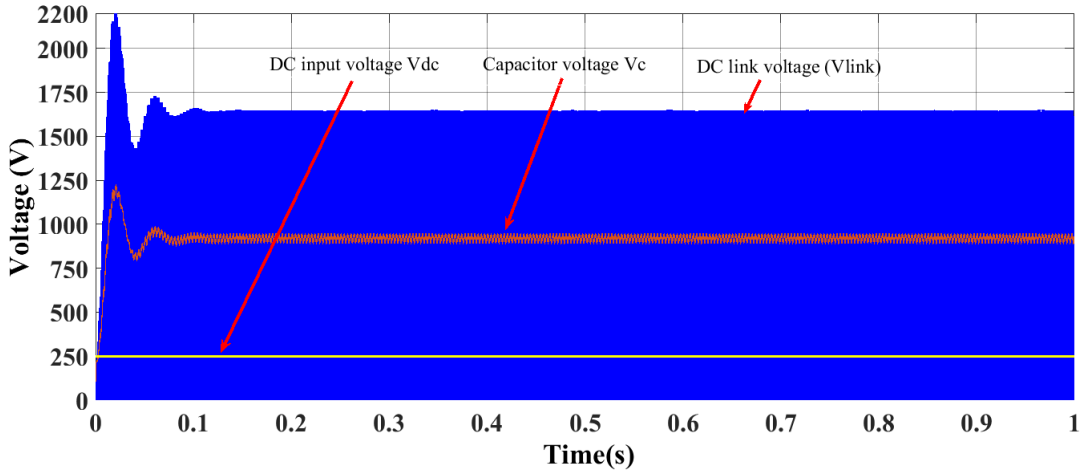
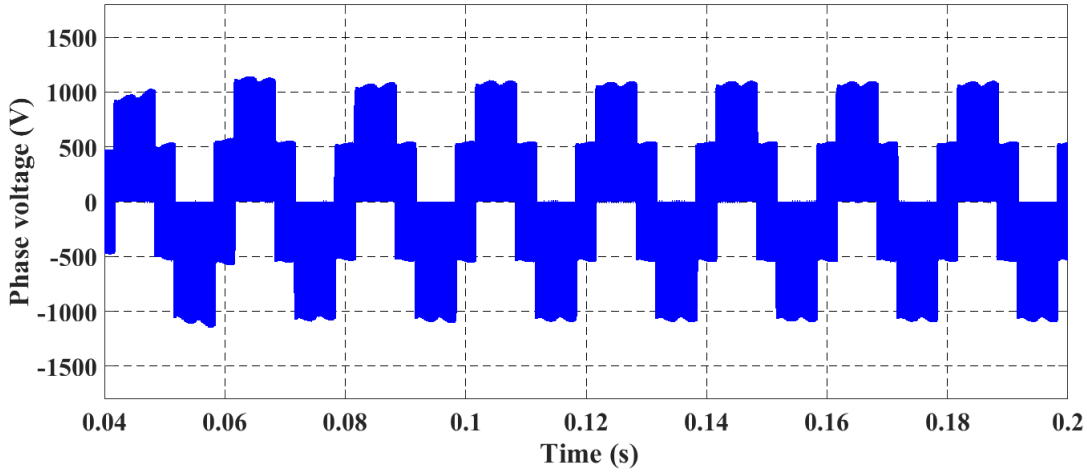
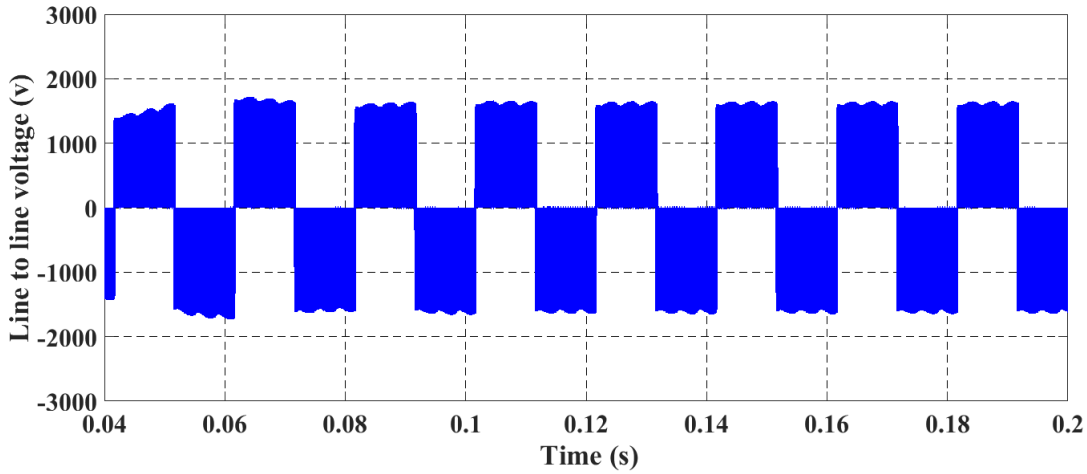


FIGURE 3.11: Simulation MBC. DC-link voltage (V_{link}), Capacitor voltage (V_c) and DC-source voltage (V_{dc}).

The switching output line voltage and phases voltage waveforms of ZSI using MBC method are shown in Figure (3.12, a and b). Figures (3.13, a and b) depicts the load output phase voltage and load phase current sine waveforms of ZSI, using the MBC techniques.

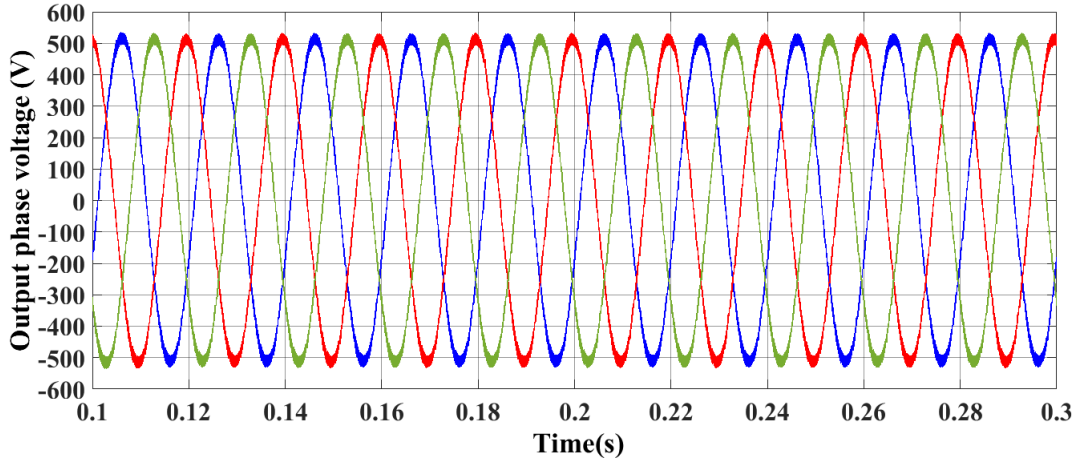


(a)

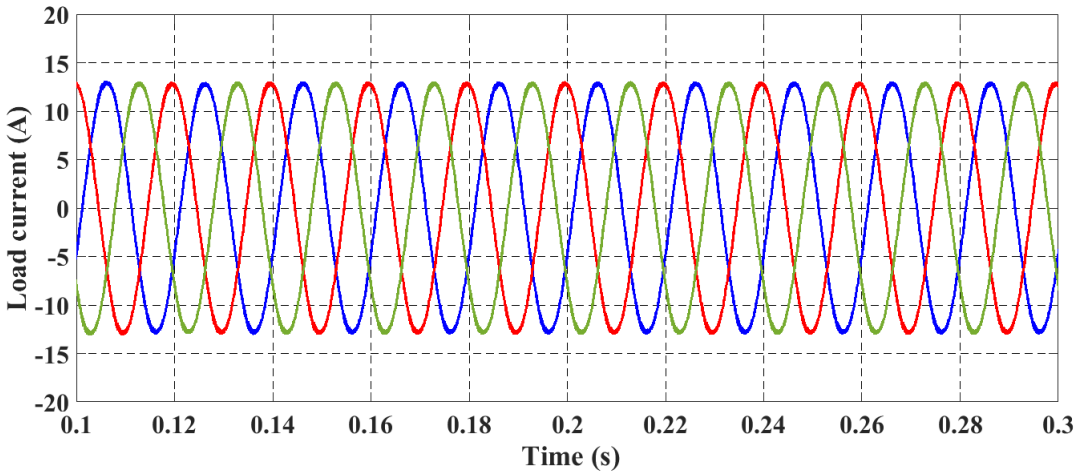


(b)

FIGURE 3.12: Switching output line voltage and phase voltage waveform of ZSI using MBC .(a) Switching output phase voltage; (b) Switching output line voltage.



(a)



(b)

FIGURE 3.13: load output phase voltage and load phase current waveform of ZSI using MBC .(a) load output phase voltage; (b) load phase current.

The main drawback of SBC is that it causes a considerable voltage stress across power devices because certain zero-state states remain unused. To overcome this limitation the maximum boost control behaves similarly as carrier-based PWM control. The distinction is that the shoot-through state occurs periodically every ($\pi/3$) which is introduced to achieve the maximum voltage boost (or voltage gain) and lowering the voltage stress, under a given modulation index. In this case figures (3.13, a and b), depict simulation waveforms at 500 Vac nominal phase voltage and 12.5 Amps phase current. With a modulation index of m=0.7, the output inverter voltage is a pure sinusoidal voltage which is identical to that of a typical PWM waveform.

3.4 Maximum Constant Boost Control

Based to the advantages and disadvantages being encountered in the simple boost control and the maximum boost control, the maximum constant boost control is proposed to benefit from the advantages of both control methods, thus the duty ratio of the shoot through should be constant to reduce the capacitor and inductance tank size of the Z-Source inverter.
Among these disadvantages of the maximum boost control is that it produces a low frequency current ripple associated with the output frequency on the inductor current and capacitor voltage. Therefore, the requirement of passive components will increase. Consequently, the researchers are investigating how to reduce the volume and cost of the z-source network with the goal of eliminating the low frequency current ripple.
In [5] Miaosen S. et al. Proposed a maximum constant boost control method for the Z-source inverter, which can achieve maximum voltage gain at any given modulation index without producing low-frequency ripple related to the output frequency. Thus, the specification of the Z-source network will be independent of the output frequency and determined solely by the switching frequency.
It is important always to maintain the shoot-through duty ratio constant. At the same time, it is desirable to increase the voltage boost for a given modulation index in order to reduce the voltage stress across the power switches, and hence reducing the volume and cost.
In this control method Figure 3.14, there are five modulation curves: three reference signals, V_1, V_2, and V_3, and two shoot-through envelope signals, V_p and V_n. When the triangular signal of the carrier is greater than the upper envelope V_P or less than the lower envelope Vn, the inverter is set to a shoot-through zero state. In between, the inverter switches act in the same way as in a traditional carrier-based PWM control. Since the boost factor is determined by the shoot-through duty cycle, as expressed in [3], the shoot-through duty cycle must be remain the same in order to maintain a constant boost. The basic idea is to obtain the maximum of B while keeping it constant all the time. Hence, the low frequency ripple that appeared in Maximum Boost technique can be eliminated.

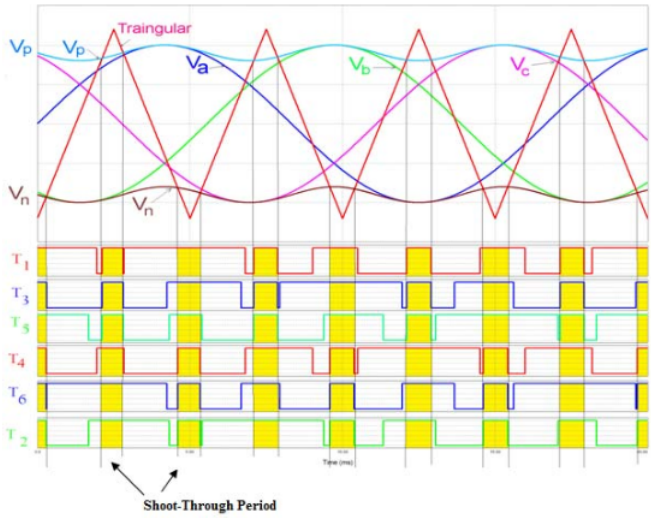


FIGURE 3.14: Sketch Map of Maximum Constant Boost Control.

The upper and lower envelope curves are periodic and correspond to three times the output frequency. There are two half-periods for both curves in a cycle. Therefore, the upper and lower envelopes curves can be expressed as follows:

The upper and lower envelopes V_p and V_n for the two periods can be expressed as:

$$v_p = \begin{cases} \sqrt{3}\,M + M\sin\left(\theta - \frac{2\pi}{3}\right) & 0 \leq \theta \leq \frac{\pi}{3} \\ M\sin\left(\theta\right) & \frac{\pi}{3} \leq \theta \leq \frac{2\pi}{3} \end{cases} \tag{3.12}$$

$$v_n = \begin{cases} M\sin\left(\theta - \frac{2\pi}{3}\right) & 0 \leq \theta \leq \frac{\pi}{3} \\ M\sin\left(\theta\right) - \sqrt{3}\,M & \frac{\pi}{3} \leq \theta \leq \frac{2\pi}{3} \end{cases} \tag{3.13}$$

According to equation (3.12) and (3.13) we can deduce that the distance $V_p - V_n$ between the two curves determines the value of the duty cycle shoot-through D; it depends therefore only on the value of the modulation index and it can be expressed as follows:

$$\frac{T_0}{T} = \frac{2 - \sqrt{3}\,M}{2} = 1 - \frac{\sqrt{3}\,M}{2} \tag{3.14}$$

Therefore, the related paramters as the boost factor B and the voltage gain can be calculated as follows:

$$B = \frac{1}{1 - 2\frac{T_0}{T}} = \frac{1}{\sqrt{3}\,M - 1} \tag{3.15}$$

$$G = \frac{\hat{v}_0}{V_{dc}/2} = MB = \frac{M}{\sqrt{3}\,M - 1} \tag{3.16}$$

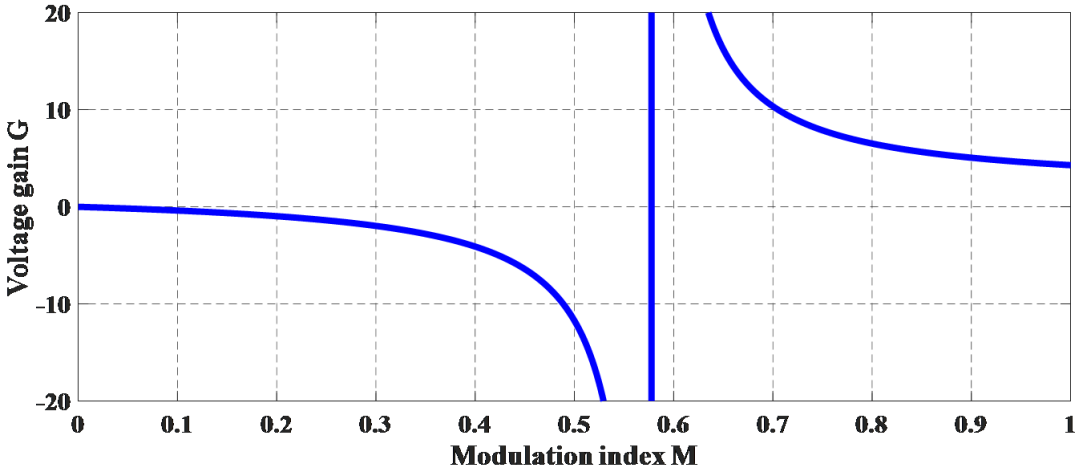


FIGURE 3.15: Voltage Gain of Maximum Constant Boost Control.

The curve of voltage gain versus modulation index is shown in Figure 3.15. As can be seen, the voltage gain approaches infinity when M is reduced to 0.5773

Figure 3.16 shows a comparison of voltage gain versus modulation index for the control strategies

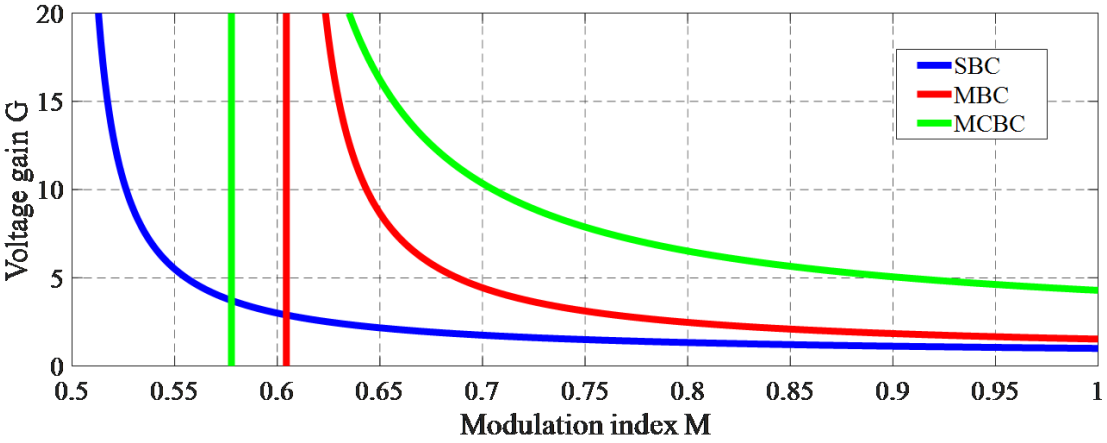


FIGURE 3.16: Comparison of voltage gain versus modulation index.

From equation (3.16) The modulation index can be deduced as:

$$M = \frac{G}{\sqrt{3}\,G - 1} \tag{3.17}$$

The voltage across the devices, Vs or the stress voltage can be calculated as:

$$V_s = BV_{dc} = \left(\sqrt{3}\,G - 1\right) V_{dc} \tag{3.18}$$

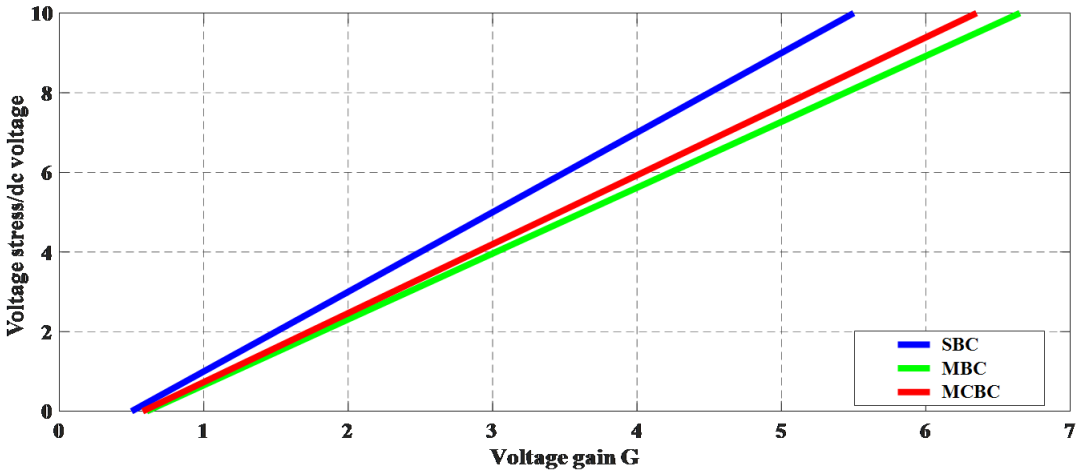


FIGURE 3.17: Comparison of normalized devices voltage stress versus voltage gain.

The voltage stresses across the devices with different control methods are shown in Figure.3.17
As can be seen in Fig. 3.17 the MCBC technique will cause a significantly higher voltage stress across the devices than the maximum control method, but a much lower voltage stress than the simple control method. However, since the MCBC technique removes the line frequency ripple, the passive components in the Z network will be smaller, which will be advantageous in many applications.

3.5 Maximum Constant Boost Control with Third Harmonic Injection [6].

The output voltage using the PWM technique is limited to 0.5 VDC. If the PWM technique is used in motor drive applications, the available voltage may not be enough to operate the motor at the rated condition.
In this situation, the machine must be derated and reduced torque is produced. To improve the output voltage of the PWM inverter using a carrier-based scheme, a third harmonic injection into the modulating signal is performed. It is shown that by adding an appropriate third harmonic component of the modulating signal into the fundamental modulating signal leads to a reduction of the peak of the resultant modulating signal. As a result, the reference value of the resulting modulated signals can be increased above 0.5 VDC, which leads to a higher output voltage at the

inverter. The third harmonic component injected into the modulated signal or reference leg voltages cancels out in the legs and does not appear in the output phase voltages. Thus, the output voltage does not contain unwanted low-order harmonics. The optimal level of third harmonic injection can be determined by considering the modulating signals:[7]

$$\begin{aligned} V_{a_m od} &= V_m \sin(wt) + V_{m3} \sin(3wt) \\ V_{b_m od} &= V_m \sin\left(wt - 2\tfrac{\pi}{3}\right) + V_{m3} \sin(3wt) \\ V_{c_m od} &= V_m \sin\left(wt + 2\tfrac{\pi}{3}\right) + V_{m3} \sin(3wt) \end{aligned} \tag{3.19}$$

For the PWM without harmonic injection, the fundamental peak magnitude of the output voltage is $0.5V_dc$. It is noted that the third harmonic has no effect on the value of the reference signal when

$wt = (2k+1)\frac{\pi}{2}$, since $\sin\left(3(2k+1)\frac{\pi}{3}\right) = 0$ for all odd k.

Thus the third harmonic is chosen to make the peak magnitude of the reference of equation (3.19) occur where the third harmonic is zero. This ensures the maximum possible value of the fundamental component. The reference voltage reaches a maximum when

$$\frac{dV_{a_m od}}{dwt} = V_m \cos(wt) + 3V_{m3} \cos(3wt) = 0 \tag{3.20}$$

This gives

$$V_{m3} = -\frac{1}{3} V_m \cos\left(\frac{\pi}{3}\right) \quad for \;\; wt = \frac{\pi}{3} \tag{3.21}$$

Therefore the maximum modulation index can be

$|V_{a_m od}| = \left|V_m \sin(wt) - \frac{1}{3} V_m \cos\left(\frac{\pi}{3}\right) \sin(3wt)\right| = 0.5V_{dc}$, This gives

$$V_m = \frac{0.5V_{dc}}{\sin\left(\frac{\pi}{3}\right)} \quad for\; wt = \frac{\pi}{3} \tag{3.22}$$

Thus the output fundamental voltage is increased by 15.47% of the value obtainable using simple PWM by injecting 1/6th third-harmonic originally.

A sketch map of the third harmonic injection control method, with 1/6 of the third harmonic, is shown in Figure 3.18.

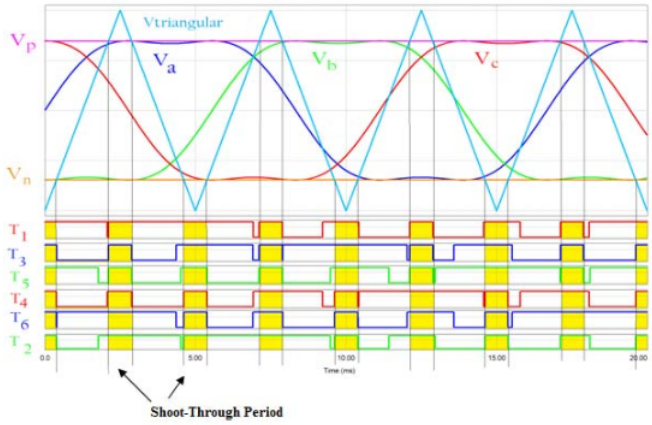


FIGURE 3.18: Sketch Map of Maximum Constant Boost Control with Third Harmonic Injection.

It is clear that; V_a reaches its peak value $\frac{\sqrt{3}\,M}{2}$ while V_b is at its minimum value $-\frac{\sqrt{3}\,M}{2}$ Therefore, a unique feature can be obtained; that is only two straight lines, V_p and V_n are needed to control the shoot-through time with 1/6 (16%) of the third harmonic injected. In this case, the shoot-through duty ratio can be calculated by:

$$M = \frac{2}{\sqrt{3}}(1 - D) \tag{3.23}$$

It can be seen that the resulting duty cycle is identical to the previous duty cycle in the maximum constant control method, so the total voltage gain G can be calculated by the same equation presented in equation(3.16). It is important to note that under the same duty cycle with the maximum constant control method, the modulation index M can be increased to $\frac{2}{\sqrt{3}}$. From equation (3.11), it can be concluded that to obtain the same value of G with the increase of M, the voltage stress will be decreased.[8].

3.6 Implementation, simulation, and results of three phase ZSI using MCBC

Maintaining a consistent shoot-through duty ratio is critical for reducing volume and cost. In order to decrease voltage stress across the switches, a higher voltage boost for any given modulation index is needed.
To maintain a constant boost, the shoot-through duty cycle must be kept constant. The main goal is to achieve the maximum possible boost factor B while maintaining it constant at all times. The upper and lower envelope curves are three times the output frequency and are periodical. Both curves have two half-periods in a cycle.
Same thing as before, the overall circuit bloc diagram of the three phase two level

impedance source inverter (ZSI) using MCBC is very similar to the previous ones of figure 3.3 including the simulation parameters, except that the PWM circuit bloc diagram must be changed according to the control mode figure 3.19.

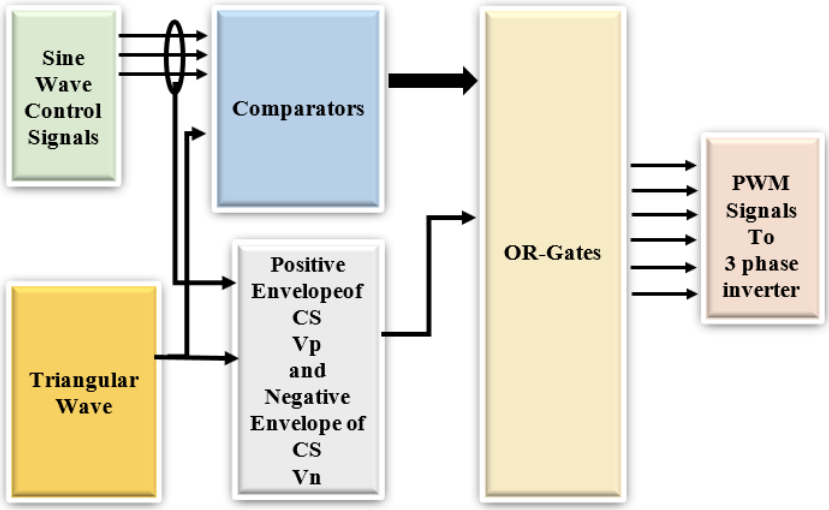


FIGURE 3.19: Bloc diagram of PWM generating signals using MCBC method.

Figure 3.20 shows the inverter's dc link voltage, the ZSI's capacitor voltage, and a comparison with the DC-maximum source's output voltage. The inverter's dc link voltage is increased to (1200V) larger than the DC-maximum source's output voltage (250 V), as seen in the figure a difference of (950 V). With a modulation index of 0.7.

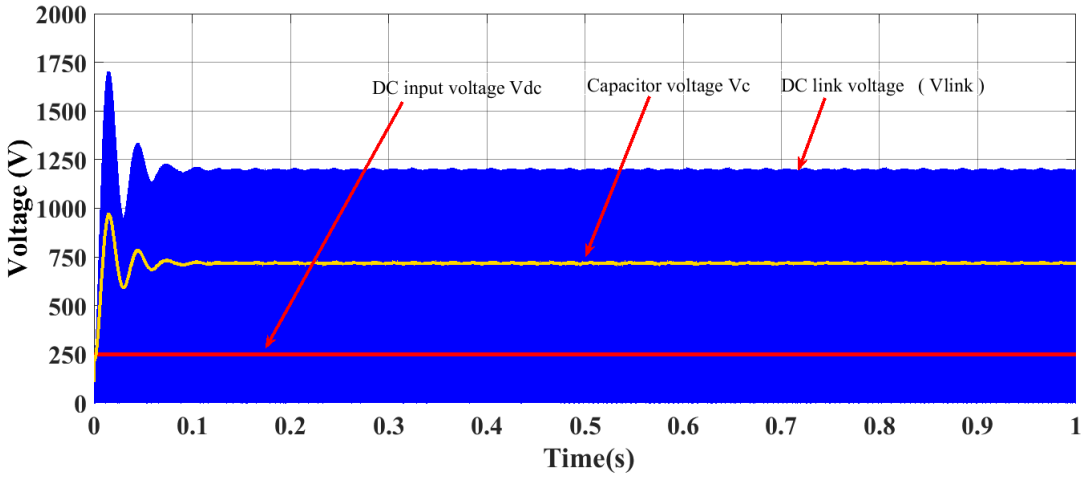


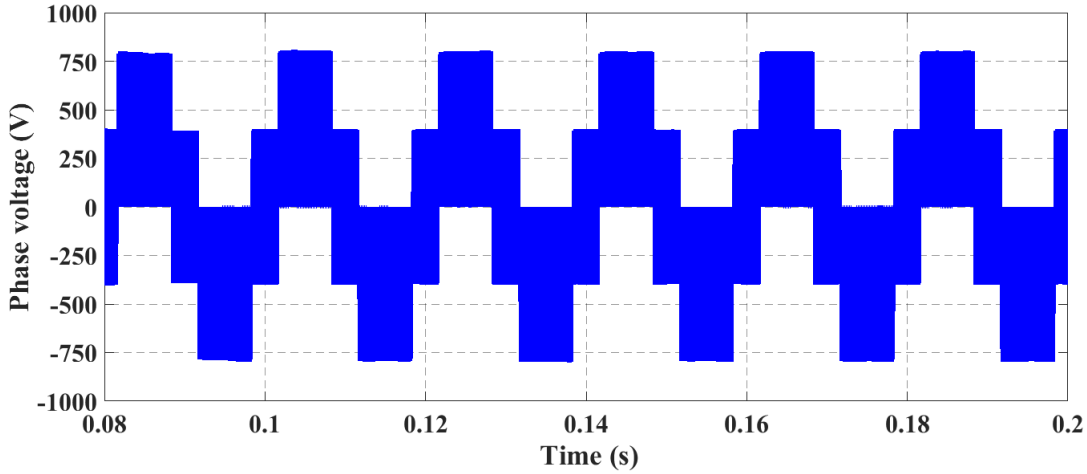
FIGURE 3.20: Simulation MBC. DC-link voltage (V_{link}), Capacitor voltage (V_c) and DC-source voltage (V_{dc}).

The switching output line voltage and phase voltage waveforms of ZSI using MCBC method are shown in Figure 3.21 (a) and (b). Figures 3.22 (a) and (b) depicts

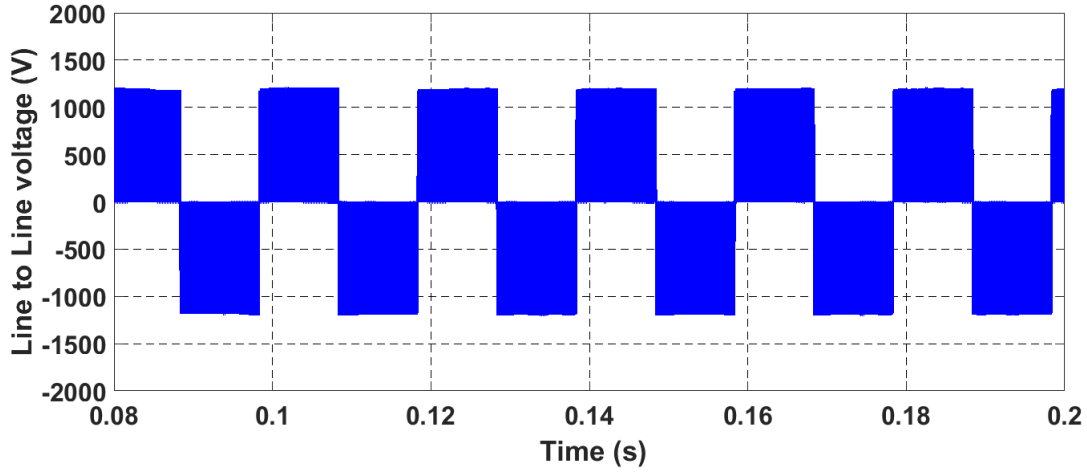
the load output phase voltage and load phase current sine waveforms of ZSI, using the MCBC techniques.

Simulations have been carried out to validate the control approach theory. And proves that the suggested technique can meet the minimal passive component requirement while maintaining low voltage stress.

In this case figures 3.22 (a) and (b), depict simulation waveforms at 400 V_{ac} nominal phase voltage and 9.9 Amps phase current. With a modulation index of m=0.7, the output inverter voltage is a pure sinusoidal voltage which is identical to that of a typical PWM waveform.

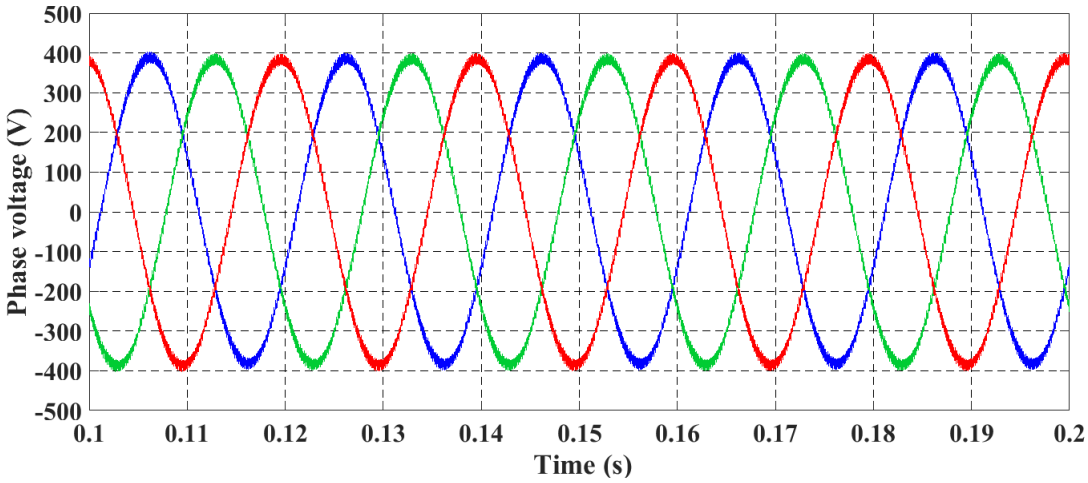


(a)

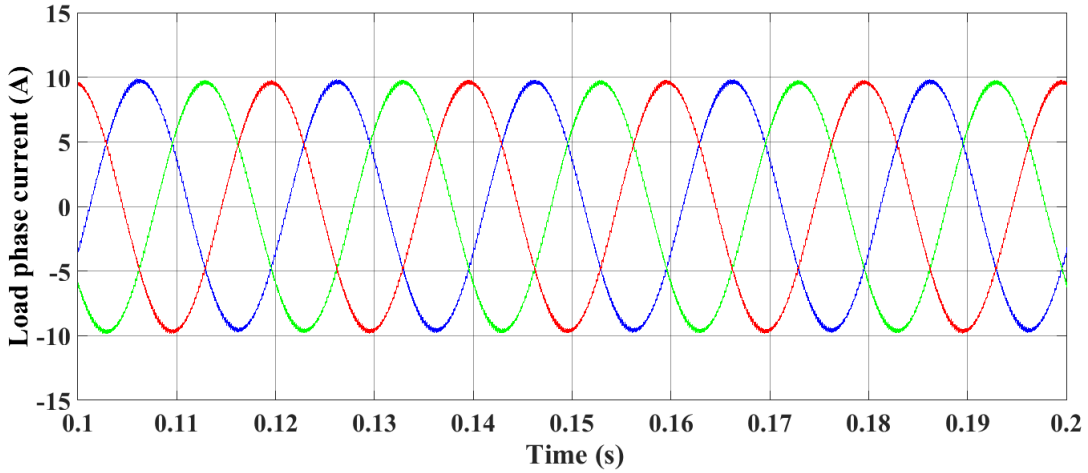


(b)

FIGURE 3.21: Switching output line voltage and phase voltage waveform of ZSI using MCBC .(a) Switching output phase voltage; (b) Switching output line voltage.



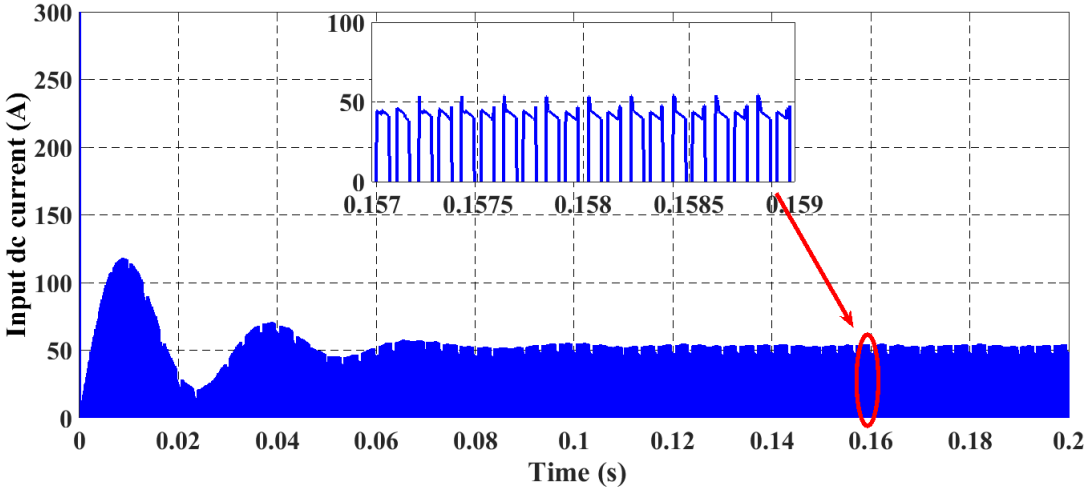
(a)



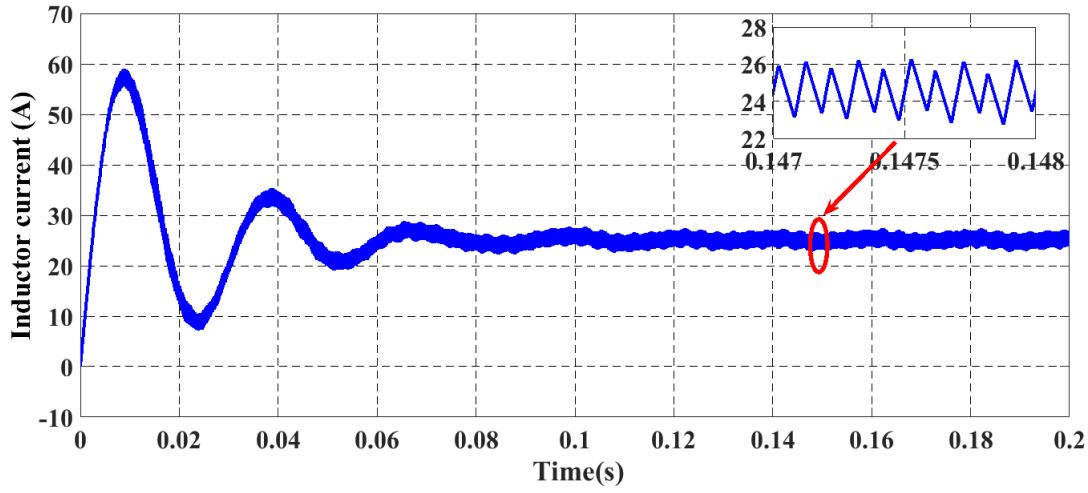
(b)

FIGURE 3.22: load output phase voltage and load phase current waveform of ZSI using MCBC .(a) load output phase voltage; (b) load phase current.

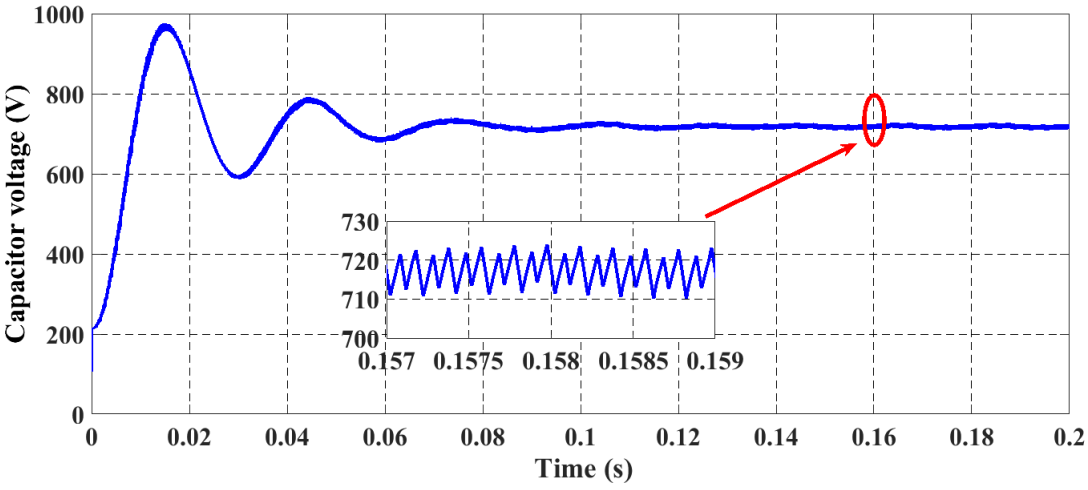
At the same time, figure (3.23 a) shows the input DC current as the current drawn from the DC source, which is discrete, figure (3.23 b) depicts the inductor current, and figure (3.23 c) shows the capacitor voltage.



(a)



(b)



(c)

FIGURE 3.23: Shows input voltage and currents (a) the input DC current, which is discrete,(b) the inductor current, and (c) the capacitor voltage.

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Chapter 4

Analysis of multi-phase qZ-source inverter with Maximum constant boost control technique.

4.1 Introduction

For several years great efforts have been devoted to the study of Z-source inverters to convert DC power to AC power of desired magnitude and frequency, which are characterized by unique features that can overcome the limitations faced in conventional VSI and CSI inverters [1].

This study presents an improvement and a continuation of the previous work of [2]. Indeed, the present work deals with the investigation of two-level multiphase inverter, which means an inverter with a number of phases more than three phases, generally this number is odd such as 5, 7,..., and a novel method of coupling a multiphase AC loads with DC sources via a multiphase Quasi–Zsource inverters. The literature on multiphase inverters shows a variety of control approaches [3-4-5]. The first version of multiphase inverters topology is five-phase VSI powering a star connected five-phase load, as shown in figure 4.1 [6-7].

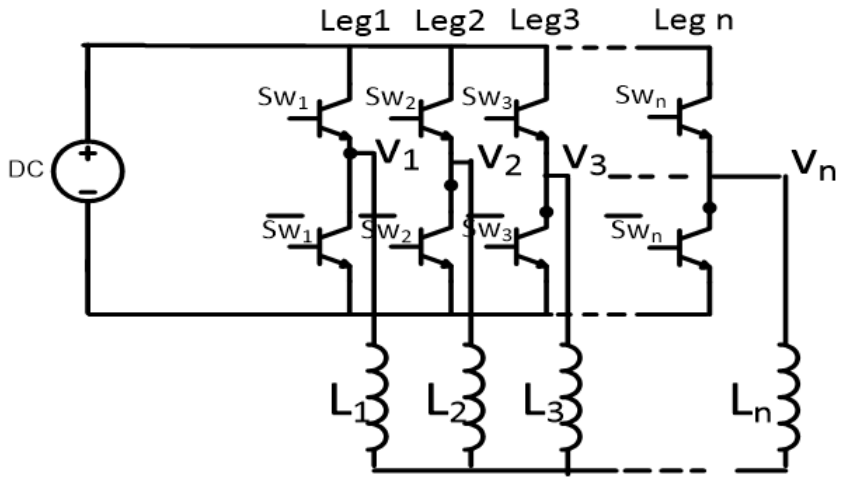


FIGURE 4.1: Multi-phase inverter topology.

Five-phase VSI configuration has found application mainly for driving five phase induction machines (MI) [8], and five phase permanent magnet synchronous machines (PMSM)[9],(the stator consecutive windings are spatially shifted by 72 degree electrical angle) based on several control techniques, which were applied and validated on the three-phase induction machine as well as on the three-phase permanent synchronous machine [10].
The qZ-source inverter (qZSI) due to its unique capability of voltage boost and buck functions in a single or multi-phase topologies[11-12], it has been specially adapted to the different renewable energy source with a wide varying source (DC-link) applications (Fuel Cells (FC), Solar panels, wind power generators, etc.) [13].
As mentioned above, the introduction of a multiphase two level inverter means 2 times N switches are used (N : is the number of phases) , These switches are similar to those used in conventional three-phase inverters, where two conditions must be ensured, bi-directional current flow and unidirectional voltage blocking capability. Indeed, it has been proven that conventional inverters have some disadvantages compared to Z-source inverter topologies, which can be summarized as follows:

- The obtained output voltage in conventional VSI is fairly limited below the input voltage, it means that the VSI inverter behaves as a buck inverter [14].
- No Two switches of the same leg can be gated at the same time to avoid the short
- circuit of the input power supply or the DC link in the input side and the opening under inductive load.
- Intermediate circuits are required, especially to overcome the DC source stability problem.

- Breaking choppers are required for damping the reversed power transferred back to the sources.
- The continuous opening and closing IGBT's produce large dv/dt and di/dt that will generate EMI noise[15].

On the other side the major advantages of the ZSI over conventional VSI can be summarized as follows:

- The ZSI has both Buck and Boost capability.
- Two switches of the same leg can be gated at the same time.
- Both Capacitor and inductor can act for energy storage and smoothing signals.

4.2 Equivalent circuit and operating mode of qZSI

The topology of the qZ-source two-level n-phase inverter is presented in figure 4.2, it is based on the topology of ZSI introduced for the first time by F. Z. peng [1]. As shown in Figure 4.2, the qZ-source network consists of two capacitors (C1, C2), two inductors (L1, L2) and a diode. Similarly to the ZSI, the quasi-Z-source inverter has two operating modes[16].The first one is the "shoot through" mode, during which at least two switches of one leg are on, which is prohibited for a traditional inverter. The other is the non-shoot-through state, in which the inverter operates in the same way as the traditional VSI[7].

For one switching cycle, T, the interval of the shoot through state is $T1$, the interval of the non-shoot through state is $T0$, and the shoot through duty cycle ratio is $D = T0/T$.

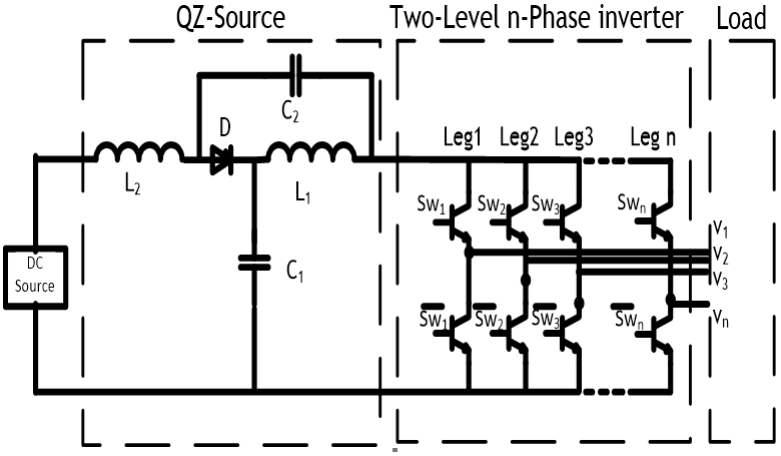


FIGURE 4.2: Multiphase Phase qZSI inverter topology.

4.2.1 Non-shoot-through state

During the interval of non-through state $T1$, the switching scheme of the qZSI is similar to that of a VSI. The inverter bridge, seen from the DC side, is equivalent to a current source. The input DC voltage is available as DC link voltage input to the inverter, making the qZSI behaves like a conventional VSI.

Figure 4.3 shows the equivalent circuit of Z-source inverter viewed from the dc link when the inverter bridge is in the non-shoot-through state.

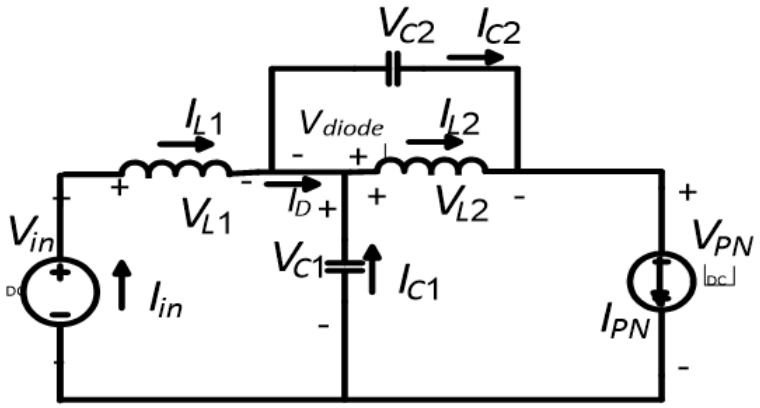


FIGURE 4.3: Equivalent circuit of qZ-source inverter when the inverter operates in the Non shoot-through state.

In this equivalent circuit of qZ-source inverter, the following equations are valid:

$$V_{L1} = V_{in} - V_{C1} \tag{4.1}$$

$$V_{L2} = -V_{C2} \tag{4.2}$$

$$V_{PN} = V_{C1} - V_{L2} == V_{C1} + V_{C2} \tag{4.3}$$

$$V_{DIODE} = 0 \tag{4.4}$$

4.2.2 The shoot-through state

In this case during T0, the switches of the same leg in the inverter bridge are switched on simultaneously for a very short time. The DC source is not bypassed, because of the presence of the LC network that links the DC source and the input of the inverter compared the conventional topology of VSI, while increasing the output voltage. The DC link voltage of the LC network during transient states is increased by a

boost factor, of which depends on the shoot through duty ratio for a given modulation index.
The equivalent circuit of qZ-source inverter, during shoot-through state is shown in figure 4.4

So we have:

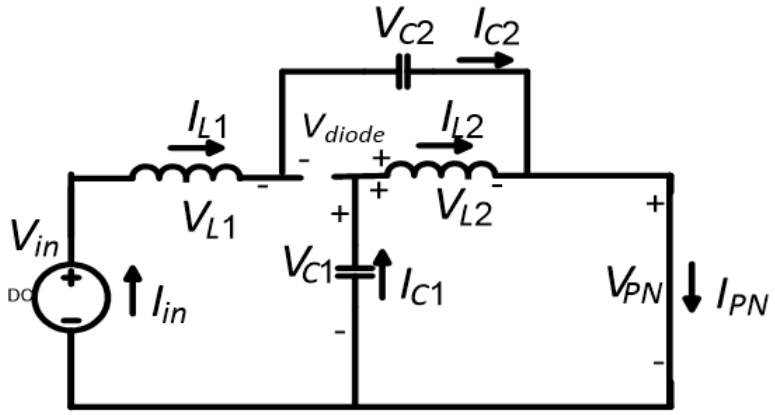


FIGURE 4.4: Equivalent circuit of qZ-source inverter when the inverter operates in the shoot-through state.

$$V_{L1} = V_{in} + V_{C2} \tag{4.5}$$

$$V_{L2} = V_{C1} \tag{4.6}$$

$$V_{PN} = 0 \tag{4.7}$$

$$V_{DIODE} = V_{C1} + V_{C2} \tag{4.8}$$

4.2.3 Circuit analysis

At steady state, the average voltage of inductors over one switching period is zero.Then from equations (4.1) and (4.5), this average voltage across the two inductors of the qZ-source can be rewritten based on the following integrals:

$$\bar{V_{L1}} = \frac{1}{T}\left[\int_0^{T-T_0} (V_{in} - V_{C1})\,dt + \int_{T-T_0}^{T} (V_{in} + V_{C2})\,dt\right] = 0 \tag{4.9}$$

$$\bar{V_{L2}} = \frac{1}{T}\left[\int_0^{T-T_0} (-V_{C2})\,dt + \int_{T-T_0}^{T} (V_{C1})\,dt\right] = 0 \tag{4.10}$$

These equations can be further simplified using the voltages across the capacitors, the input voltage and the periods of times of shoot-through and non-shoot-through periods as follows:

$$\bar{V_{L1}} = \frac{(V_{in} - V_{c1})(T - T_0) + (V_{in} + V_{C2})T_0}{T} = 0 \tag{4.11}$$

$$\bar{V_{L2}} = \frac{(-V_{c2})(T - T_0) + (V_{C1})T_0}{T} = 0 \tag{4.12}$$

Solving (4.4) and (4.5) for V_{C1} and V_{C2} we obtain:

$$V_{C1} = \frac{T - T_0}{T - 2T_0} V_{in} \tag{4.13}$$

And

$$V_{C2} = \frac{T_0}{T - 2T_0} V_{in} \tag{4.14}$$

The peak dc voltage across the inverter bridge can be calculated using equations (4.4), (4.7), (4.11) and (4.12) :

$$V_{PN} = V_{C1} + V_{C2} = \frac{1}{1 - 2\frac{T_0}{T}} V_{in} \tag{4.15}$$

The duty cycle is defined as follows:

$$D = \frac{T_0}{T} \tag{4.16}$$

The ratio between the output voltage of the qZ-source of the inverter V_{PN} and the input voltage V_{in} presents the boost factor, such as :

$$B = \frac{V_{PN}}{V_{in}} \tag{4.17}$$

Based on equations (4.13) and (4.14) the boost factor B can be expressed as:

$$B = \frac{1}{1 - 2D} \tag{4.18}$$

And the output peak phase voltage of the qZ_source inverter $\widehat{V_{ac}}$ can be expressed as:

$$D = \frac{T_0}{T}\widehat{V_{ac}} = M\frac{V_{PN}}{2} = M \bullet B\frac{V_{in}}{2} = G\frac{V_{in}}{2} \tag{4.19}$$

Where M the modulation is index, and G is the voltage gain of the inverter.
The average current across the inductors L1 and L2 can be calculated by the system power rating P.

$$I_{L1} = I_{L2} = I_{in} = \frac{P}{V_{in}} \tag{4.20}$$

By using Kirchhoff's current law, and relation (4.18) the currents in the both capacitors can be calculated as follows:

$$I_{C1} = I_{C2} = I_{PN} - I_{L1} \tag{4.21}$$

And

$$I_D = 2I_{L1} - I_{PN} \tag{4.22}$$

4.3 Maximum constant Boost Control MCBC backgrounds

Since the invention of the famous ZSI inverter introduced by F.Z.Peng[1], many control methods have been proposed especially those based on PWM techniques, basically what is known as, the simple boost control, the maximum boost control, and the maximum constant boost control as seen before.
For the first method SBC control it was the common easiest method to be used. In order to introduce the shoot through states two straight lines envelope are added, which are equal to or greater than the maximum value of the three phase references in traditional PWM [17]. When the carrier triangular signal is more than the upper straight line V_p, or lower than the bottom straight line V_n shoot-through occurs and its duty ratio can be controlled, otherwise the inverter acts in the same way as in conventional carrier based PWM control. This method is very simple, and presents some uncontrollable traditional zero states, resulting in a relatively high voltage stress across the switches.
The main drawback of the simple boost control method consists of the presence of higher voltage stress for higher voltage gain, due to the no use of some traditional zero states. Hence to overcome this issue, the voltage stress must be minimized. In this case the voltage stress across the switches is given by:

$$V_{stress} = B \bullet V_{dc} \tag{4.23}$$

It can be written further as follows:

$$V_{stress} = (2G - 1) \bullet V_{dc} \tag{4.24}$$

From equations (4.17) and (4.22), in order to minimize V_{stress} and at the same time to maintain the gain voltage G relatively high, the boost factor B must be decreased and the modulation index M must be increased.

The second method named maximum boost control MBC was first introduced by [18] to reduce the voltage stress. This means that the control keeps the six active states unchanged and transforms all zero states into shoot-through states. Thus, maximum value of T_0 and Bare obtained for any given modulation index M without distorting the output voltage waveforms [19].

This method introduces a low-frequency current ripple that is associated with the output frequency in the inductor current and capacitor voltage. That results in an increased need for passive components when the output frequency becomes very low. Therefore, maximum boost control is suitable for applications that have a fixed or relatively high output frequency. Moreover this method may require a large DC inductance [20-21].

The third method MCBC control is the most interesting method to the carrier-based PWM control which has been proposed by [22]. This is developed to reduce volume and cost, it is always important to maintain the shoot-through duty ratio constant. At the same time, it is desirable to increase the voltage boost for a given modulation index in order to reduce the voltage stress across the power switches. Table (4.1). Illustrates the three different PWM control method expressions for duty cycle (D), boost factor (B, gain voltage (G), Modulation index (M), and voltage stress (V_s).

TABLE 4.1: Operation of single phase inverter.

	Simple boost	**Maximum boost**	**Maximum constant Boost**
D	$1 - M$	$\frac{2\pi - 3\sqrt{3} \bullet M}{2\pi}$	$\frac{2 - \sqrt{3} \bullet M}{2}$
B	$\frac{1}{2M-1}$	$\frac{\pi}{3\sqrt{3} \bullet M - \pi}$	$\frac{1}{\sqrt{3} \bullet M - 1}$
G	$\frac{M}{2M-1}$	$\frac{\pi M}{3\sqrt{3} \bullet M - \pi}$	$\frac{M}{\sqrt{3} \bullet M - 1}$
M	$\frac{G}{2G-1}$	$\frac{\pi G}{3\sqrt{3} \bullet G - \pi}$	$\frac{G}{\sqrt{3} \bullet G - 1}$
V_s	$(2G - 1) \bullet Vin$	$\frac{3\sqrt{3} \bullet G - \pi}{\pi} Vin$	$\left(\sqrt{3} \bullet G - 1\right) Vin$

4.4 Generalized MCBC control to Multiphase qZ-Source Inverter

As mentioned above, this study is the extension of a previous work presented by Kouzou et al. [2], where we focus to generalize the similar control to Multiphase qZ-Source Inverter using Maximum Constant Boost Control, that means instead of 3-

phase we switch to multiphase (n-phases) qZ-source inverter, this leads to a control method which has $n+2$ modulation curves: n reference signals, V_1, V_2,V_3,... and V_n, and two shoot-through envelope signals, VP and VN (Envelopes of the n reference signals, V_1, V_2, V_3,... and V_n).

When the triangular signal of the carrier is greater than the upper envelope VP or less than the lower envelope VN, the inverter is set to a shoot-through zero state. In between, the inverter switches act in the same way as in a traditional carrier-based PWM control. Since the boost factor is determined by the shoot-through duty cycle, as expressed in [18], the shoot-through duty cycle must be remain the same in order to maintain a constant boost. The basic idea is to obtain the maximum of B while keeping it constant all the time. The upper and lower envelope curves are periodic and correspond to n times the output frequency. There are two half-periods for both curves in a cycle. Therefore, the upper and lower envelops curves can be expressed as follows:

$$V_P = \begin{cases} V_{P1}, & [0 \quad \pi/n] \\ V_{P2}, & [\pi/n 2\pi/n] \end{cases} \tag{4.25}$$

$$V_N = \begin{cases} V_{N1}, & [0 \quad \pi/n] \\ V_{N2}, & [\pi/n 2\pi/n] \end{cases} \tag{4.26}$$

And to determine the expression ofV_{P1},V_{P2} ,V_{N1} and V_{N2} the following parameters are needed :

$$\mu_1 = int\left(\frac{n}{4}\right) + 2 \tag{4.27}$$

$$\mu_2 = int\left(\frac{3n}{4}\right) + 2 = n + 3 - \mu_1 \tag{4.28}$$

$$\delta_1 = sin\left(\frac{1}{4}\left(\frac{2\pi}{n}\right) - (\mu_1 - 1).\frac{2\pi}{n}\right) \tag{4.29}$$

$$\delta_2 = sin\left(\frac{1}{4}\left(\frac{2\pi}{n}\right) - (\mu_2 - 1).\frac{2\pi}{n}\right) \tag{4.30}$$

It is evident that $\forall\ n$($n$the number of phases) the following equivalences are true:
$\delta_1 = -1 \ \Leftrightarrow \delta_2 \neq 1$ and $\delta_2 = 1 \ \Leftrightarrow \delta_1 \neq -1$

$$\forall\ n \delta_1 < 0 \quad and\ \delta_2 > 0$$

Then the shoot-through envelope curves for the first half period can be expressed as follows:

The upper curve is:

$$V_{P1}\begin{cases} M\sin\left(\theta-(\mu_1-1)\frac{2\pi}{n}\right)-2\sin\left(\frac{\pi}{n}-(\mu_1-1)\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\ \delta_1=-1 \\ \\ M\bullet\sin\left(\theta-(\mu_2-1)\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\ \delta_2=1 \end{cases} \tag{4.31}$$

The lower curve is:

$$V_{N1}\begin{cases} M\sin\ \left(\theta-(\mu_1-1)\frac{2\pi}{n}\right), \\ \qquad\qquad if\ \delta_1=-1 \\ \\ M\bullet\sin\left(\theta-(\mu_2-1)\frac{2\pi}{n}\right)-2\sin\left(\frac{\pi}{n}-(\mu_2-1)\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\ \delta_2=1 \end{cases} \tag{4.32}$$

For the second half period the shoot-through curves of the upper envelope and lower envelop can be defined as follows:

The upper curve is:

$$V_{P2}\begin{cases} M\sin\ \left(\theta-(\mu_2-1)\frac{2\pi}{n}\right), \\ \qquad\qquad if\ \delta_1=-1 \\ \\ M\bullet\sin\left(\theta-(\mu_1-1)\frac{2\pi}{n}\right)-2\sin\left(\frac{\pi}{n}-(\mu_1-1)\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\ \delta_2=1 \end{cases} \tag{4.33}$$

The lower curve is:

$$V_{N2}\begin{cases} M\sin\left(\theta-(\mu_2-1)\frac{2\pi}{n}\right)-2\sin\left(\frac{\pi}{n}-(\mu_2-1)\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\ \delta_1=-1 \\ \\ M\bullet\sin\left(\theta-(\mu_1-1)\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\ \delta_2=1 \end{cases} \tag{4.34}$$

From the above equations the difference between the two curves for the same half period is constant, this yields to equation (4.33):

$$V_{P1}-V_{N1}=\begin{cases} -2\sin\left(\frac{\pi}{n}-(\mu_1-1)\frac{2\pi}{n}\right)=-2\sin\left(\frac{3\pi}{n}-\mu_1\frac{2\pi}{n}\right)\ , \\ \qquad\qquad if\delta_1=-1 \\ \\ 2\sin\left(\frac{\pi}{n}-(\mu_2-1)\frac{2\pi}{n}\right)\ =2\sin\left(\frac{3\pi}{n}-\mu_2\frac{2\pi}{n}\right), \\ \qquad\qquad if\delta_2=1 \end{cases} \tag{4.35}$$

And equation (4.34):

$$V_{P1} - V_{N1} = \begin{cases} 2\sin\left(\frac{\pi}{n} - (\mu_2 - 1)\frac{2\pi}{n}\right) = 2\sin\left(\frac{3\pi}{n} - \mu_2\frac{2\pi}{n}\right) \ , \\ if \delta_1 = -1 \\ \\ -2\sin\left(\frac{\pi}{n} - (\mu_1 - 1)\frac{2\pi}{n}\right) = -2\sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right), \\ if \delta_2 = 1 \end{cases} \tag{4.36}$$

Finally, the following equation is obtained:

$$V_{P1} - V_{N1} = V_{P2} - V_{N2} = 2sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right) \tag{4.37}$$

$$= -2sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right)$$

For$\forall\ n = 2k+1 \quad with \quad k \in N^+$
And the values of $\mu_1$and μ_2 are constant for a constant value of$n$, [2].

According to equation (4.35) we can deduce that the distance between the two curves determines the value of the duty cycle shoot-through D; it depends therefore only on the value of the modulation index and it can be expressed as follows:

$$D = \frac{2 + 2\sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right).M}{2}$$

$$= 1 + \sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right).M \tag{4.38}$$

Hence; the boost factor B can be calculated as follows:

$$B = \frac{1}{1-2D} = \frac{-1}{2.\sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right).M + 1} \tag{4.39}$$

From this equation, the modulation index required for any desired output voltage is deduced from the boost factor, which can be calculated as follows:

$$M = -\frac{1+B}{2.\sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right).B} \tag{4.40}$$

The gain of the qZ-source G representing the boost factor describing the capability of this topology in ensuring improved voltage at the input side of the inverter, can be finally expressed as follows:

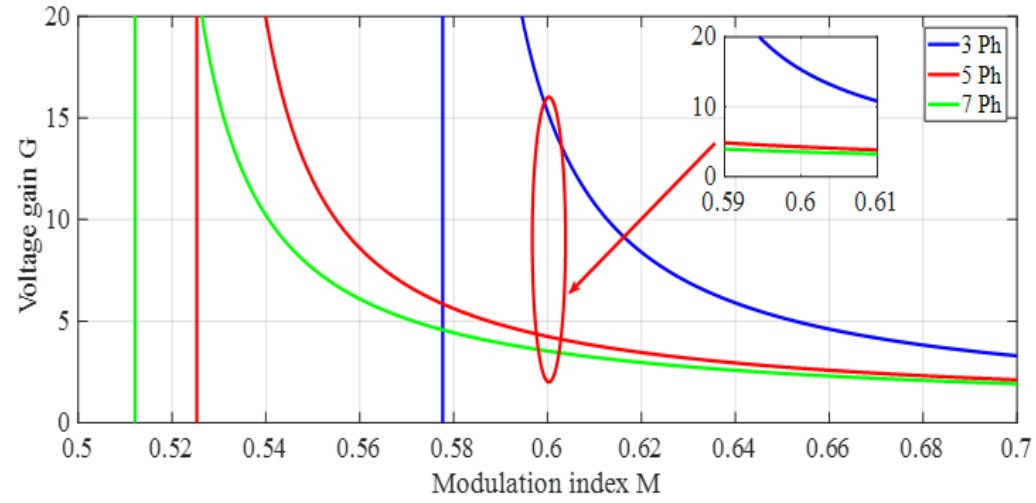
$$G = B.M = -\frac{1+B}{2.\sin\left(\frac{3\pi}{n} - \mu_1\frac{2\pi}{n}\right)} \tag{4.41}$$

TABLE 4.2: Shows Duty cycle, Boost factor and Gain voltage Vs number of phases.

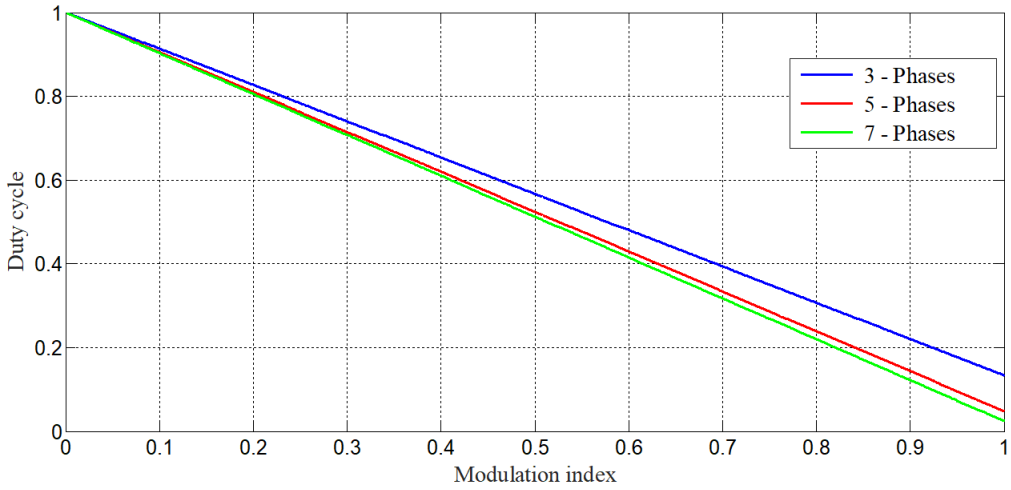
n	D_0	B	G
3	$1-\frac{\sqrt{3}}{2}.M$	$\frac{1}{\sqrt{3}.M-1}$	$\frac{M}{\sqrt{3}.M-1}$
5	$1-\sin\left(\frac{2\pi}{5}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{5}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{5}\right).M-1}$
7	$1-\sin\left(\frac{3\pi}{7}\right).M$	$\frac{1}{2sin\left(\frac{3\pi}{7}\right).M-1}$	$\frac{M}{2sin\left(\frac{3\pi}{7}\right).M-1}$
9	$1-\sin\left(\frac{5\pi}{9}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{9}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{9}\right).M-1}$
11	$1-\sin\left(\frac{5\pi}{11}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{11}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{11}\right).M-1}$
13	$1-\sin\left(\frac{7\pi}{13}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{13}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{13}\right).M-1}$
15	$1-\sin\left(\frac{7\pi}{15}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{15}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{15}\right).M-1}$
17	$1-\sin\left(\frac{9\pi}{17}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{17}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{17}\right).M-1}$
19	$1-\sin\left(\frac{9\pi}{19}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{19}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{19}\right).M-1}$
21	$1-\sin\left(\frac{9\pi}{21}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{21}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{21}\right).M-1}$
23	$1-\sin\left(\frac{9\pi}{23}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{23}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{23}\right).M-1}$
25	$1-\sin\left(\frac{9\pi}{25}\right).M$	$\frac{1}{2sin\left(\frac{2\pi}{25}\right).M-1}$	$\frac{M}{2sin\left(\frac{2\pi}{25}\right).M-1}$

The following table 2 summarizes various parameters of the qZsource inverter for different number of phases based on the above equations:

The gain of the multiphase qZ-source inverter and the duty cycle shoot-through D versus the modulation index are presented in figure 4.5. In (a) It can be seen that the gains start for $0.5 < M < 0.7$, from infinity (reaching a peak value) then they damp toward unity (1) as M tends to unity, this is the same for different number of phases. It depends on the number of phases, for 3-phase and for $M = 0.6$ the gain exceeds 15, 5-phase gain is about 4.5 whereas for 7-phase the gain is 3.5. In (b) the duty cycle shoot-through varies from 1 to near 0 as M varies from 0 to unity.



(a)



(b)

FIGURE 4.5: (a)The gain versus modulation index for MCBCqZ-source 3,5 and 7 phases.(b)The duty cycle shoot-through D versus modulation index for 3, 5 and 7 phases.

Based on the approach presented in [2], the purpose of this paper is to generalize study and analysis of the proposed multiphase qZ-source inverter using the maximum constant control method. To verify the efficiency of this topology, a five-phase inverter was introduced, and to ensure a constant duty cycle, the upper and lower comparison envelope curves should be periodic and their frequency must be three times higher than the output frequency [11]. Therefore, the obtained equations for n phase inverters become for five phase inverter as follows:
The first half period the envelope curves can be obtained as follows:

$$V_{P1} = M\sin\left(\theta - \frac{8\pi}{5}\right) \quad for \;\; 0 < \theta < \frac{\pi}{5} \tag{4.42}$$

$$V_{N1} = M\sin\left(\theta - \frac{8\pi}{5}\right) - 2\sin\left(\frac{\pi}{5} - \frac{8\pi}{5}\right) \; for \; 0 < \theta < \frac{\pi}{5} \tag{4.43}$$

For the second half period the envelope curves are expressed as follows:

$$V_{P1} = M\sin\left(\theta - \frac{8\pi}{5}\right) + 2\sin\left(\frac{\pi}{5} - \frac{8\pi}{5}\right) \quad for \; \frac{\pi}{5} < \theta < \frac{2\pi}{5} \tag{4.44}$$

$$V_{N1} = M\sin\left(\theta - \frac{8\pi}{5}\right) \quad for \; \frac{\pi}{5} < \theta < \frac{8\pi}{5} \tag{4.45}$$

The duty cycle of the shoot-through is:

$$D = 1 - \sin\left(\frac{3\pi}{5}\right).M \tag{4.46}$$

The boost factor is given as:

$$B = \frac{-1}{1 - \sin\left(\frac{3\pi}{5}\right).M} \tag{4.47}$$

Finally the gain is expressed as follows:

$$G = \frac{1 + B}{\sin\left(\frac{3\pi}{5}\right)} \tag{4.48}$$

The control signals map for five phases (n=5), qZsource inverter is presented in figure 4.6, which shows all signals of the maximum constant boost control method, the five reference signals, the two envelope signals, the switching signal of each power switch, and the shoot-through intervals as well.

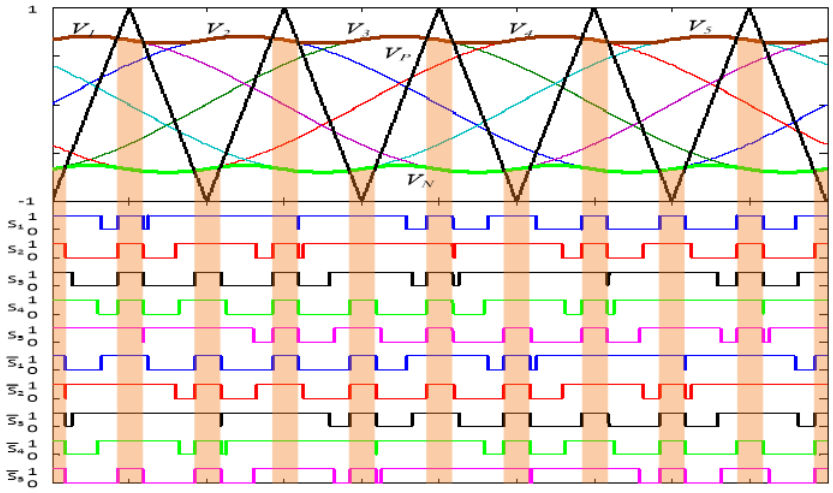


FIGURE 4.6: The Maximum Constant Boost Control signals of a qZ-source five phase inverter.

The following table 3 presents a comparison between different voltages and average currents analysed in section 2, for shoot through and non shoot through states, it

can be noticed that for the qZSI in addition of taking all the benefits of the ZSI, it has low voltage across the capacitor Vc2 and draw smooth current from the input DC supply.
Where:

$$m=\frac{T-T_0}{T-2T_0}$$

$$n=\frac{T_0}{T-2T_0}$$

TABLE 4.3: Shows a comparison between different voltages and average currents qZSI & ZSI[23].

V and Average I		qZSI	ZSI
V_{L1}=V_{L2}	T_0	mV_{in}	mV_{in}
	T_1	-nV_{in}	-nV_{in}
V_{PN}	T_0	*0*	*0*
	T_1	BV_{in}	BV_{in}
V_{diode}	T_0	BV_{in}	BV_{in}
	T_1	*0*	*0*
V_{C1}		mV_{in}	mV_{in}
V_{C2}		nV_{in}	mV_{in}
V_{in}		$M\ B\ V_{in}/2$	$M\ B\ V_{in}/2$
I_{in}=I_{L1}=I_{L2}		P/V_{in}	P/V_{in}
I_{C1}=I_{C2}		I_{PN}-I_{L1}	I_{PN}-I_{L1}
I_D		$2I_{L1}$-I_{PN}	$2I_{L1}$-I_{PN}

4.5 Simulation and results

Simulations have been carried out to validate the main advantages and performances of the multiphase qZSI inverter which is implemented in SIMULINK / MATLAB as a five phase inverter using the Power System block set. The switching signals for the five-phase qZSI two-level inverter are developed using a multi-carrier PWM control, based on MCBC control technique, Figure 4.6.
The presented simulations have been performed using the following parameters: The model consists of an input DC source, qZ-impedance element values are inductances L_1=L_2=10mH, Capacitors C_1=C_2=10uF, two level inverter of 10 power switches IGBT's, output filter of inductance/phase L_f=5mH, and a load of inductance/phase= 1mH with a resistance/phase= 40 ohms. The switching frequency is 10Khz, and the sampling frequency is 1Mhz.

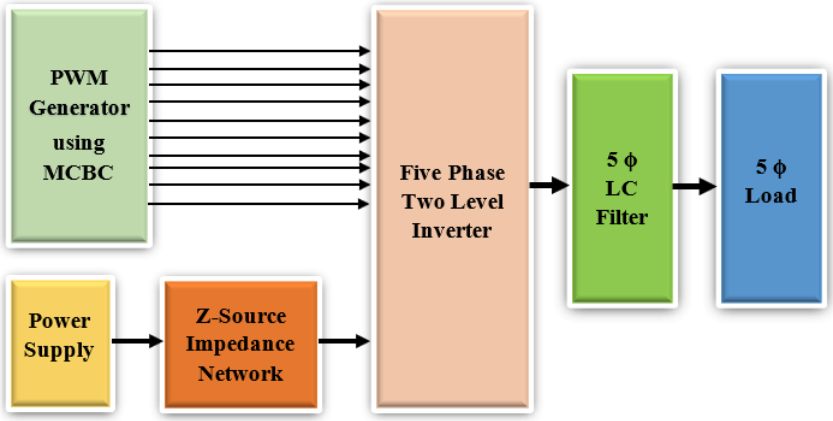


FIGURE 4.7: Bloc diagram of a multiphase qZ-source inverter.

In addition to the previous parameters, the input voltage has been set at $Vin/2$ = 125v, and the modulation index at M=0.63.

The bloc diagram of MATLAB/Simulink model of the multiphase qZ-source inverter using maximum constant boost control is shown in the Figure 4.7.

The qZ-impedance circuit is shown in Figure 4.8 :

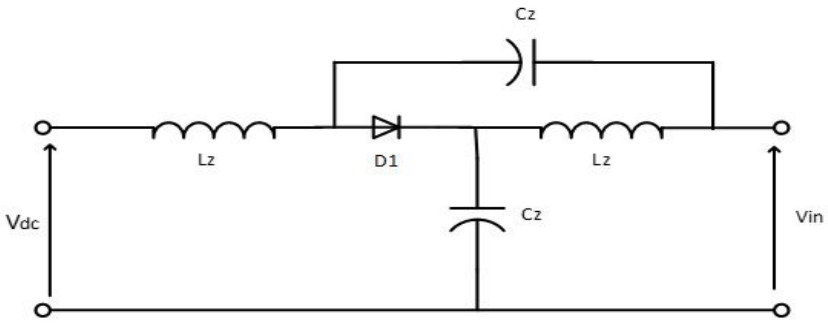


FIGURE 4.8: The Z-impedance circuit of the multiphase qZ-source inverter.

The simulation yields to the main obtained parameters presenting the key stone of the used topology such as the duty cycle D, the Boost factor B, and the overall gain voltage G which are 0.400, 5.04 and 3.176 respectively.

Figure 4.9 shows the current in the input dc supply which is the same as the inductor current. It can be seen clearly, that this currents contains some ripples as shown in the depicted zoom, but they are limited and with less magnitude compared to the classical ZSI, figure 4.10 which was considered as one among the main drawback for ZSI. Furthermore, the advantage of the input current that it presents a continuous current without interruption contrary to the case of the conventional Z-source.

Figure 4.11 shows the output voltage and its corresponding frequency spectrum, It is clear that it contains some remarkable low frequency harmonics, which are suppressed in the load current thanks to the low pass filter behaviour of the load due to the presence of the inductor. While Figure 4.12 presents the load currents and the frequency spectrum of one phase. These results are fully in accordance with the conceptual analysis, and verifies the above analysis as well as the control strategy.

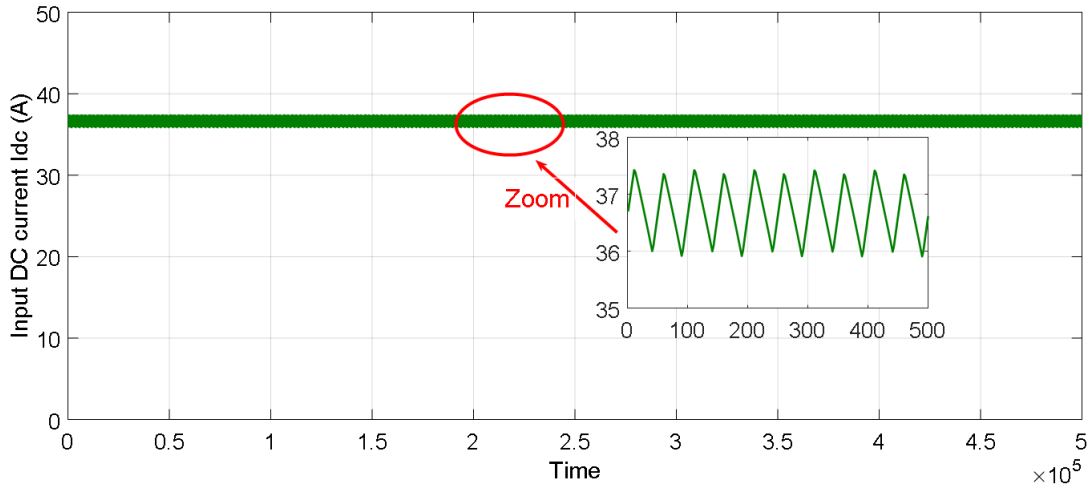


FIGURE 4.9: The input DC current for M=0.63 of a qZ-source five phase inverter.

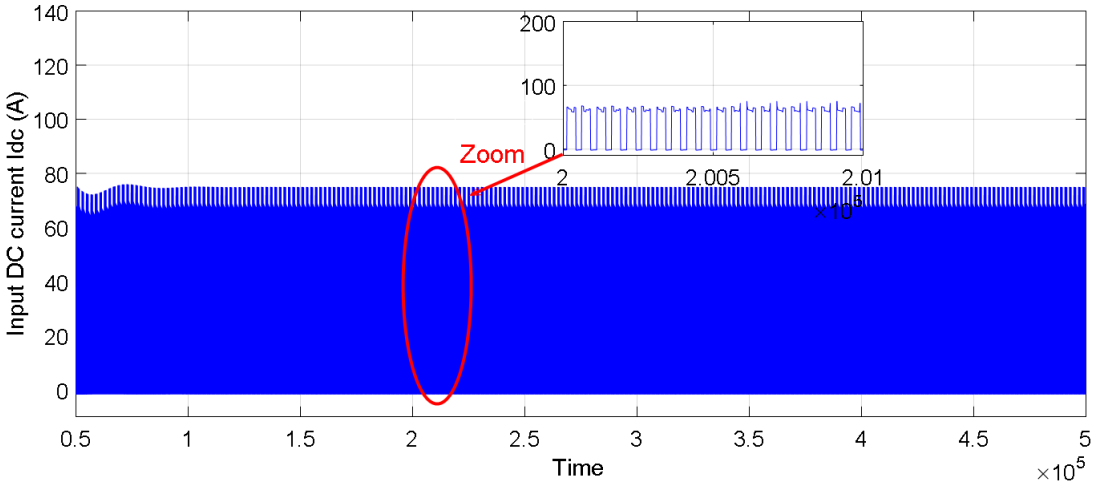
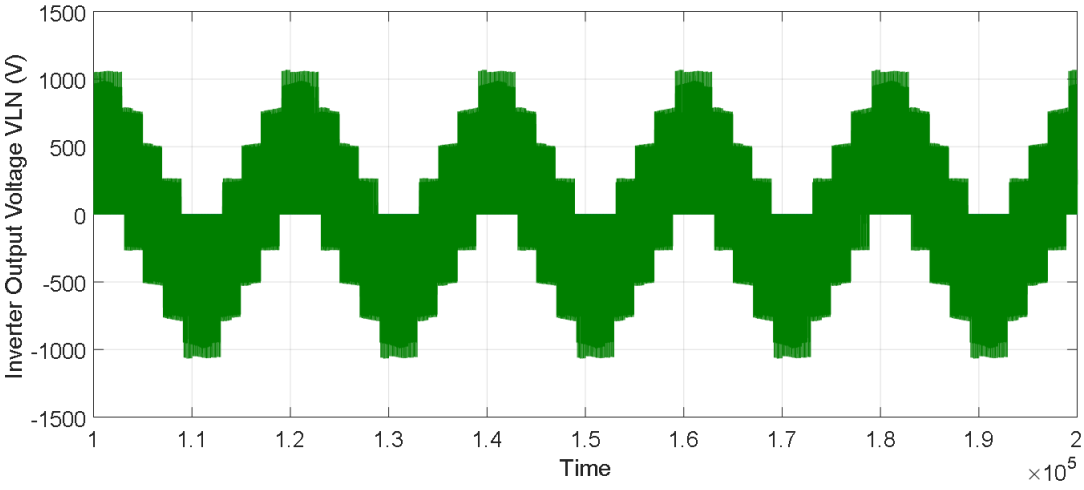
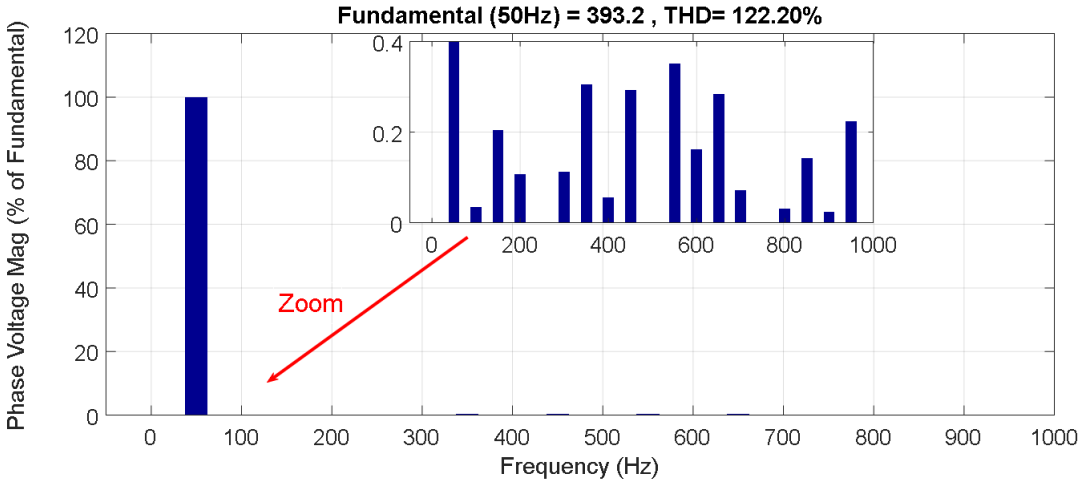


FIGURE 4.10: The input DC current for M=0.63 of a Classical Z-source five phase inverter.



(a)



(b)

FIGURE 4.11: Shows output phase voltage signals and its total harmonic distortion with M=0.63 of the qZ-source five phase inverter.

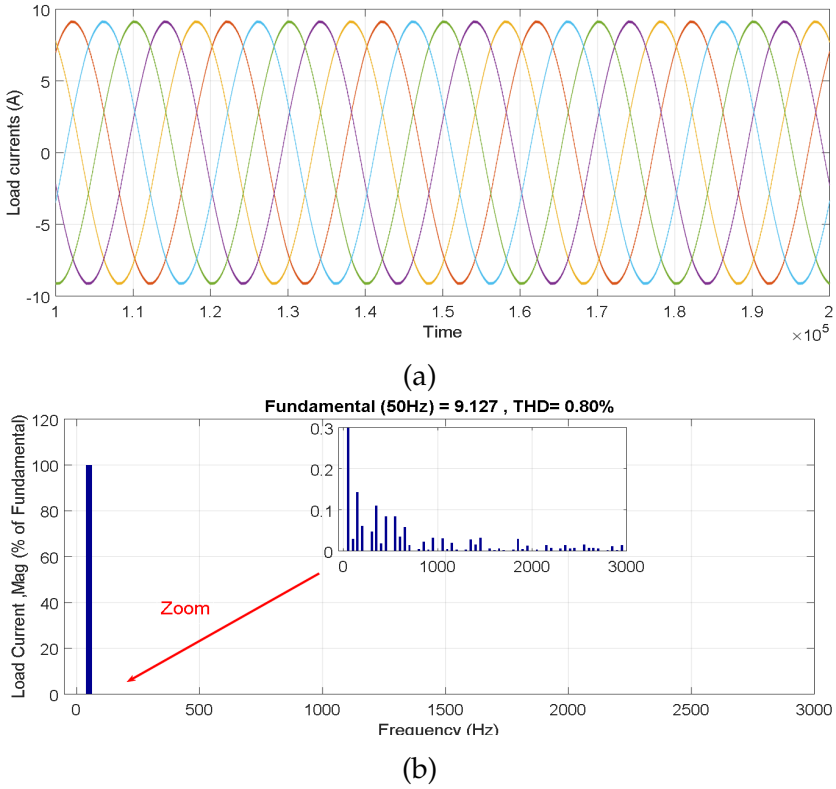


FIGURE 4.12: Shows Load current signals and their total harmonic distortion with M=0.63 of the qZ-source five phase inverter.

4.6 Simulation Results and discussions using a five phase resistive load in parallel with a five phase induction machine.

A qZ-source five-phase inverter simulation was done to check the consistency of the boost factor, the limits of the capacitors voltage stress, and the inductors current ripple in order to test the efficacy of the given qZ-source n-phase inverter.

The two different loads used are, five phase resistive load ($R_L = 40\ \Omega$,$L_L = 0$), and five phase induction machine with varying load torque, the main circuit is shown in Figure. 4.13.
The control technique strategy employed in this simulation may be thought of as an extension of the well-known maximum constant boost control algorithm for Z-source three-phase inverters, where $f_c = 10\ kHz$ and $f_s = 1\ MHz$ are the carrier signal and sampling frequency, respectively.

The modulation index is M=0.63, which leads to the previous parameters of duty cycle shout-through, boost factor, and gain voltage. This is seen to be a significant advantage of the qZ-source five phase inverter over the conventional Z-source five

phase inverter.

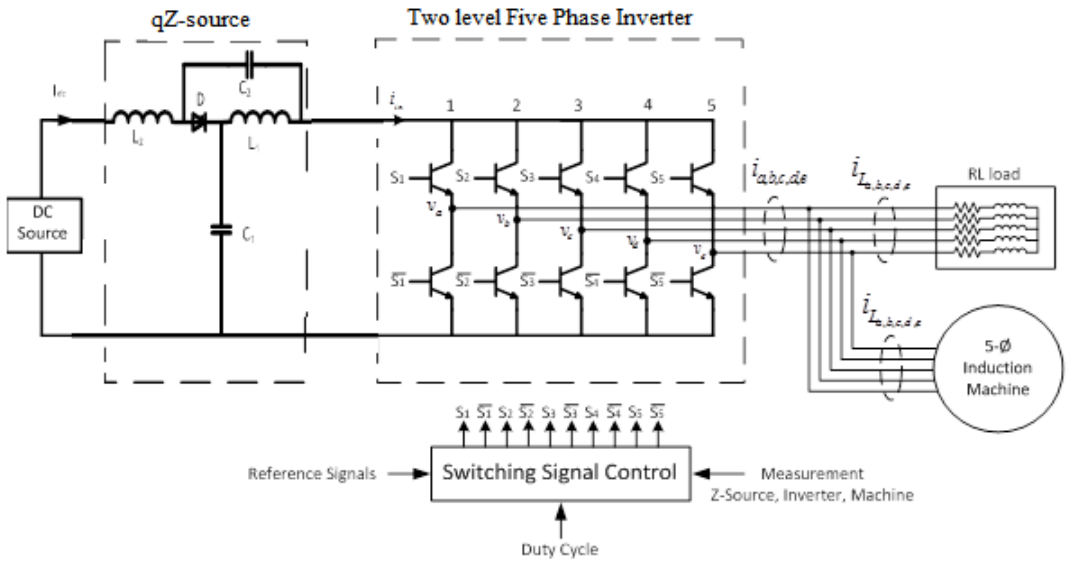


FIGURE 4.13: Circuit diagram of the qZ-source five phase inverter implemented by simulation.

Figure 4.14 depicts the current of the resistive load, which has a $THD = 0.81\%$ and a magnitude of $\widehat{I} = 9.151\ A$. The resistive load is connected in parallel with the five phase induction motor ,and the current absorbed by the motor is illustrated in Figure 4.15.

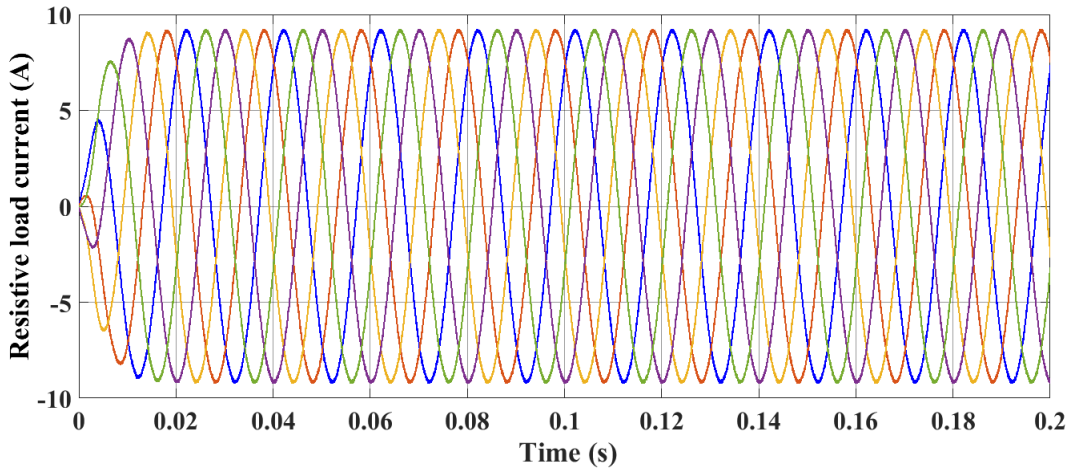


FIGURE 4.14: The current of the resistive load.

Its magnitude at steady state is$\widehat{I} = 2.547\ A$ with a $THD = 0.65\%$, and it is clear that the magnitude of the inrush current is $\approx 13\ A$ when there is no load applied to the motor, which is less relevant when compared to the same five phase machine

with ZSI inverter and the three-phase case.

A resistive torque $T_L \approx 8.33\ Nm$ is applied to the machine at t=0.5 s, enabling a current change to $\widehat{I} = 3.001\ A$ with a $THD = 0.55\%$.

The current absorbed by the five phase induction machine

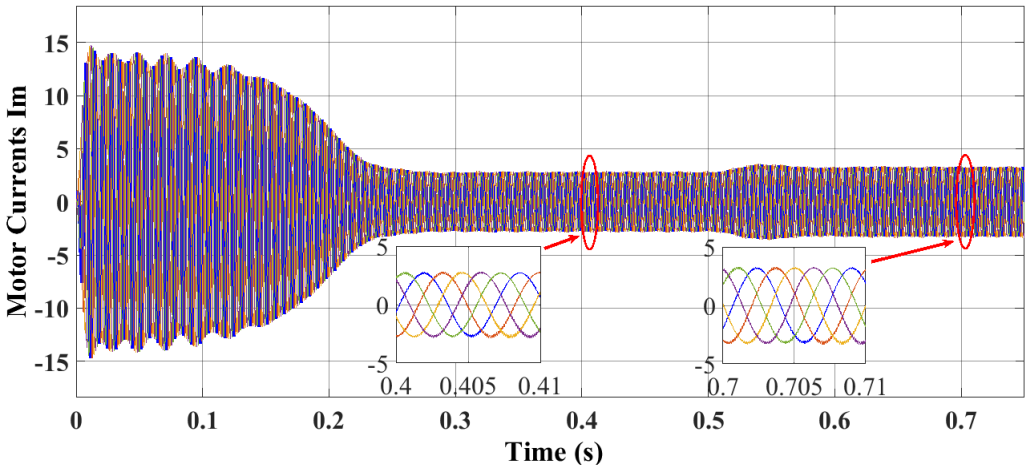


FIGURE 4.15: The current absorbed by the five phase induction machine.

It can be concluded that when the load is increased, the effect of harmonics ripples in the current is decreased, as can be seen in the expanded area of Figure 4.15. The torque and speed produced by the five-phase machine are shown in Figures 4.16 and 4.17 below. It is obvious that they are following the load change appropriately, with a normal machine start-up being ensured; nevertheless, it is clearly noted that the influence of the oscillation in the torque is significantly damped.

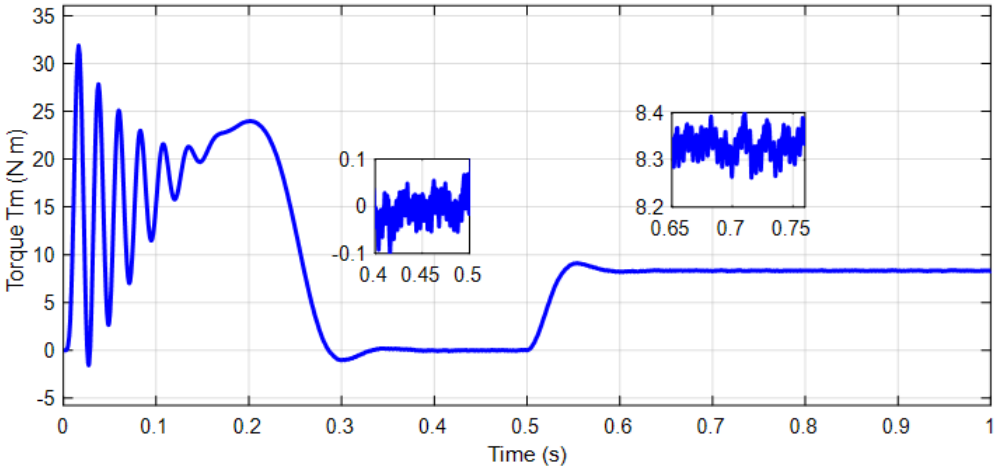


FIGURE 4.16: The torque developed by the phase induction machine.

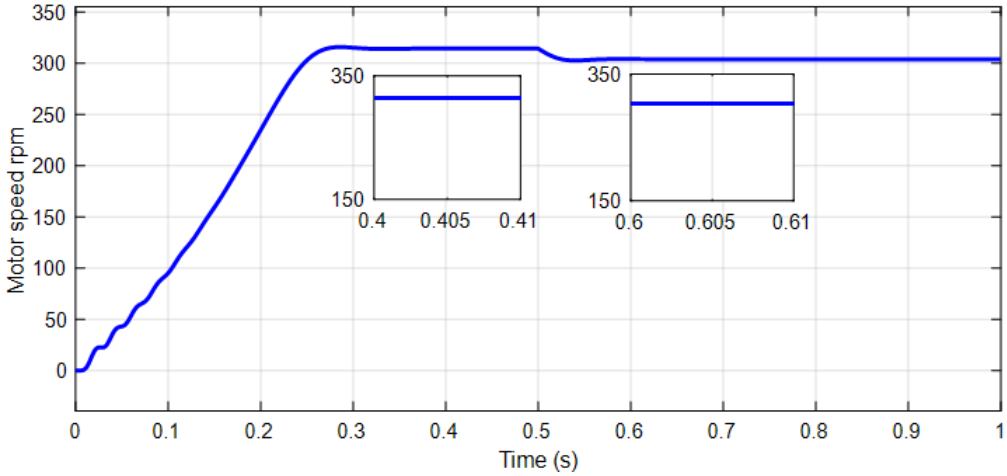


FIGURE 4.17: The speed developed by the five phase induction machine.

It is shown that the ripple current in the qZ-source inductors is unaffected by load current variations Figure 4.18. To clarify, the qZ-current source's inductors are zoomed during one period of the output current in the steady state intervals, low load during [0.3 0.32], high load during [0.7 0.72], and during the transitional phase during the load transitions in the interval [0.49 0.51], where a low ripple current with a constant value of $\Delta I_L = 1.6\ A$ is observed.
In contrast to a traditional, five phase Z source inverter, there is no inrush current during startup. The current increases linearly at first and then achieves a steady state, Figure 4.18. This current is smooth and continuous. Figure 4.19 shows the voltage of the qZ-source capacitors, when this voltage is zoomed in at the same intervals as the inductor's current, it is observed that a continuous stress voltage occurs $\Delta V_C = 80\ V$. Which is unaffected by load current variations, whereas the average values are $V_{C2average} = 500\ V$ and $V_{C1average} = 745\ V$, these voltages are approximately two and three times the DC source voltage, respectively. It can be concluded that this stress is 6.5 times much less than the $V_{C2\_average}$, and 10 times much less than the $V_{C1\_average}$, which can be neglected compared to the average values $V_{Caverage}$ and to the capacitor voltage stress presented in the Z-source five and classical three phase inverters. Another advantage is the reduced and limited peak value of the capacitor voltage at start up which increases also linearly and reaches its peak value at steady state. These results strongly support the use of the qZ-source inverter in multiphase systems, particularly in multiphase machines.
When compared to five phase ZSIs and traditional five and three phase inverters, it offers numerous benefits. On the other hand, the obtained results demonstrate the ease design advantage of the qZ-source impedance to satisfy the need of a wider range of load variation.

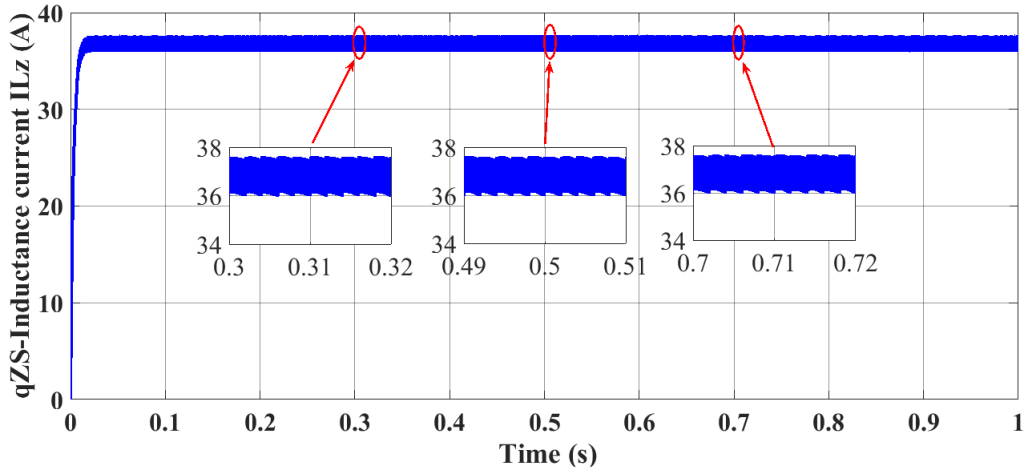


FIGURE 4.18: The inductance current in the qZ-source impedance.

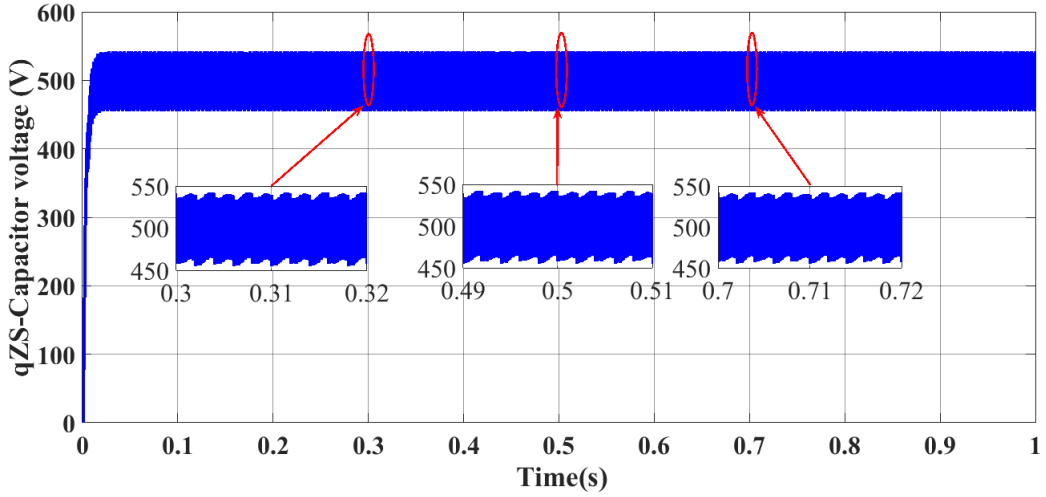


FIGURE 4.19: The Voltage across the capacitor of the qZ-source impedance.

4.7 Conclusion

This work presents the study of the qZ-source inverter topology which is extended to multi-phase inverter/machine. Indeed, it was proved theoretically in this work how the boosting advantage can be achieved for any number of phases while keeping the characteristics of the input current, the output current and the output voltage as desired respectively. In the same time the stresses of the current and voltage on the used switches, the voltage stress across the qZ-source capacitors and the current stress through the inductance of the qZ-source are kept within acceptable levels. It is worthy to mention that it is possible to further improve the efficiency by the use of qZ-source compared to the conventional ZSI, which draws continuous input current from DC input supply, reduces the passive component ratings and lowers voltage

and current stress on capacitors and inductors respectively. It can be said furthermore that the proposed multiphase qZsource inverter is highly insensitive to EMI noise and offers more efficient operation at lower cost.

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General conclusion

The Z-Source family of inverters is a very exciting topology to be functioning as a power conditioning circuit for AC, DC power applications, it can be controlled via PWM control methods for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion.

This impedance source inverter is used to overcome the problems of traditional source inverters. This ZSI inverter uses a unique impedance network coupled with the main inverter circuit to the power source. This inverter has unique features compared to traditional sources.

This thesis presents the study of the qZ-source inverter topology which is extended to multi-phase inverter/machine. Indeed, it was proved theoretically in this study how the boosting advantage can be achieved for any number of phases while keeping the characteristics of the input current, the output current and the output voltage as desired respectively. In the same time the stresses of the current and voltage on the used switches, the voltage stress across the qZ-source capacitors and the current stress through the inductance of the qZ-source are kept within acceptable levels. Thus, the present thesis proposes the topology of two level five-phase qZ-source inverter, where the main aim is to be used for driving the five-phase machine and consequently benefiting from the merits of the advantages of both topologies of the machine and the inverter in building one combined topology. The simulations results obtained using MATLAB/SIMULINK prove the quality of the improved performances of the proposed topology in comparison with previous works which can be a promising solution in many industrial applications based on the aforementioned advantages.

It is worthy to mention that it is possible to further improve the efficiency by the use of qZ-source compared to the conventional ZSI, which draws continuous input current from DC input supply, reduces the passive component ratings and lowers voltage and current stress on capacitors and inductors respectively. It can be said furthermore that the proposed multiphase qZsource inverter is highly insensitive to EMI noise and offers more efficient operation at lower cost.

In addition to the above, Z source topologies can provide the following benefits

- It can produce any desired output ac voltage, even greater than the line voltage.
- Provides ride –through during voltage sags without any additional circuits and energy storage;
- Minimizes the motor ratings to deliver a required power;
- Reduces in-rush and harmonic current.
- Unique drives features include buck-boost inversion by single power-conversion stage, improved reliability, strong EMI immunity, and low EMI
- The Impedance source technology can be applied to the entire spectrum of power conversion.