الجمهورية الجزائرية الديمقراطية الشعبية
People's Democratic Republic of Algeria
وزارة التعليم العالي والبحث العلمي
Ministry of Higher Education and Scientific Research

جامعة زيان عاشور بالجلفة
Ziane Achour University of Djelfa

كلية العلوم و التكنولوجيا
Faculty of Science and Technology

Department: Electrical Engineering

Order N° : . …. / 2026

Defense authorization N° ……/2026

DOCTORAL THESIS

3rd Cycle Doctoral (D-LMD)

Presented by

Kheireddine Moulay

With a view to obtaining the doctoral diploma in 3rd Cycle Doctoral (D-LMD)

Branch: Electronics

Specialty: Embedded systems

Topic

Fault Diagnosis of Modular Multilevel Converter with Contribution to their Fault-Tolerant Controls

Supported, on 02 /15 / 2026, before the jury composed of:

Last and first name	Grade	Institution of affiliation	Designation
Mr Boudiaf MOUHAMED	Professor	University of Djelfa	President
Mr Merzouk IMAD	MCA	University of Djelfa	Supervisor
Mr Hafaifa AHMED	Professor	University of Djelfa	Co-Supervisor
Mr Dif ISMAIL	MCA	University of Djelfa	Examiner
Mr Aissat SIDALI	MCA	University of Djelfa	Examiner
Mr Roubache TOUFIK	Professor	University of M’sila	Examiner

Djelfa University, FST - 2026

Acknowledgment

First and foremost, I express my deepest gratitude to Almighty Allah, who has blessed me with courage, determination, patience, and good health throughout these years. Without His guidance and mercy, the completion of this work would not have been possible.

﴿ وَقُل رَّبِّ زِدْنِي عِلْمًا ﴾

I would like to extend my profound gratitude to my supervisor, ***Dr. Imad Merzouk****, for his continuous guidance, valuable feedback, and constant encouragement during the course of this research. His expertise and unwavering support have been fundamental to the successful completion of this thesis.*

My sincere thanks also go to my Co-supervisor, ***Prof. Ahmed Hafaifa****, for his constructive advice, insightful suggestions, and dedicated supervision, which greatly enriched the quality of this work.*

I am truly honored to express my appreciation to the distinguished members of the jury for accepting to examine and evaluate this thesis. Their expertise, insightful comments, and thoughtful feedback are of great value and represent an immense contribution to the refinement of this research.

I am also deeply grateful to ***Dr. Hegazy Rezk*** *for his valuable assistance and guidance, which have been of great benefit throughout my research journey.*

Finally, I would like to thank my laboratory colleagues for their cooperation, encouragement, and for fostering a friendly and motivating atmosphere that made this journey both productive and enjoyable

Dedication

My deepest love and heartfelt gratitude go to my beloved parents, ***Mohamed*** *and* ***Aicha****, whose sincere prayers, patience, and unwavering moral and material support have been the foundation of my academic journey.*

﴿ وَقُل رَّبِّ ٱرۡحَمۡهُمَا كَمَا رَبَّيَانِي صَغِيرًا ﴾

I also extend my sincere thanks to my dear brothers, ***Redouane*** *and* ***Tahar****, who have always surrounded me with love, encouragement, and constant support at every step of my studies.*

To my beloved fiancée, ***Narimane****, whose love, understanding, and encouragement have been a constant source of strength and motivation. Your patience and support have brightened this journey and made this achievement even more meaningful.*

This work is lovingly dedicated to all of you.

Kheireddine Moulay

الملخص

تُعَدّ المحوّلات متعددة المستويات المعيارية (MMC) من بين أهم التقنيات في أنظمة القدرة الحديثة، وذلك بفضل كفاءتها العالية، ومرونتها، وقابليتها للتوسّع. غير أنّ بنيتها المعقّدة تجعلها عرضةً لأنواع مختلفة من الأعطال، مثل أعطال مفاتيح القدرة وأعطال مكثفات الوحدات الفرعية، الأمر الذي قد يهدّد أداءها ويؤثر سلباً على استقرار النظام.

تهدف هذه الأطروحة إلى تطوير استراتيجيات متقدمة للتشخيص والتحكم المُتحمِّل للأعطال، من أجل تعزيز موثوقية الـ MMC وقدرتها على العمل في ظروف التشغيل الحرجة. في الجزء الأول، تم اقتراح منهج ذكي للكشف عن أعطال الفتح في مفاتيح الـ IGBTوالصمام الثنائي المضادة للتوازي الخاصة بها، وذلك بالاعتماد على الدمج بين المنطق الضبابي وتقنيات معالجة الإشارة من أجل تحسين استخراج الخصائص وضمان دقة التحديد. في الجزء الثاني، تم تقديم مقاربة هجينة للكشف عن أعطال القصر المتعددة داخل الوحدة الفرعية الواحدة، بالاعتماد على الشبكات العصبية ذات الدوال الأساس الشعاعية (RBFNN) مدمجة مع التحويل المويجي المتقطع (DWT) بهدف رفع كفاءة التشخيص. كما تم تطوير تقنية سريعة لمعالجة الإشارة من أجل الكشف المبكر عن أعطال القصر في مفاتيح الـIGBT، مما يساهم في تقليل زمن الاكتشاف واتخاذ إجراءات وقائية في الوقت المناسب. وأخيراً، تم اقتراح إستراتيجية بسيطة للتحكم المُتحمِّل للأعطال لمعالجة أعطال المكثفات، حيث تضمن هذه الإستراتيجية استقرار التشغيل في الوضع المتدهور وتجنّب التوقفات غير الضرورية.

تمت محاكاة جميع الأساليب المقترحة والتحقق من فعاليتها باستخدام بيئة المحاكاة MATLAB/Simulinkعلى نموذج MMCبخمسة مستويات، حيث أظهرت النتائج دقتها وموثوقيتها في تحسين التشخيص وضمان استمرارية التشغيل.

الكلمات المفتاحية ـــالمحوّل متعدد المستويات المعياري (MMC) ، التحكم المتحمّل للأعطال، الشبكات العصبية (RBFNN)، التحويل المويجي المتقطع (DWT) ، المنطق الضبابي، معالجة الإشارة

Abstract

Modular Multilevel Converters (MMCs) are increasingly recognized as a core technology in modern power systems due to their high efficiency, modularity, and scalability. However, their complex structure also makes them susceptible to faults, as switching dispositive failures and the capacitor of submodule malfunctions. These faults pose a significant threat as they directly affect output performance and system stability.

This thesis investigates advanced diagnostic and fault tolerant control strategies to enhance the fault resilience of MMCs. the first part of this work presents an intelligent diagnostic method for

open-circuit faults in IGBTs and their anti-parallel diodes. This method combines fuzzy logic for fault classification with signal-processing techniques to improve feature extraction and ensure accurate localization. The second part introduces a hybrid diagnostic approach for detecting multiple short-circuit faults within a single submodule, using a radial basis function neural network (RBFNN) integrated with discrete wavelet transform (DWT) to enhance robustness. A third aspect is a fast signal-processing technique for IGBT short-circuit detection, which significantly reduces detection latency and enables timely protective actions to prevent converter damage. Finally, a simple fault-tolerant control (FTC) strategy is proposed for capacitor failures. Based on intelligent decision-making and logical operators, this FTC ensures stable operation in degraded mode and avoids unnecessary shutdowns. All proposed methods validated using a five-level MMC benchmark model in MATLAB/Simulink. The simulation studies confirm the effectiveness of the proposed methods in improving diagnostic accuracy and operational reliability.

Keywords—Modular Multilevel Converter (MMC), Fault-Tolerant Control, signal-processing technique, Radial Basis Function Neural Network (RBFNN), Discrete Wavelet Transform (DWT), Fuzzy Logic

Résumé

Les convertisseurs multiniveaux modulaires (MMC) représentent une technologie clé dans les systèmes électriques de forte puissance grâce à leur haut rendement, leur modularité et leur évolutivité. Toutefois, leur structure complexe les rend sensibles à divers défauts, tels que les défaillances des interrupteurs de puissance et les dysfonctionnements des condensateurs de sous-modules, pouvant compromettre à la fois les performances et la stabilité du système.

Ce travail de thèse s'inscrit dans le cadre du développement de stratégies de diagnostic et de commande tolérante aux défauts pour la résilience des MMC, une méthode intelligente de détection des défauts circuit ouverte des IGBT et de leurs diodes antiparallèles est proposée. Basé sur l'association de la logique floue et du traitement du signal afin d'améliorer l'extraction de caractéristiques et la précision de localisation., une autre approche hybride est introduite pour la détection de courts-circuits multiples dans le même sous-module, intégrant un réseau de

neurones à fonctions de base radiale (RBFNN) et la transformée en ondelettes discrète (DWT), renforçant ainsi la robustesse du diagnostic. Une méthode rapide de traitement du signal est ensuite développée pour la détection des courts-circuits d'IGBT, permettant de réduire significativement le temps de détection et de garantir des actions de protection rapides. Enfin, une stratégie simple de commande tolérante aux défauts est mise en œuvre pour gérer les pannes de condensateurs, assurant un fonctionnement stable en mode dégradé.

L'ensemble des approches proposées a été validé par simulations sous MATLAB/Simulink sur un modèle de MMC à cinq niveaux, confirmant leur efficacité en termes de précision de diagnostic et de fiabilité opérationnelle.

Mots-clés — Convertisseur multiniveaux modulaire (MMC), Commande tolérante aux défauts, Réseau de neurones RBF, Transformée en ondelettes discrète (DWT), Logique floue, Traitement du signal.

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Appendix

List of Abbreviations and Symbols

Abbreviation

1D-CNN	:	1 dimensional Convolutional Neural Network
AC	:	Alternating current
AFTC	:	Active Fault tolerant control
AI	:	Artificial intelligence
ANFIS	:	Adaptive Neuro-Fuzzy Inference System
ANN	:	Artificial neural network
APOD	:	Alternative phase opposition disposition
CHB	:	Cascaded H-Bridge
CVI	:	Capacitor Voltage Increasing
DC	:	Direct current
DWT	:	the Discrete Wavelet Transform
ESO	:	Extended Sliding Mode Observer
FACTS	:	Flexible AC Transmission Systems
FB	:	Full bridge
FC	:	Flying Capacitor
FD	:	Fault detection
FDI	:	Fault Detection and Identification
FIR	:	finite impulse response
FL	:	Fault localization
FTC	:	Fault tolerant control
HB	:	Half bridge
HVDC	:	High Voltage Direct Current
IGBTs	:	Insulated Gate Bipolar Transistor
LS-PWM	:	Level-Shifted PWM

MKSTM	:	mixed-kernel support tensor machines
MLCs	:	Multilevel Converters
MMC	:	Modular Multilevel Converter
NLM	:	Nearest Level Modulation
NPC	:	Neutral-Point-Clamped
OCF	:	Open-circuit fault
PCA	:	Principal component analysis
PD	:	Phase disposition
PFTC	:	Passive Fault tolerant control
POD	:	Phase Opposition disposition
PS-PWM	:	Phase-Shifted Pulse Width Modulation
PWM	:	Pulse-width modulation
RBFNN	:	Radial basis function neural network
RMS	:	Root mean square
RMS-CC	:	Root mean square current comparison
RNN	:	recurrent neural network
SCF	:	Short-circuit fault
SHE	:	Selective Harmonic Elimination
SMOs	:	Sliding Mode Observers
SMs	:	Sub-modules
STD	:	Standard deviation
SVM	:	Support vector machine
SVPWM	:	Space Vector Pulse-width modulation
THD	:	Total Harmonic Distortion
VSCs	:	Voltage source converters
WOF	:	wear-out faults
ZSVI	:	Zero-Sequence Voltage Injection

Symbols

C_{SM}	:	SM Capacitor
$\|h(t)\|$	:	the Hilbert envelope
$\max(\|h_i(t)\|)$	:	Max of the Hilbert envelope
K_δ	:	tuning factor.
f_{eff}	:	The effective frequency
$\emptyset$	:	The phase-shifted angle
Bp_i	:	Fault flags
$Bp_{u,l}$	:	Activation signals
Ceq	:	The equivalent capacitance
D_{coef}	:	the detail coefficients
G_i	:	Control signal
i_{ac}	:	Output current
i_{idff}	:	Circulating current
i_l	:	Current across the lower arm
i_{SM}	:	Current across SM capacitor
i_u	:	Current across the upper arm
L_{arm}	:	Arm inductor
m_l	:	modulation index for lower arm
m_u	:	modulation index for upper arm
N	:	Number of SM per arm
N_n	:	Number of SMs inserted in the lower arm
N_p	:	Number of SMs inserted in the upper arm
N_r	:	Number of redundant SM

$\mathbf{N_{sm}}$	:	Number of activated SM
$\boldsymbol{R_{arm}}$	:	Arm resistor
$\mathbf{RMS}_{\boldsymbol{idiff\ mes}}$	:	the measured value
$\boldsymbol{S}$	:	Switching state
$\mathbf{SM_r}$	:	Redundant submodule
$\mathbf{S_{r\ u,l}}$	:	Switching state of redundant
$\boldsymbol{U_c}$	:	Voltage across SM capacitor
$\boldsymbol{V_o}$	:	Output voltage
$\boldsymbol{V_{DC}}$	:	DC bus voltage
$\boldsymbol{v_p}$	:	Voltage across the upper arm
$\mathbf{Vc_r}$	:	Capacitor voltage of redundant
$\boldsymbol{v_F}$	:	Voltage of full bridge SM
$\boldsymbol{v_H}$	:	Voltage of half bridge SM
$\boldsymbol{v_n}$	:	Voltage across the lower arm
$\boldsymbol{\mu}\ \mathbf{RMS}_{\boldsymbol{idiff\ ref}}$	:	mean RMS current during normal operation
$\boldsymbol{w_i}$	:	weight
$\boldsymbol{\delta}$	:	the threshold value of the RMS-CC

General Introduction

The growing demand for electrical energy and the global shift toward renewable sources has increased the requirements on power electronic systems, which must now be efficient, reliable, and capable of handling high voltages and power levels. Multilevel converters (MLCs) have emerged as a key solution for medium- and high-voltage applications due to their scalability, reduced harmonic distortion, and high efficiency [1]. Compared to conventional two-level converters, MLCs generate nearly sinusoidal waveforms by combining multiple voltage levels, making them suitable for HVDC transmission, FACTS, motor drives, and renewable integration.

Several topologies exist, including Neutral-Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-Bridge (CHB), and the Modular Multilevel Converter (MMC), each with trade-offs in scalability, complexity, and fault tolerance [2]. Among them, the MMC has become the most prominent, especially in HVDC and large-scale renewable systems. Thanks to its modular design, the converter can handle very high voltages and power levels while operating at relatively low switching frequencies The MMC offers key benefits such as high efficiency, low voltage stress on devices, excellent harmonic performance, flexible scalability, and improved reliability through submodule redundancy [3].

MOTIVATION

Despite these strengths, the complex structure of MMCs also introduces significant challenges. Each converter arm is composed of several submodules, and each submodule integrates semiconductor switches (typically IGBTs with anti-parallel diodes) and capacitors. The use of many devices inherently increases the chance of failures, which can compromise system performance or even lead to catastrophic failure if not handled appropriately. Typical faults encountered in MMCs include [4]:

- Open-circuit faults in IGBTs or their anti-parallel diodes, which disturb current paths and lead to unbalanced arm currents.
- Short-circuit faults**,** particularly in power switches, which can cause severe current surges and potential damage to the entire converter.
- Capacitor failures**,** such as degradation or malfunction, which impair voltage balancing and system stability.

Such faults emphasize the vital role of fault detection, localization, and fault-tolerant control in MMCs. Without advanced monitoring and protection schemes, faults may propagate rapidly, leading to costly downtime or even permanent damage to the system.

This concern forms the motivation of the present work**.** While numerous diagnostic techniques have been proposed in the literature [5-7], several limitations remain. Many methods are restricted to detecting only specific fault types, such as open-circuit faults in IGBTs [8,9], without considering diode-related faults. Others suffer from slow response times, limited accuracy in localizing the faulty submodule [10,11], or difficulties in distinguishing between similar fault signatures. Furthermore, few studies address capacitor-related faults and their integration into a complete fault-tolerant control framework**.** [12,13]

CONTRIBUTION

To address these gaps, this thesis proposes a set of intelligent fault detection, localization, and control strategies tailored for MMCs. The main contributions of this research are outlined below.

- ✓ Intelligent methods for fault detection and localization were proposed to diagnose both IGBTs and anti-parallel diodes open-circuit fault.
- ✓ Multiple short-circuit faults within a single submodule were detected and localized using a hybrid diagnostic method.
- ✓ A novel and fast signal-processing-based method was developed for accurate IGBT short-circuit diagnosis.
- ✓ A simple fault-tolerant control strategy, based on intelligent decision-making and logical operators, was proposed to handle capacitor failures.

By addressing multiple fault types and proposing both diagnostic methods and control strategies**,** this work aims to improve the reliability, safety, and availability of MMC-based systems.

THESIS OUTLINE

The remainder of this thesis is organized as follows:

- **Chapter I** provides a general overview of multilevel converter topologies, with a particular emphasis on MMCs. It introduces MMC operating principles, mathematical modeling, modulation techniques, control strategies, and typical faults.
- **Chapter II** addresses open-circuit fault detection and localization in MMC submodules. It begins by analyzing the impact of such faults on converter performance and stability. Two diagnostic approaches are then developed: one using Artificial Neural Networks (ANNs) for automatic classification, and another combining Discrete Wavelet Transform (DWT) with fuzzy logic for improved accuracy. Both methods are validated through simulations under different operating conditions. Results show their effectiveness in identifying and localizing open-circuit faults.
- **Chapter III** focuses on short-circuit faults, among the most severe failure modes in MMCs. After examining their behavior and influence on system performance, the chapter introduces diagnostic methods based on signal processing and machine learning. DWT-extracted features are classified using Radial Basis Function Neural Networks (RBFNNs) for rapid and reliable detection. Complementary signal processing techniques are also presented to improve robustness and sensitivity. Simulation results confirm fast detection and effective fault localization, minimizing system risks.
- **Chapter IV** investigates capacitor failures, critical due to their role in energy storage and voltage balancing in MMCs. The chapter reviews existing fault-tolerant control (FTC) strategies, highlighting their strengths and limitations. Based on this, a novel FTC method is proposed to maintain stability and output quality under capacitor faults. The strategy also aims to extend converter lifetime by mitigating capacitor degradation. Simulation studies verify its effectiveness and demonstrate potential for real-world implementation.
- **Conclusion** summarizes the main conclusions of this research and suggests possible directions for future work.

Chapter I

Overview of Modular Multilevel Converters: Topologies, Operation, and Fault Management.

I.1.Introduction

Due to their scalable structure, multilevel converters have become extensively applied in modern power electronics, high-quality output waveforms, and efficiency. Among them, MMC is considered one of the most important topics in research and industry.

This chapter first reviews major multilevel topologies Neutral-Point Clamped (NPC), Flying Capacitor (FC), Cascaded H-Bridge (CHB), and MMC highlighting their main features. The operating principles of MMCs are then presented, focusing on submodule configurations, the behavior of a single-phase leg, and differences between half-bridge and full-bridge submodules.

A simplified mathematical model of the MMC is introduced to support analysis and control design. Based on this model, modulation techniques such as Level-Shifted PWM (LS-PWM) and Phase-Shifted PWM (PS-PWM) are discussed, along with open- and closed-loop control strategies, emphasizing the balance between simplicity and dynamic performance.

Finally, typical MMC faults open-circuit, short-circuit, and capacitor failures are described, followed by an overview of detection and isolation methods aimed at improving system reliability.

I.2. Multilevel converters

In medium-voltage and high-power systems, Multilevel Converters (MLCs) are commonly adopted since they can generate multi-level output signals. Such operation minimizes total harmonic distortion (THD), improves power quality, and alleviates voltage stress across devices relative to standard two-level topologies [14,15]

these topologies can be grouped into four main families as illustrate in Figure.I.1:

- Neutral Point Clamped (NPC)
- Flying Capacitor (FC)

- Cascaded H-Bridge (CHB)
- Modular Multilevel Converter (MMC)

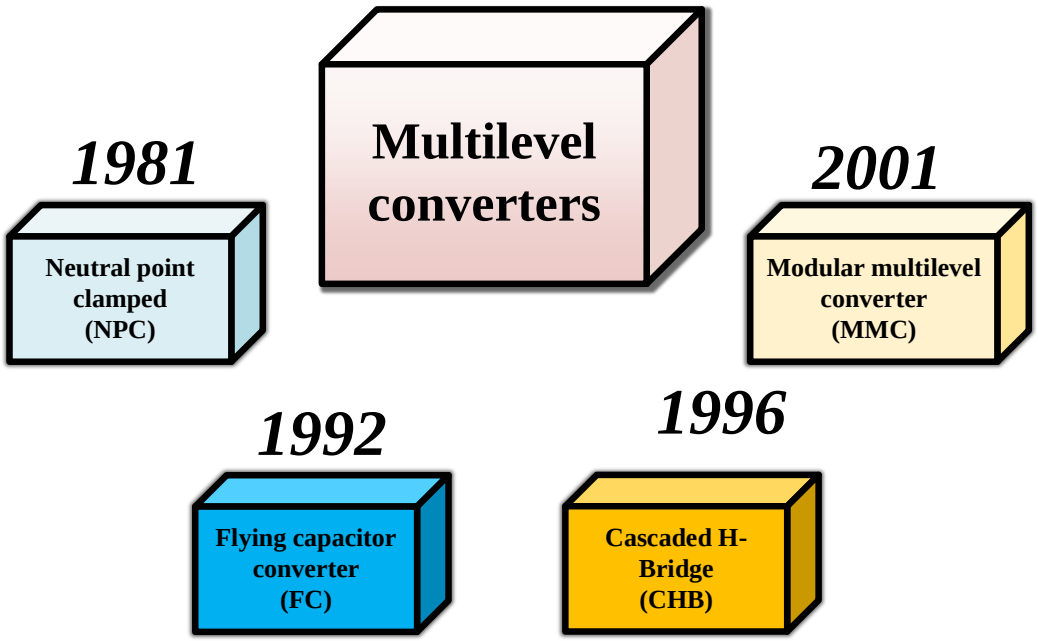


Figure.I.1 : Multilevel converters

I.2.1. The Neutral Point Clamped (NPC) converter

The Neutral-Point Clamped (NPC) converter, introduced by Nabae et al. in 1981, is widely applied in high-voltage industrial drives for its ability to handle high power and reduce device voltage stress [16,17].

As shown in Figure I.2, the NPC topology employs clamping diodes to connect the DC-link midpoint to the output, using four switches per arm. This allows generation of three or more voltage levels, resulting in improved waveform quality and reduced semiconductor stress compared to two-level VSCs [18].

Key advantages include the absence of separate DC sources and enhanced power quality through clamping diodes. However, challenges remain, such as DC-link capacitor voltage imbalance,

diode voltage stress, increased design complexity with higher levels, and reduced reliability due to the large component count [14,18].

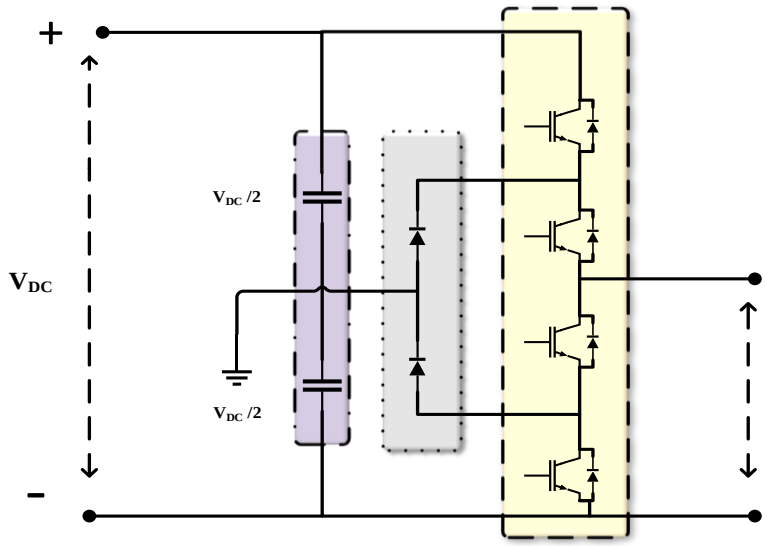


Figure I.2: structure of NPC

I.2.2. The Flying Capacitor (FC) converter

The Flying Capacitor (FC) converter, proposed by Meynard and Foch in 1992, uses floating capacitors to generate intermediate voltage levels, enabling more levels than the NPC topology and improving waveform quality while reducing THD [19].

Structurally similar to NPC but with flying capacitors instead of clamping diodes (Figure I.3), the FC converter offers modularity, scalability, redundancy, and improved fault tolerance, making it suitable for medium- and high-voltage applications [20,21].

However, its main limitation is capacitor voltage ripple, which depends on load current and switching frequency. Mitigation requires larger capacitors (increasing size and cost) or higher switching frequencies (causing greater losses and reduced efficiency) [22,23].

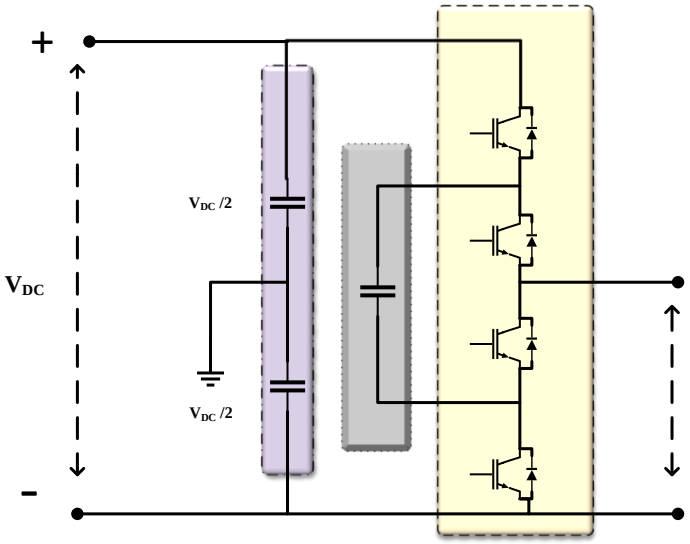


Figure I.3:structure of FC

I.2.3. the cascaded H-bridge (CHB) converter

The Cascaded H-Bridge (CHB) converter, proposed by Lai et al. in 1996, is widely applied in motor drives and renewable energy systems due to its modular and scalable structure [24].

It is composed of series-connected single-phase H-bridge cells, each powered by an isolated DC source (Figure I.4). Each cell produces three voltage levels (positive, negative, zero), and their combination generates a staircase multilevel output with reduced THD and enhanced power quality [25]. The modular design also simplifies control and facilitates fault management, making CHB attractive for medium- and high-voltage applications [26].

However, CHB requires multiple isolated DC sources, which increases cost, size, and complexity. Maintaining voltage balance among these sources under varying load conditions is also challenging, potentially affecting performance and reliability [26].

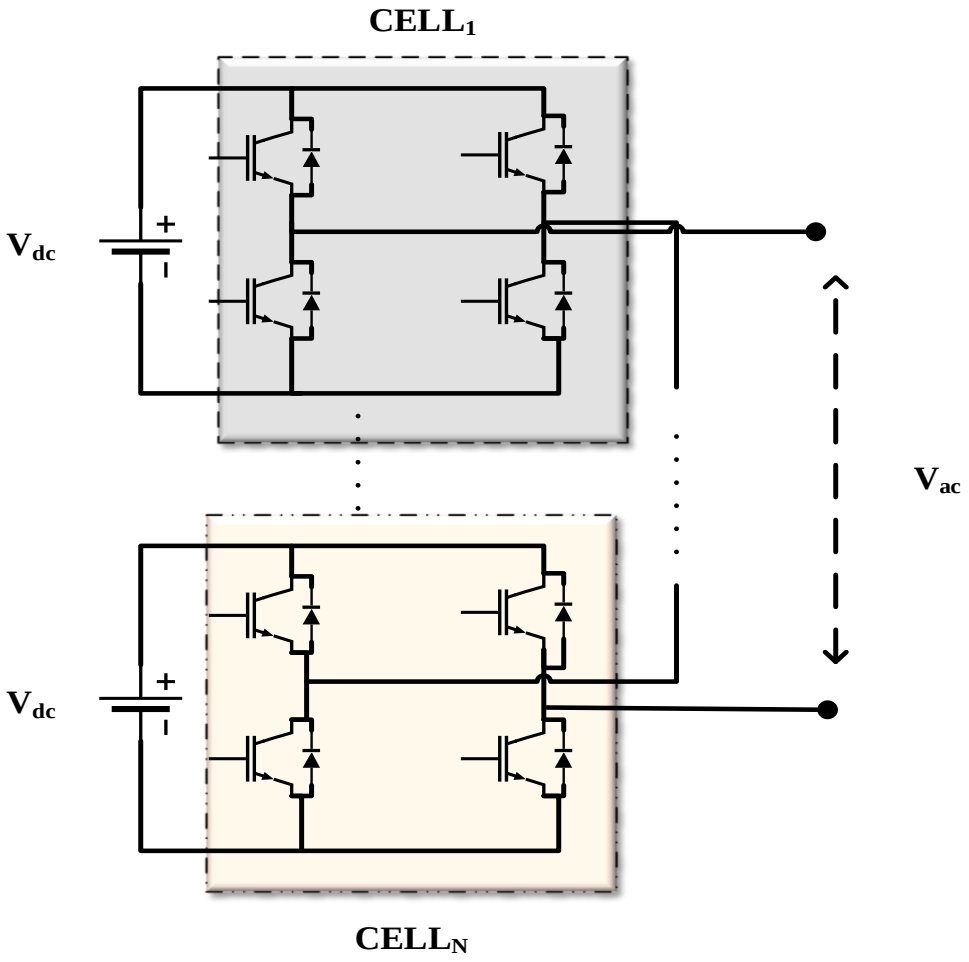


Figure I.4: structure of CHB

I.2.4. The Modular Multilevel Converter (MMC)

Developed by Marquardt and Lesnicar in 2001, the Modular Multilevel Converter (MMC) marks a significant advancement in MLCs technology, offering exceptional scalability, efficiency, and fault tolerance. The MMC is especially well-suited for high-voltage direct current (HVDC) transmission systems and large-scale industrial applications. Designed specifically to overcome the limitations of earlier topologies, Today, the MMC is viewed as a key topology for high-voltage applications, especially in transmission and distribution networks [27,28]

One of the most important advantages of MMC is its modular architecture, which reduces switching losses and eliminates the need for large central DC-link capacitors. By using a sufficient number of voltage levels, MMC can also reduce or even eliminate the need for bulky harmonic filters, improving system efficiency and simplifying design.[29]

From a structural perspective, each phase leg of an MMC is composed of several series-connected submodules. Every submodule usually incorporates a capacitor, which functions as an energy storage element between the DC link and the AC side. Depending on application requirements and the level of fault-tolerance needed, these submodules may be implemented in either half-bridge or full-bridge configurations. As shown in Figure I.5, a phase leg is separated into an upper and a lower arm, each containing the same number of submodules to ensure balanced voltage distribution within the converter. Furthermore, arm inductors are inserted to suppress circulating currents and minimize current ripple, thereby improving both stability and dynamic performance [30].

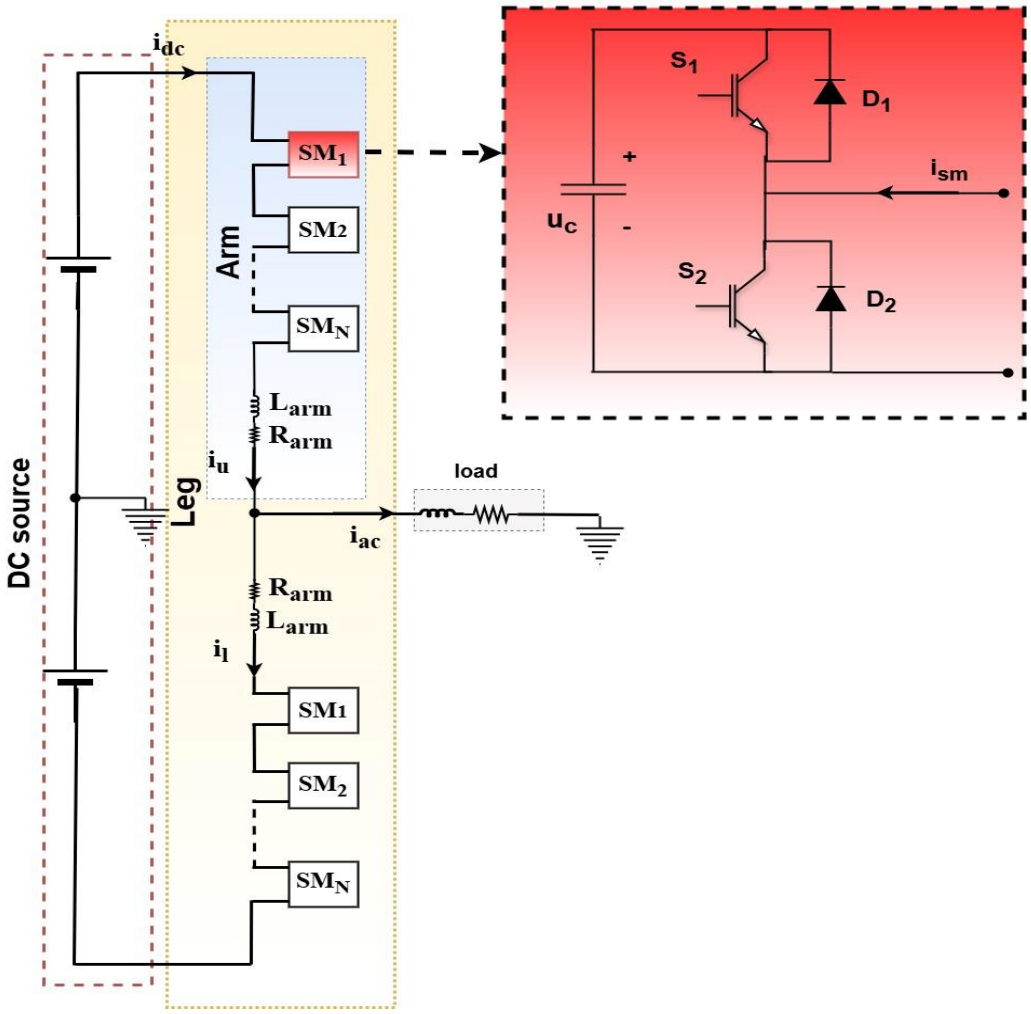


Figure.I.5*:* structure of MMC

I.3.Operating principle of Modular Multilevel Converter

Understanding the operation of a Modular Multilevel Converter (MMC) begins with its basic building block the submodule (SM), which functions as a simple DC–AC conversion circuit typically composed of low-voltage IGBTs and a DC capacitor [30].

Common SM topologies include:

- Half-Bridge (HB)
- Full-Bridge (FB)

- Flying Capacitor (FC)
- Cascaded Half-Bridge (CH)
- Double Clamp (CD)

Among these, the half-bridge and full-bridge submodules are most widely used in MMCs and will be discussed in detail in the following section.

I.3.1. Half-bridge (HB) submodule

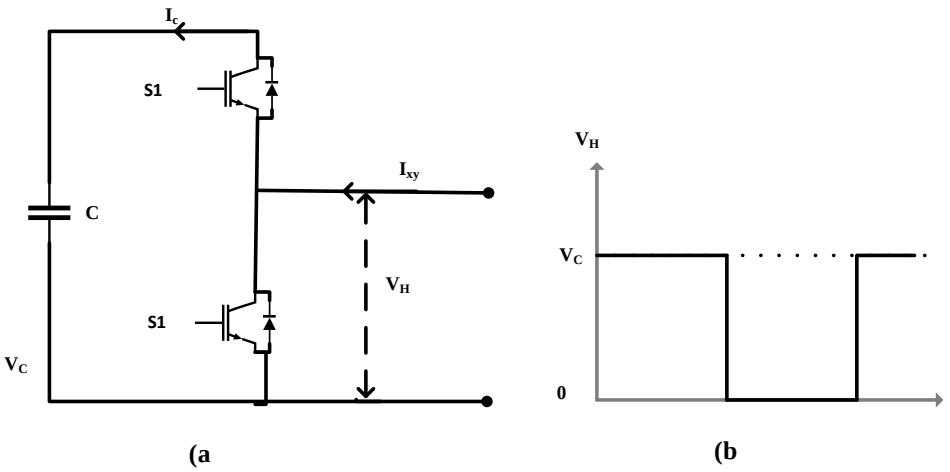


Figure I.6:a) The half- bridge SM structure, b) The AC output voltage of a half-bridge SM

HB submodule, or chopper cell, is illustrated in Figure I.6.a. This configuration consists of two IGBT switches (S1 and $\overline{S1}$), each equipped with antiparallel diodes, A single DC capacitor (C) is included, with the two IGBT switches functioning in a complementary manner to regulate its voltage at the reference value v_c [31,32]

The expression for the capacitor voltage is given by:

$$v_c = \frac{1}{C}\int_{0+}^{t} i_c(\tau)d\tau \qquad \text{I.1}$$

Where: v_c. is the capacitor voltage, $i_c(\tau)$is the current flowing into the capacitor at time τ

Depending on whether the top switch S1 is turned on or off, the DC capacitor current will either follow the AC arm current or remain zero. Table.I.1 illustrates the different switching states of

S1 and explains how these states influence the DC capacitor voltage under various directions of the AC arm current.

Table.I.1 switching states of HB-SM

State	S1	v_H	$i_{x,y} > 0$	$i_{x,y} < 0$
1	1	v_C	$v_C \uparrow$	$v_C \downarrow$
2	0	0	$v_C \approx$	$v_C \approx$

$\approx: No\ change, \uparrow: increasing, \downarrow decreasing$

The AC output voltage of a half-bridge submodule can take two levels: "0" or v_c (as illustrated in Figure I.6.b).

• **S1 ON** → The output voltage $v_H = v_c$ The capacitor charges when the arm current is positive and discharges when it is negative.

• **S1 OFF** → The output voltage $v_H = 0$ The capacitor voltage remains unchanged regardless of the current direction.

From that The AC output voltage of the submodule can generally be expressed as:

$$v_H = S1.v_C \qquad \text{I.2}$$

I.3.2. Full-bridge submodule:

The full-bridge (FB) submodule, often called an H-bridge converter, is illustrated in Figure 7.a. Its circuit consists of two half-bridge legs formed by switches (S1, $\overline{S1}$) and (S2, $\overline{S2}$) connected across a single DC capacitor (C). Each leg includes a pair of IGBT devices equipped with antiparallel diodes, which are controlled in a complementary way to achieve the desired voltage levels [31,32].

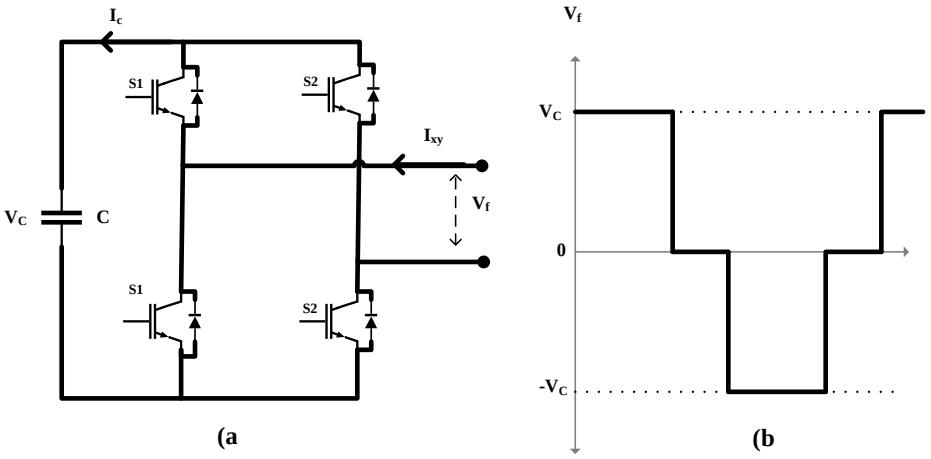


Figure I.7:a) full-bridge SM structure, b) the AC output of the full-bridge SM

In a full-bridge submodule, the DC capacitor voltage is controlled by switching devices S1 and S2. Although its capacitor voltage expression is identical to that of the half-bridge (Equation I.1), the FB can generate three output voltage levels 0, $+v_C$, and $-v_C$, through four possible switching states, as summarized in Table.I.2 and illustrated in Figure I.7.b

Table.I.2 switching states of FB-SM

State	**S1**		v_F	$i_{x,y} > 0$	$i_{x,y} < 0$
1	1	1	v_C	$v_C \uparrow$	$v_C \downarrow$
2	1	0	0	$v_C \approx$	$v_C \approx$
3	0	1	0	$v_C \approx$	$v_C \approx$
4	0	0	$-v_C$	$v_C \downarrow$	$v_C \uparrow$

$\approx: No\ change, \uparrow: increasing, \downarrow decreasing$

- **S1, S2 ON** → Output voltage $v_H = v_C$,The capacitor charges with positive arm current and discharges with negative current.
- **S1 ON & S2 OFF, or S1 OFF & S2 ON** → Output voltage $v_H = 0$. The capacitor voltage remains constant. These redundant states help balance power losses between switches.
- **S1, S2 OFF** → Output voltage $v_H = -v_C$

The overall relation between output voltage, capacitor voltage, and switching states is expressed by Equation I.3

$$v_F = (S1S2 - \overline{S1S2})v_c \qquad \text{I.3}$$

I.3.3. operating principle of single-phase MM

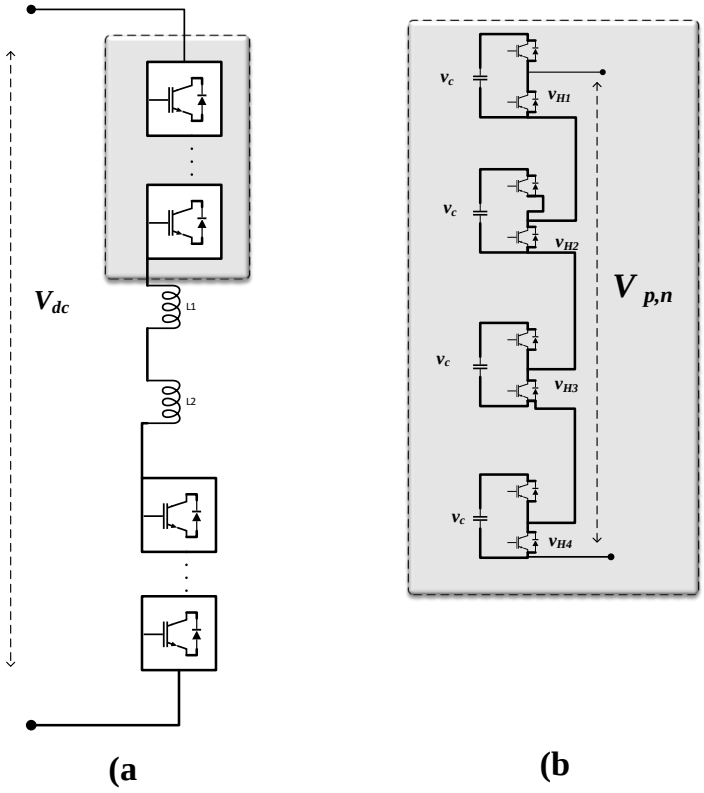


Figure I.8 :a) five level MMC, b) MMC arm

In this section, the operation of a modular multilevel converter (MMC) based on the widely used half-bridge submodule is described. The structure of a single-phase MMC is illustrated in Figure.I.8. a, where each arm consists of four identical half-bridge submodules connected in series, as shown in Figure I.8.b. Each submodule is equipped with a capacitor rated at voltage v_c, and the corresponding submodule output voltages are labeled as $v_{H1}, v_{H2}, v_{H3}, v_{H4}$, These submodule output terminals are cascaded to generate the total arm voltage

The different switching states of the submodules, along with the resulting submodule and arm output voltages, are presented in Table.I.3. For an arm composed of four submodules, the arm voltage can step through five discrete voltage levels: "0,v_c,2v_c,3$v_c$and 4v_c", The maximum arm voltage, 4v_c, is achieved by turning ON all four switches S1, S2, S3, S4 , whereas the minimum voltage level, 0, is obtained by turning all switches OFF.As indicated in Table.I.3, the intermediate voltage levels can be produced by different switching combinations, known as redundant switching states. These redundant states are typically exploited to regulate the capacitor voltages within the submodules.

Table.I.3 switching state and voltage level

S1	**S2**	**S3**	**S4**	v_{H1}	v_{H2}	v_{H3}	v_{H4}	$v_{P,n}$
0	0	0	0	0	0	0	0	0
1	0	0	0	v_C	0	0	0	v_C
0	1	0	0	0	v_C	0	0	v_C
0	0	1	0	0	0	v_C	0	v_C
0	0	0	1	0	0	0	v_C	v_C
1	1	0	0	v_C	v_C	0	0	$2v_C$
1	0	1	0	v_C	0	v_C	0	$2v_C$
1	0	0	1	v_C	0	0	v_C	$2v_C$
0	1	1	0	0	v_C	v_C	0	$2v_C$
0	1	0	1	0	v_C	0	v_C	$2v_C$
0	0	1	1	0	0	v_C	v_C	$2v_C$
1	1	1	0	v_C	v_C	v_C	0	$3v_C$
1	1	0	1	v_C	v_C	0	v_C	$3v_C$
1	0	1	1	v_C	0	v_C	v_C	$3v_C$
0	1	1	1	0	v_C	v_C	v_C	$3v_C$
1	1	1	1	v_C	v_C	v_C	v_C	$4v_C$

From Table.I.3 The equation describing the arm voltage$v_{p,n}$

$$v_{p,n} = v_{H1} + v_{H2} + v_{H3} + v_{H4} = S1v_C + S2v_C + S3v_C + S4v_C \quad \text{I.4}$$

By selectively activating a specific number of submodules (SMs) within each arm, the converter is able to regulate and control the resulting arm voltage levels.$v_{p,n}$so, the arm voltage can be writing as:

$$\begin{cases} v_{p=N_P}.v_C \\ v_{n=N_n}.v_C \end{cases} \quad \text{I.5}$$

Where:

v_p,v_n are the upper and lower voltage arm respectively,N_P,$N_n$are the number of SMs inserted in the upper and lower arm respectively

To produce the desired output waveform, the output voltage $v_0$is obtained from the voltages across the upper armv_p and the lower arm v_n.

$$v_0 = -v_p + \frac{V_{dc}}{2} = v_n - \frac{V_{dc}}{2} \quad \text{I.6}$$

Where:

V_{dc} is the DC bus voltage

This operational principle can be readily generalized to accommodate any number of submodules per arm. By increasing the number of submodules, the converter gains finer voltage resolution and improved waveform quality, which enables more precise control, reduced harmonic distortion, and enhanced scalability for high-voltage and high-power applications. [33,34].

I.4. MMC mathematical model

To analyse and control the behaviour of the single-phase Modular Multilevel Converter (MMC), a mathematical model is essential. The model captures the dynamic interaction between the arm currents, submodule capacitor voltages, and the AC output voltage, forming the basis for control design and simulation studies.

As shown in Figure I.9, the converter arms in an MMC are represented as variable capacitors connected in series with arm inductance. It is assumed that the number of submodules per arm is quite enormous and the switching frequency is very high for analytical simplicity and to better explain the basic behaviour of the circuit. The approximation of continuous voltage and current waveforms made possible by this assumption makes it easier to analyse the system's dynamic responsiveness and performance. [34,35].

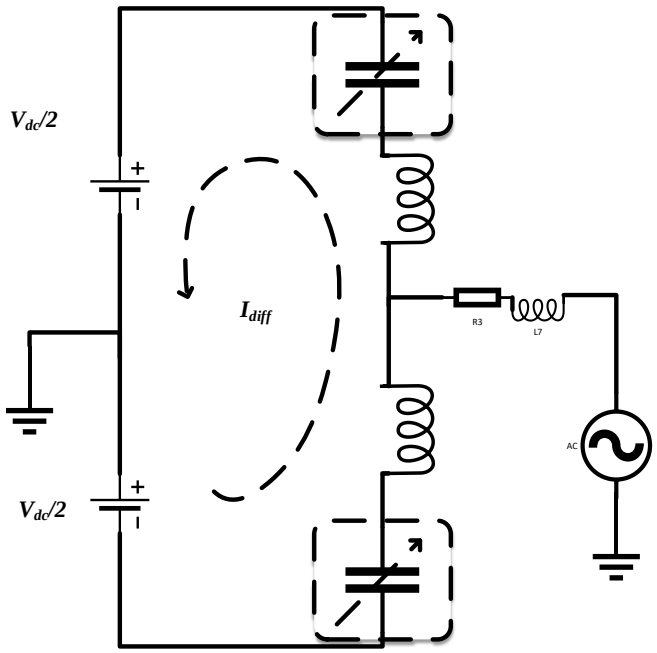


Figure I.9:equivalent circuit of MMC

The capacitor banks in each arm are modelled using a modulation index:

m_u : for the upper arm

m_l : for the lower arm

Both indices range from 0 (fully bypassed) to 1 (fully inserted). The sum of voltages across inserted submodule capacitors is denote $\sum v_{cu}$ and $\sum v_{cl}$for upper and lower arms, respectively.

The voltage in each arm is defined as:

$$v_u(t) = m_u . \sum_{1}^{N} v_{cui} \quad \text{I.7}$$

$$v_u(t) = m_u . \sum_{1}^{N} v_{cui} \quad \text{I.8}$$

The equivalent capacitance in each arm can be represented as:

$$C_{eq_u = \frac{C_{SM}}{N m_u(t)}} \quad \text{I.9}$$

$$C_{eq_l = \frac{C_{SM}}{N m_l(t)}} \quad \text{I.10}$$

Where C_{SM} is the capacitance of a single submodule, and *N* is the number of submodules per arm.

If $i_u(t)$ and $i_l(t)$ represent the current in the upper and lower arms, then the capacitor voltage evolution becomes:

$$\frac{d}{dt}\sum v_{cu} = \frac{i_u(t)}{C_{eq_u}} \quad \text{I.11}$$

$$\frac{d}{dt}\sum v_{cl} = \frac{i_l(t)}{C_{eq_l}} \quad \text{I.12}$$

The alternating output current$i_{ac}$is defined as:

$$i_{ac} = i_u - i_l \quad \text{I.13}$$

The differential current, i_{diff}represents the current flowing through the phase leg. Assuming balanced arm voltages, this current equally contributes to both the upper and lower arms. The currents in the upper (i_u) and lower (i_l) arms can be expressed in terms of i_{diff} and the AC current (i_{ac}) as follows:

$$i_u = i_{diff} + \frac{i_{ac}}{2} \quad \text{I.14}$$

$$i_l = i_{diff} - \frac{i_{ac}}{2} \quad \text{I.15}$$

$$i_{diff} = \frac{i_u + i_l}{2} \quad \text{I.16}$$

The capacitor voltage dynamics can be expressed for the upper and lower arms by:

$$\frac{d\sum_1^N v_{cui}}{dt} = \frac{N.m_u.i_u}{C_{SM}} \quad \text{I.17}$$

$$\frac{d\sum_1^N v_{cli}}{dt} = \frac{N.m_l.i_l}{C_{SM}} \quad \text{I.18}$$

By applying Kirchhoff's Voltage Law (KVL) to the circuit shown in Figure I.9, the output AC voltage (v_o) can be expressed for the upper and lower arms as:

$$v_o = \frac{V_{dc}}{2} - R_{arm}i_u - L_{arm}\frac{d_{i_u}}{dt} - m_u.\sum_1^N v_{cui} \quad \text{I.19}$$

$$v_o = -\frac{V_{dc}}{2} + R_{arm}i_l + L_{arm}\frac{d_{i_l}}{dt} - m_l.\sum_1^N v_{cli} \quad \text{I.20}$$

V_{dc}: DC link voltage. $R_{arm}$and L_{arm} Resistance and inductance of each arm, respectively.

I.5.modulation and control techniques of MMC

The modulation strategy employed in Modular Multilevel Converters (MMCs) is a key factor in their operation, as they determine how submodules (SMs) are inserted or bypassed, shaping the output voltage waveform. It also ensures capacitor voltage balance, suppresses circulating currents, and directly impacts system performance in terms of efficiency, harmonic distortion, and dynamic response [36,37].

Over the years, a variety of modulation strategies have been proposed and developed. These can generally be classified into three main categories Figure I.10:

1. Staircase-Based Modulation,
2. Carrier-Based Pulse Width Modulation (PWM),
3. Space Vector-Based PWM (SVPWM).

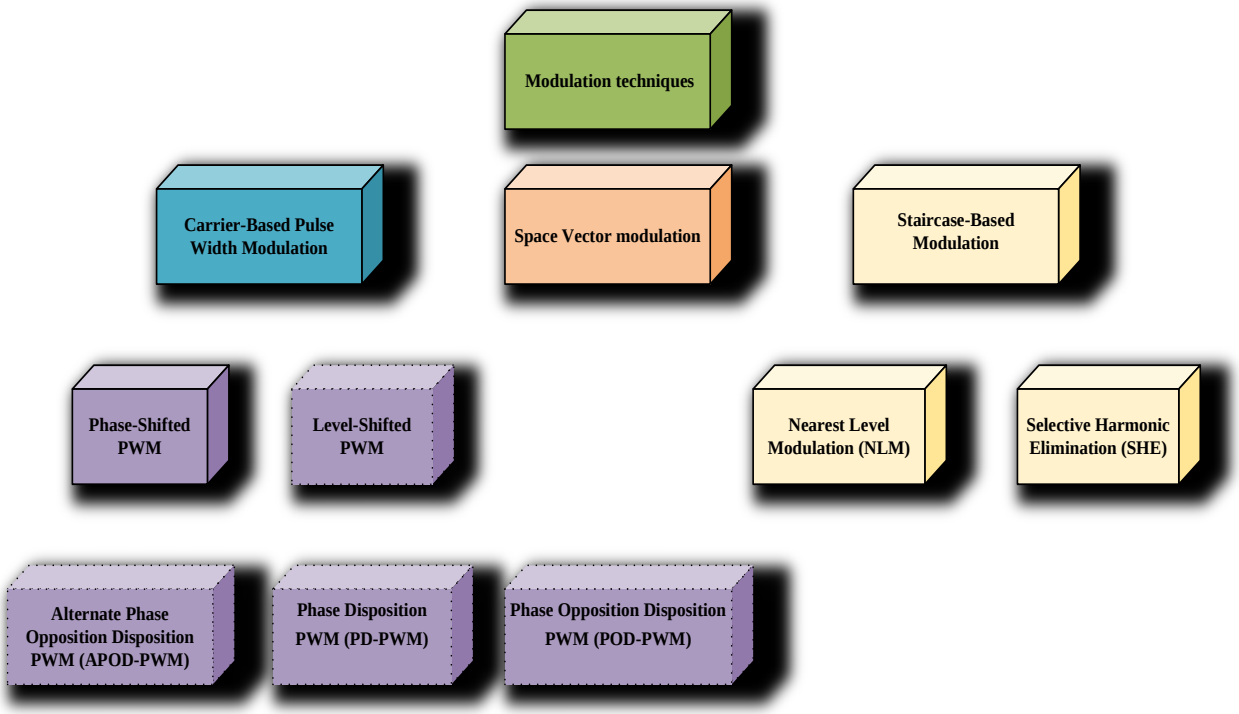


Figure I.10 :Modulation techniques

- **Staircase-based modulation techniques:** such as Nearest Level Modulation (NLM)and Selective Harmonic Elimination (SHE)**,** generate the output waveform by directly controlling the number of submodules (SMs) inserted into each arm at every instant. NLM is particularly attractive for high-voltage direct current (HVDC) systems and other low-frequency applications due to its ability to produce high-quality output voltage with very low switching frequency [38,39]. In contrast, SHE determines specific precomputed switching angles to selectively cancel targeted low-order harmonics, thereby improving the waveform quality without significantly increasing switching frequency [40,41].

Although both approaches achieve low switching losses and excellent steady-state performance, they generally have limited flexibility under dynamic operating conditions and often require complex control algorithms to implement effectively [36].

- **Space Vector Pulse Width Modulation (SVPWM):** extends conventional vector modulation techniques to Modular Multilevel Converters (MMCs), providing optimized switching sequences that minimize switching losses while maintaining favorable harmonic performance. Additionally, SVPWM contributes to effective capacitor voltage balancing, which is critical for MMC operation. Despite these advantages such as enhanced spectral quality and improved dynamic response SVPWM is relatively complex to implement in practice. Its deployment typically involves advanced mathematical transformations, significant real-time computational effort, and a solid understanding of vector space theory [42-45].
- **Carrier-Based Pulse Width Modulation (PWM):** is widely used in MMCs for its simplicity, scalability, and suitability at high switching frequencies. It compares a sinusoidal reference with triangular carriers to generate gate signals, supporting modular control. The two main variants Level-Shifted PWM (LS-PWM) and Phase-Shifted PWM (PS-PWM) ensure uniform switching, balanced power loss, better thermal distribution, and capacitor voltage balancing [46–49]. This thesis focuses on Carrier-Based Sinusoidal PWM for detailed analysis.

I.5.1. Phase-shifted PWM Scheme

Phase-Shifted PWM (PS-PWM) is widely applied in MMCs, especially for medium- and high-voltage systems [50,51]. By assigning each submodule a triangular carrier of equal frequency but phase-shifted (Figure I.11*)*, PS-PWM distributes switching losses evenly, enhances harmonic quality, and remains simple to implement [52].

$$\emptyset = \frac{360°}{N} \qquad \text{I.21}$$

Where *N* is the number of submodules per arm, all SMs share the same sinusoidal reference, while each uses a distinct phase-shifted carrier. This interleaving of switching events increases

the effective switching frequency and improves harmonic cancellation. The effective frequency is expressed as:

$$\emptyset = f_{eff} = N.f_{carrier} \qquad \text{I.22}$$

This interleaving reduces low-order harmonic content, lowers total harmonic distortion (THD), and distributes switching losses more evenly, thereby extending device lifetime. It also aids in balancing submodule capacitor voltages. Under dynamic conditions, additional methods such as sorting algorithms or modulation index rescaling can be applied to further improve voltage balancing [53].

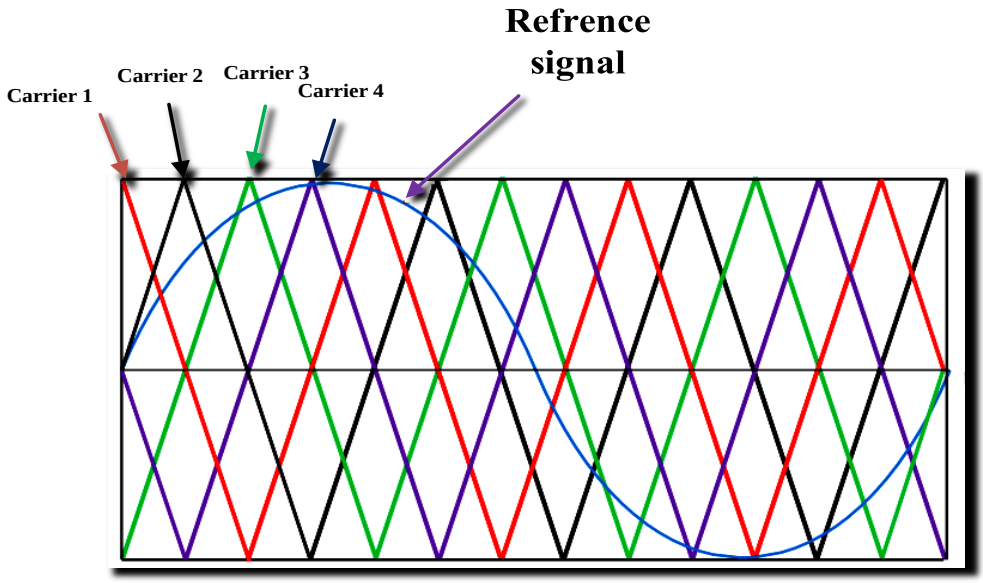


Figure I.11: PS-PWM

I.5.2. level-shifted PWM Scheme

Level-Shifted Carrier Pulse Width Modulation (LS-PWM) is a popular multicarrier technique in Modular Multilevel Converters (MMCs), particularly suited for medium- and high-voltage systems. Each submodule (SM) is assigned a triangular carrier of identical frequency and amplitude but vertically shifted to cover the full modulation range. A common sinusoidal

reference is compared with all carriers, and the number of carriers exceeded determines how many SMs are inserted, producing a stepped output waveform [54-56].

The main variants of LS-PWM are [55]:

- Phase Disposition PWM (PD-PWM)
- Phase Opposition Disposition PWM (POD-PWM)
- Alternate Phase Opposition Disposition PWM (APOD-PWM)

Phase Disposition PWM (PD-PWM)

In PD-PWM, all carriers are in phase and stacked vertically, covering the modulation range. The reference signal is compared with all carriers (Figure I.12), and SMs are inserted according to how many carriers the reference exceeds. PD-PWM is known for producing low total harmonic distortion (THD) and is straightforward to implement, making it suitable for FPGA-based control systems. It can naturally balance capacitor voltages in MMCs when combined with carrier rotation or virtual sub module mapping. [57,58].

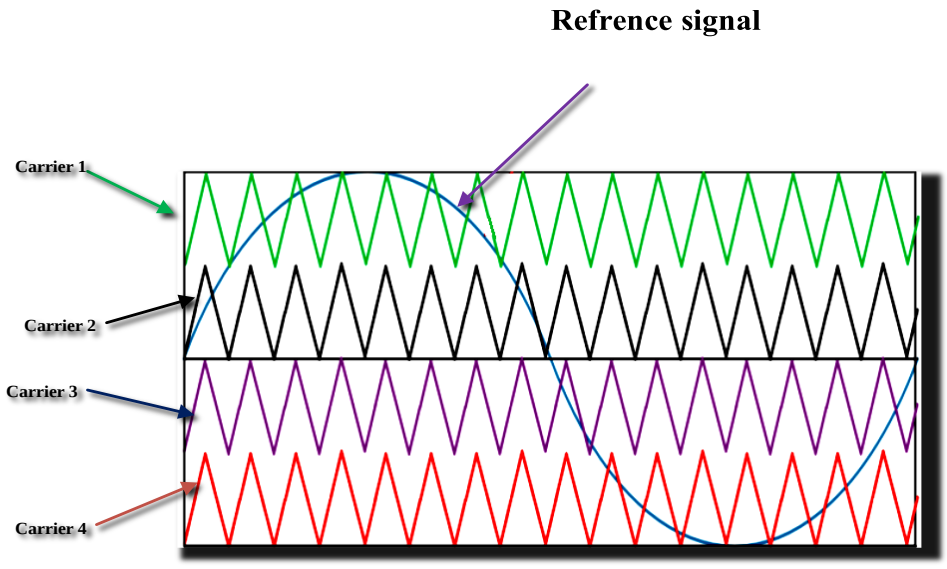


Figure I.12: PD-PWM

Phase Opposition Disposition PWM (POD-PWM)

In POD-PWM all carrier signals positioned above the zero-voltage axis are kept in phase with each other, while all carriers below the zero axis are also in phase among themselves but inverted by 180° relative to the upper group (Figure I.13),. This symmetrical arrangement of carriers enhances harmonic cancellation, particularly improving the suppression of even-order harmonics at lower modulation indices, which can lead to lower total harmonic distortion (THD) in the output voltage. However, because POD-PWM has less natural voltage self-balancing compared to phase-shifted PWM, it typically requires additional capacitor voltage balancing algorithms to ensure stable operation in Modular Multilevel Converters. [59,60].

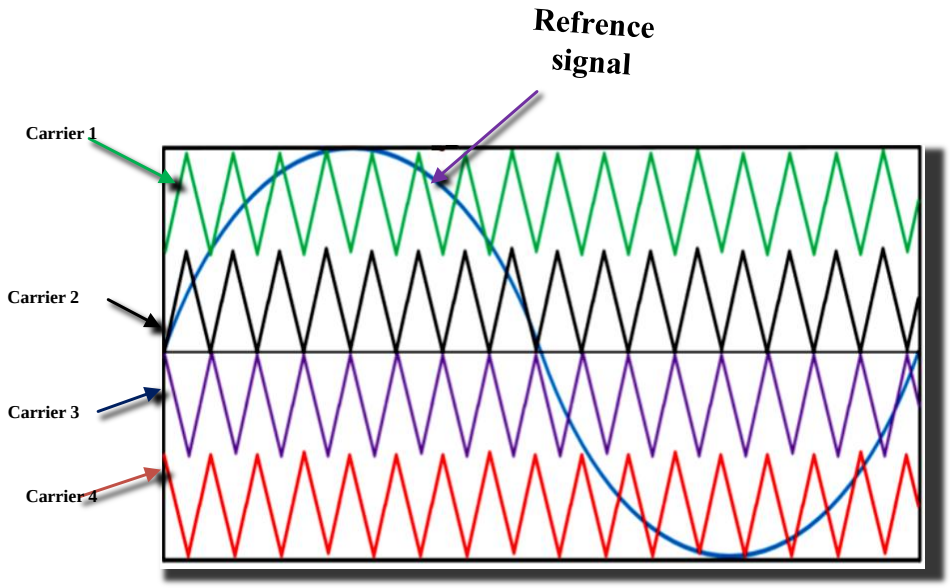


Figure.I. 13. POD-PWM

Alternate Phase Opposition Disposition PWM (APOD-PWM)

is a level-shifted multicarrier modulation method in which each consecutive carrier waveform is phase-shifted by 180°, so that adjacent carriers are always in opposite phase (Figure

I.14),. This alternating carrier pattern significantly improves harmonic cancellation and helps reduce electromagnetic interference (EMI), leading to lower total harmonic distortion (THD) particularly beneficial in converters with a higher number of levels Despite its harmonic advantages, APOD-PWM still requires dedicated capacitor voltage balancing strategies in Modular Multilevel Converters to maintain stable operation, especially during transient or dynamic conditions. [61,62].

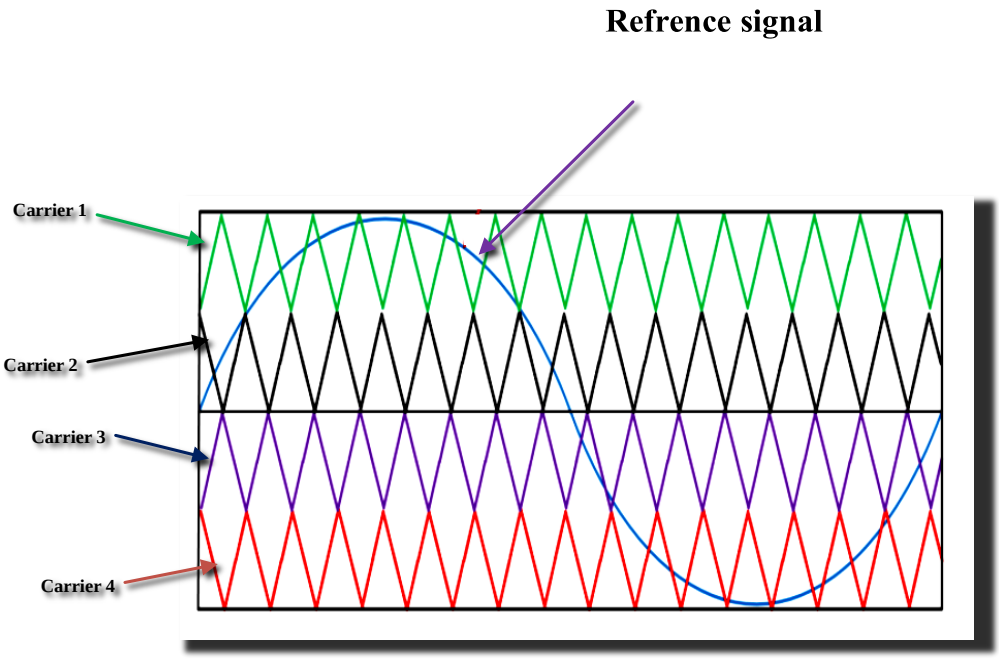


Figure I.12: APOD-PWM

In general, control of Modular Multilevel Converters (MMCs) involves managing submodule capacitor voltages, circulating currents, and output currents. Classical control methods typically use closed-loop control strategies to regulate these quantities as shows Figure I.15. Capacitor voltage control usually consists of two parts: leg voltage control, which maintains the average capacitor voltage across all submodules at a reference value, and voltage balancing control, which ensures uniform voltage sharing among submodules in each arm. Voltage balancing can be achieved using submodule selection algorithms during modulation or through dedicated controllers [63,64].

Furthermore, circulating currents and output currents are often regulated using PI controllers in the synchronous reference frame or other advanced control techniques. These classical control methods are generally compatible with various modulation schemes, such as Phase-Shifted Carrier PWM (PSCPWM), Level-Shifted PWM (LSPWM), Nearest Level Control (NLC), and Space Vector Modulation (SVM) [65].

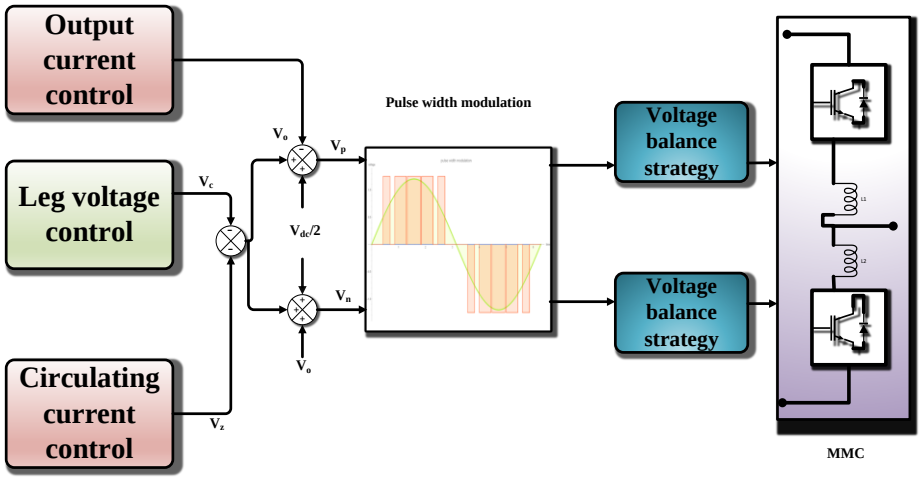


Figure I.15: control scheme of the MMC

To assess the steady-state performance of the proposed single-phase five-level Modular Multilevel Converter (MMC), an open-loop control approach was implemented. This strategy was selected to reduce the complexity associated with feedback-based control systems, making it more suitable for initial system validation and analysis. In this configuration, the converter operates using Phase-Shifted Pulse Width Modulation (PS-PWM), a well-established technique that distributes switching events across the submodules to minimize harmonics and ensure better voltage waveform synthesis. See Figure.I.16

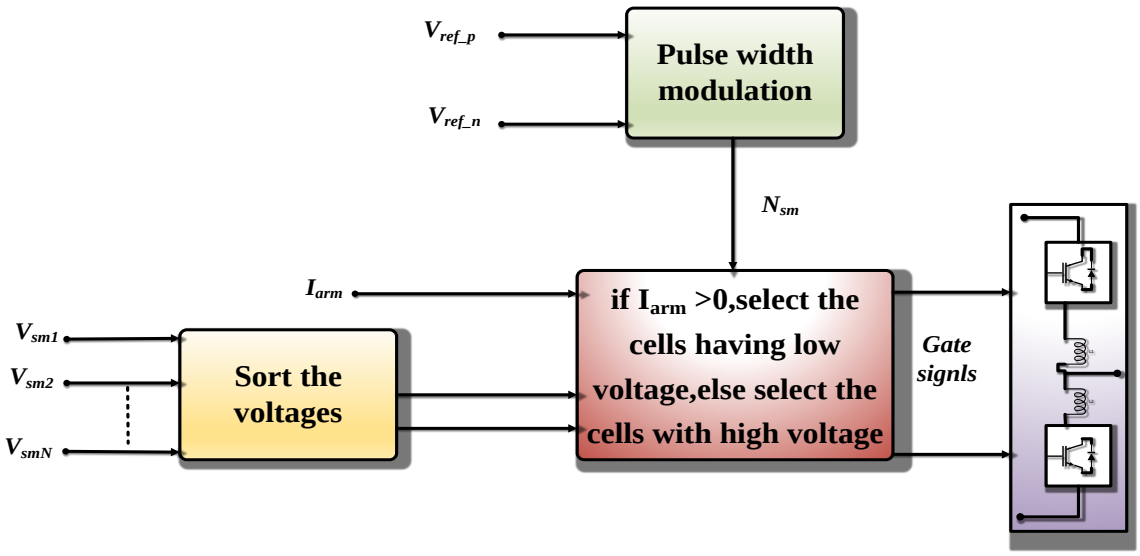
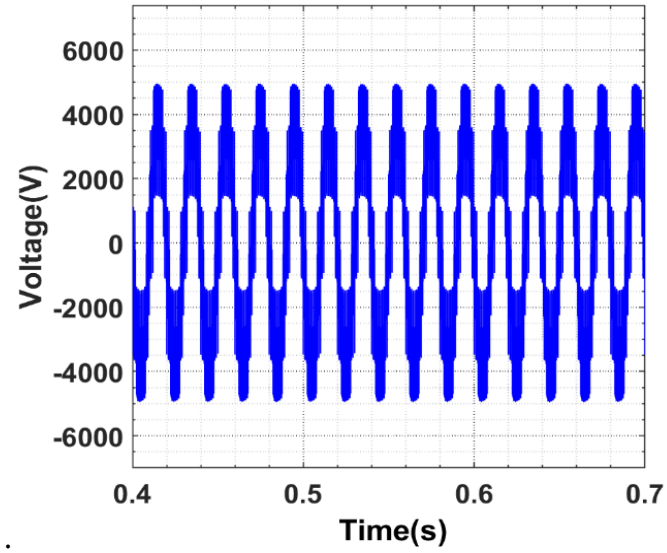


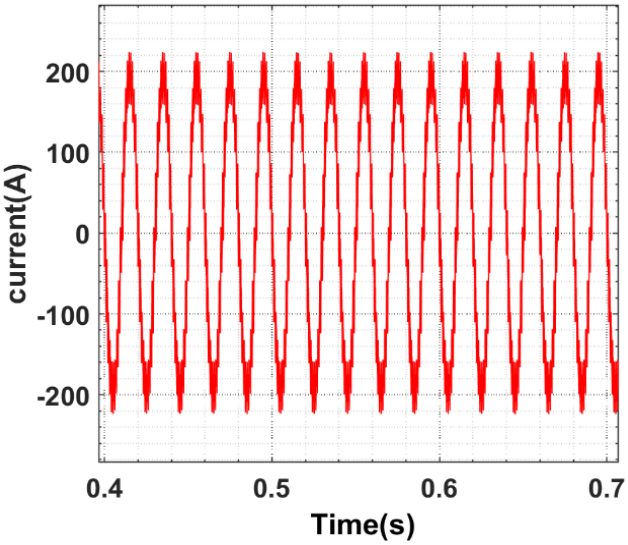
Figure I.16: open Loop control

Figure I.17 presents the simulation results that validate the correct operation of the converter under the applied control scheme. The output voltage waveform (Figure I.17.a) exhibits a clearly defined five-level staircase pattern, indicating accurate PWM timing and proper voltage level generation across the switching cycle. This waveform confirms that the submodules are being activated in the correct sequence, ensuring the synthesis of the desired output voltage.

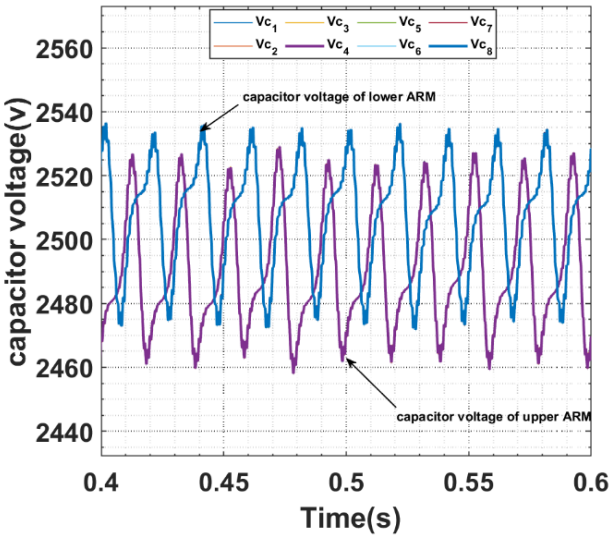
The output current waveform (Figure I.17.b) appears smooth and nearly sinusoidal, with minimal distortion. This suggests that the converter successfully replicates the reference AC current, confirming that the modulated voltage is appropriate for the connected load.

The capacitor voltage for all eight submodules (Figure I.17.c) remains relatively balanced around the nominal value of 2500 V. Although minor fluctuations are observed, these are inherent to MMC operation and are within acceptable tolerance levels. The voltage balancing algorithm effectively ensures that none of the capacitor's experiences excessive deviation, thereby preserving the reliability and longevity of the converter





a) b)



c)

Figure.I.17: simulation, results: a) output voltage, b) output current, c) capacitor voltage

I.6. common faults in modular multilevel converters

Modular Multilevel Converters (MMCs)**,** while offering significant advantages such as scalability, modularity, and high-quality output voltage, are also susceptible to various types of faults due to their complex architecture and the large number of switching components. Among the most critical failure mechanisms are open-circuit and short-circuit faults in the Insulated Gate Bipolar Transistors (IGBTs), as well as capacitor failures within the submodules. As illustrated in Figure I.18, these two components IGBTs and capacitors account for more than 50% of total converter failures, highlighting their critical impact on overall system reliability. Such faults can severely degrade the converter's performance, reduce operational safety, and potentially lead to system shutdowns if not promptly detected and mitigated [66].

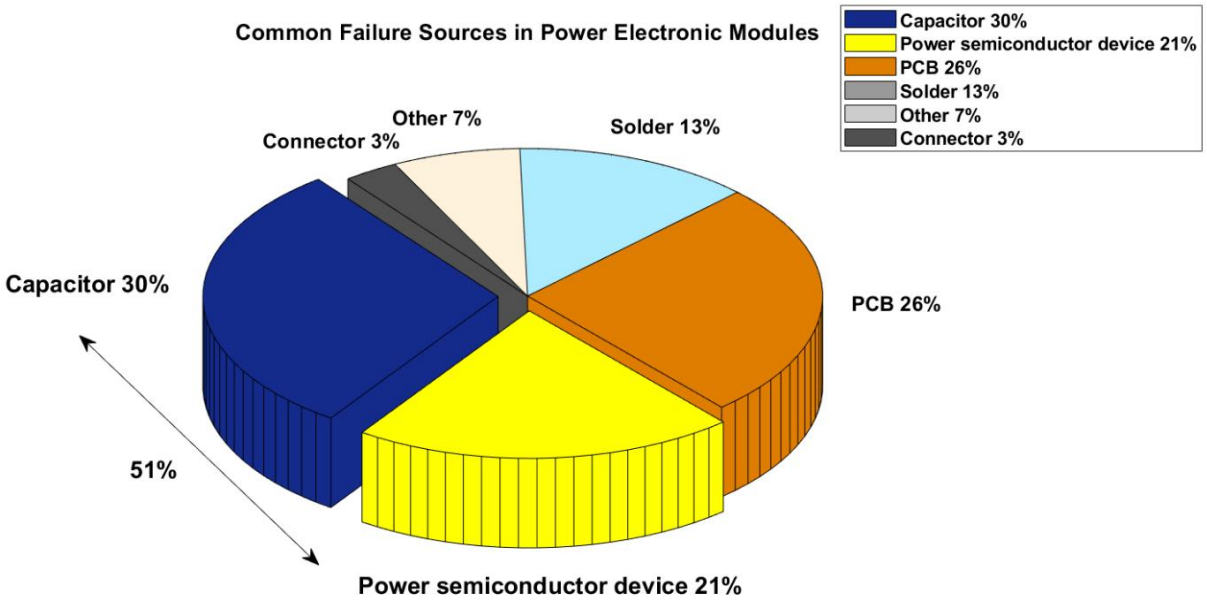
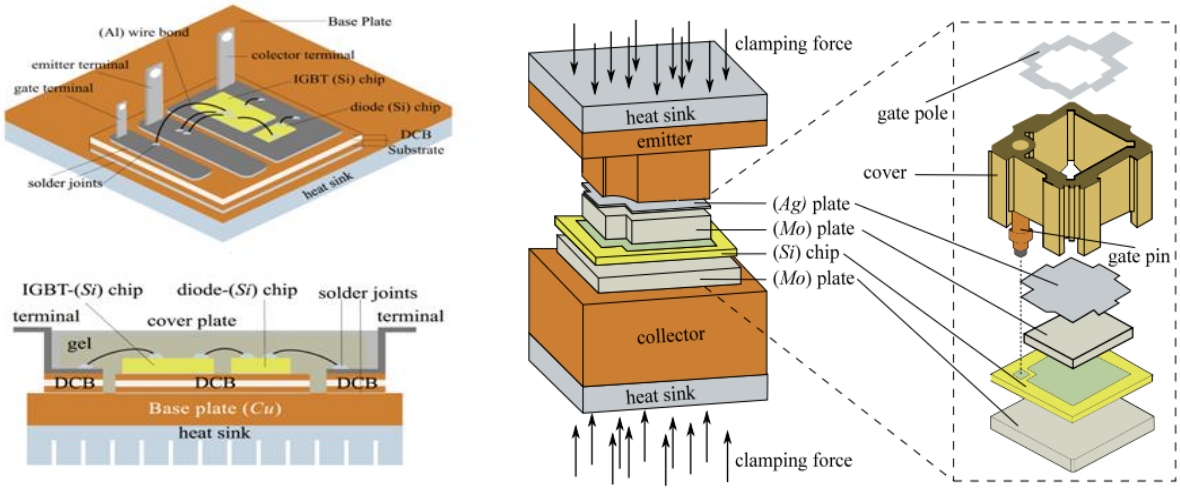


Figure I.18: MMC faults

I.6.1. IGBT Failure Mechanisms

Insulated Gate Bipolar Transistors (IGBTs) are widely used in power electronic converters thanks to their high efficiency and fast switching capability. However, their reliability is challenged by two main failure mechanisms: open-circuit failures (OCFs) and short-circuit failures (SCFs). Understanding these modes is crucial for developing robust and fault-tolerant systems, especially in high-power applications such as Modular Multilevel Converters (MMCs).

IGBTs are typically available in two packaging types: wire-bonded modules (Figure I.19.a) and press-pack modules (Figure I.19.b) Each type has distinct thermal, electrical, and mechanical properties that strongly influence its failure behavior under operational stress [67–69].



a) b)

Figure.I.19: IGBT types [71]: a) wire-bonded modules, b) press-pack modules

The wire-bond IGBT module is composed of a copper (Cu) base plate, direct copper bond (DCB) substrates, silicon (Si) chips, and aluminum wire bonds that connect the chips to external terminals. Silicone gel encapsulation provides electrical insulation, protects against moisture, and minimizes partial discharges. However, wire-bond modules are prone to fatigue-related failures such as bond wire lift-off and solder joint cracking. These issues mainly arise from the mismatch

in thermal expansion coefficients between Si and Al, which induces cyclic mechanical stress especially under frequent load variations and temperature fluctuations [69].

In contrast, the press-pack IGBT module eliminates wire bonds entirely. It uses mechanical clamping between copper electrodes, sandwiching layers of molybdenum (Mo), silver (Ag), and the Si chip. This structure ensures uniform clamping pressure and superior thermal conduction through Mo layers and copper plates, while a flexible silicon shim accommodates mechanical deformations. As a result, press-pack modules effectively overcome wire-bond lift-off problems and offer higher reliability in demanding high-power applications [68,69].

Table.I.4: Main Characteristics of Wire-Bond IGBT Module VS press-pack IGBT

Feature	Wire-bond IGBT	Press-pack IGBT
Power Handling Density	Offers average power density	Capable of delivering high power density
Operational Reliability	Provides moderate reliability	Exhibits superior reliability
Economic Cost	Relatively cost-effective	Typically, more expensive
Main Fault Behavior	Tends to develop open-circuit faults	Prone to short-circuit faults
Heat Dissipation Capacity	Has medium thermal resistance	Features low thermal resistance

A) Open-circuit fault (OCF)

Open-circuit failures (OCFs) in IGBTs occur when the device cannot turn ON despite a gate signal. In wire-bonded modules, the main cause is bond wire lift-off from thermal fatigue due to load and temperature cycling. Advanced interconnection methods such as sintered silver and transient liquid phase bonding have been proposed to address this issue [70,71]. Another major cause is gate driver failure, often triggered by over-voltage, over-current, or insulation breakdown. Since gate drivers are complex and sensitive, they are among the most failure-prone components in converters [72,73].

Table.I.5 .MMC Under OCF

The state of the SM	**The sign of the arm current**	**The SM output voltage**		
		Normal operation	Upper switch OC fault	Lower switch OC fault
bypassed	+	V_C	V_C	V_C
	-	V_C	0	V_C
Inserted	+	0	0	V_C
	-	0	0	0

While OCFs rarely cause immediate converter shutdown, they can degrade performance, create unbalanced operation, and increase stress on healthy components, potentially leading to secondary faults. Table.I.5 summarizes system behavior under OCFs.

B) Short-circuit fault (SCF)

Short-circuit failures (SCFs) occur when an IGBT becomes permanently conductive, losing its blocking capability. In MMCs, this can generate dangerously high currents, especially if the complementary switch in the same leg is ON while the submodule capacitor is charged, potentially damaging the submodule or the entire converter arm [70].

SCFs are mainly triggered by thermal overstress, where excessive fault currents (e.g., shoot-through) raise the junction temperature beyond ~250 °C, leading to thermal runaway and die destruction. Voltage overstress may also cause avalanche breakdown, while other factors such as latch-up, secondary breakdown, energy shocks, or gate drive issues can contribute [70,71]. Although latch-up is less common in modern trench-gate IGBTs, SCFs remain one of the most destructive failure modes.

Table.I.6 summarizes system behavior under SCFs

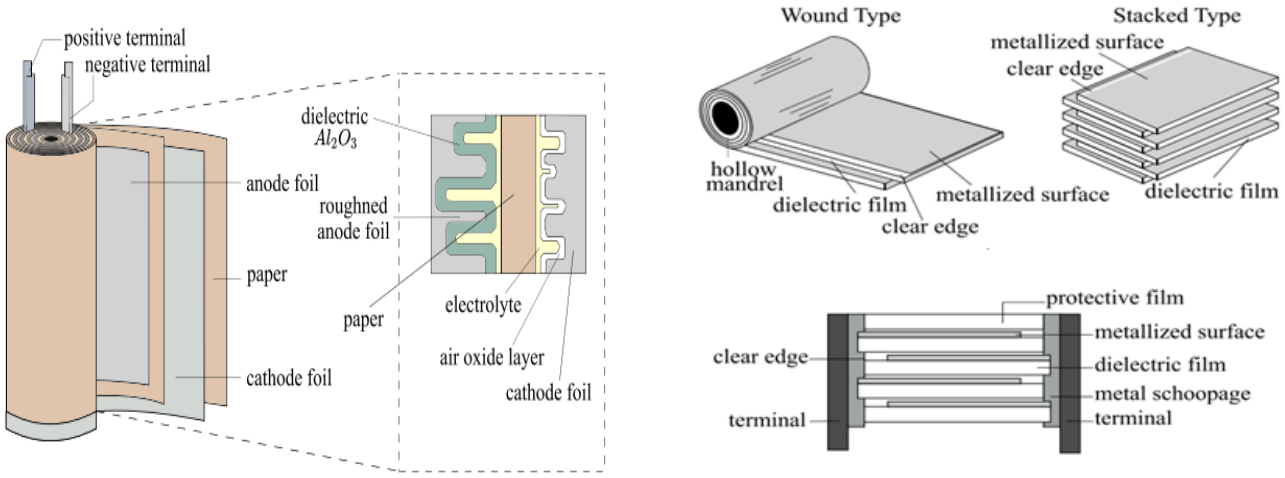
Table.I.6.MMC Under SCF

The state of the SM	The sign of the arm current	The SM output voltage		
		Normal operation	Upper switch SC fault	Lower switch SC fault
bypassed	+	V_C	V_C	0
	-	V_C	V_C	0
Inserted	+	0	V_C	0
	-	0	V_C	0

I.6.2. capacitor failure mechanisms

Power capacitors are the second most critical components in power electronic systems and serve as the central energy storage elements within each submodule of a Modular Multilevel Converter (MMC)[72]. Their performance directly influences key operational parameters such as voltage stability, current ripple, and energy buffering, making them essential to the reliable functioning of the converter. Faults in these capacitorswhether due to aging, dielectric failure, or thermal stresscan significantly compromise the overall stability and reliability of the MMC system. [71,73].

Two primary types of capacitors are commonly used in MMC applications: Aluminum Electrolytic Capacitors (Al-Caps) (Figure I.20.a) and Metallized Polypropylene Film Capacitors (MPPF-Caps) (Figure I.20.b). Al-Caps are polarized devices constructed from etched aluminum foil, paper separators, and an aluminum oxide dielectric layer. They provide high capacitance density but are more vulnerable to voltage surges and temperature variations [74,75].



a) b)

Figure I.20. capacitor types [71]: a) Al-electrolytic capacitors, b) MPPF capacitors.

In contrast, MPPF-Caps are non-polarized and feature a self-healing dielectric film, offering superior reliability and lower equivalent series resistance (ESR), which makes them particularly suitable for high-frequency operation and fault-prone environments. [76,77].

Capacitors in MMCs are vulnerable to failures from electrical overstress (over-voltage/current), thermal overload, mechanical stress, and aging. These factors lead to three main fault modes: open-circuit faults (OCFs) from dielectric breakdown or terminal detachment; short-circuit faults (SCFs) from severe dielectric failure causing high surge currents; and wear-out faults (WOFs) from aging, marked by reduced capacitance, higher ESR, and leakage current. Such degradation increases power losses and thermal stress, which can evolve into SCFs. If undetected, these faults compromise converter performance, stability, and safety, while also forcing higher IGBT switching frequency to maintain voltage balance, further stressing the system [78–80].

I.7. Fault Detection and Identification techniques (FDI)

Ensuring the stability and reliable operation of Modular Multilevel Converters (MMCs) relies heavily on timely and accurate fault detection and localization. In recent years, considerable research efforts have been dedicated to developing advanced diagnostic techniques to enhance the reliability, safety, and efficiency of MMC systems., these diagnostic methods can be broadly categorized into three main groups: model-based approaches**,** signal processing-based approaches**,** and artificial intelligence-based approaches.

I.7.1 model-based approaches

Model-based fault detection methods rely on accurate mathematical models of converters to detect deviations between expected and actual behavior (Figure I.21). Two main strategies are common observer-based approaches (e.g., SMO, ESO), which estimate system states and use residuals to identify faults [5–8], and signal estimation methods, which monitor key variables like capacitor voltages or arm currents and compare them with measured values. Kalman filter-based techniques, for example, can localize faults by detecting voltage deviations [81], while extensions also address sensor and device failures [82].

These methods provide high detection accuracy without significant hardware redundancy, making them attractive for MMCs. However, their reliability depends heavily on model accuracy and proper observer tuning, as inaccuracies can cause false alarms or missed detections. Overall, model-based approaches remain an effective and widely studied solution for balancing diagnostic performance with hardware requirements.

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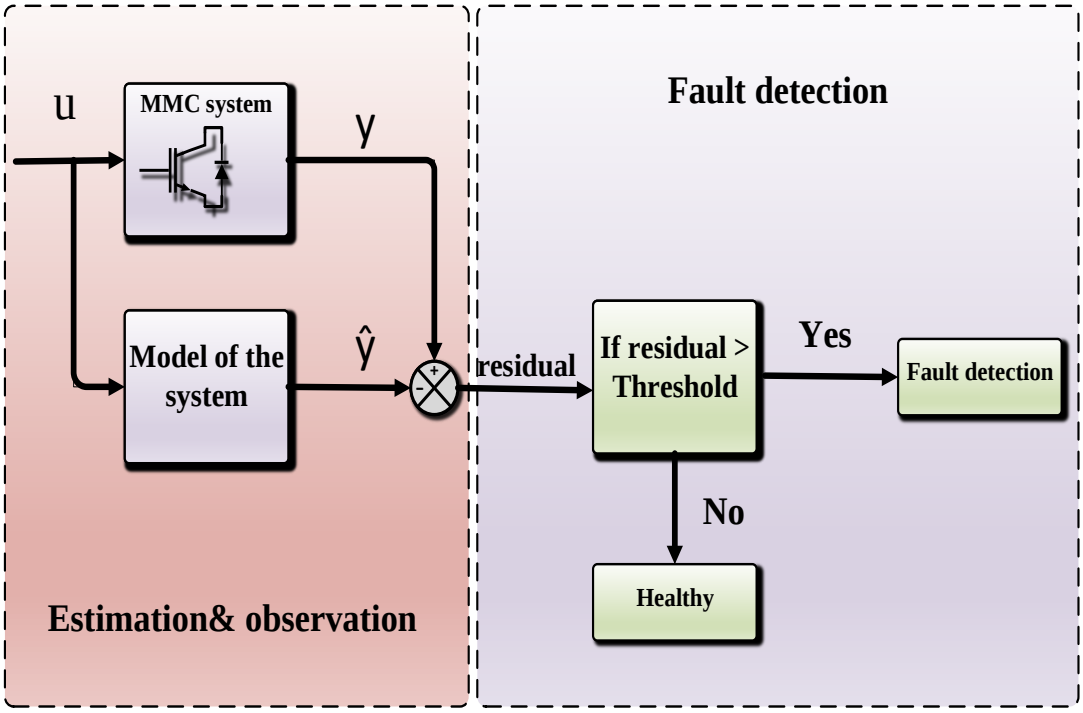


Figure I.21: structure of model-based approaches

I.7.2. signal processing -based approaches

Signal processing-based fault detection methods diagnose faults by analyzing measured electrical signals (voltages, currents) rather than relying on detailed system models (Figure I.22). Techniques range from simple strategies, such as average load current monitoring [83] or logical operations on voltage and current signals [9], to more advanced tools like the signal ring theorem [84], Boolean logic [85], or wavelet transforms for transient analysis [10]. Methods that reduce sensor requirements such as using synthesized capacitor voltages [87] or optimized sensor placement [86] have also been proposed. These approaches are flexible and effective for both transient and steady-state faults, offering valuable diagnostic capabilities without extra hardware.

However, their performance can be affected by noise, parameter variations, and system complexity, and they still rely on accurate knowledge of expected signal behavior. Overall, they provide a practical alternative where redundant sensors or complex observers are not feasible.

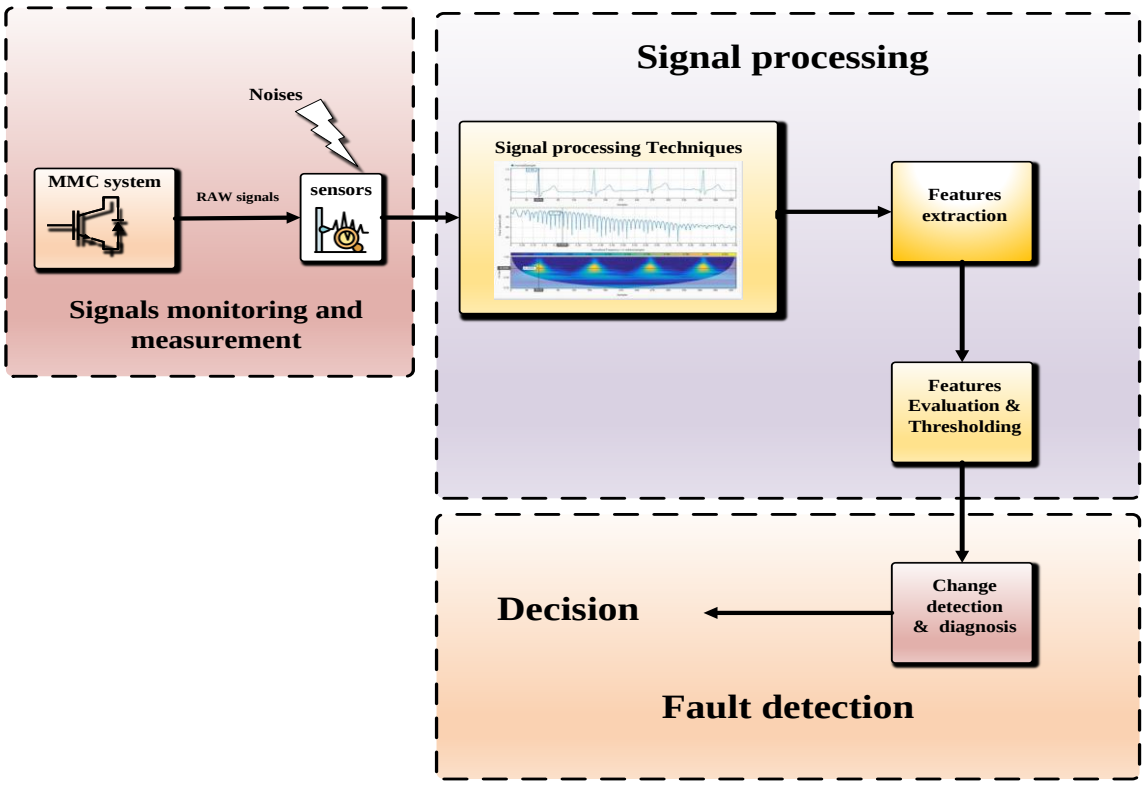


Figure I.22: structure of signal processing- based approaches

I.7.3. Artificial Intelligence-based approaches

AI-based fault detection methods rely on machine learning and data-driven algorithms trained on historical fault data to identify and localize faults without detailed physical models (Figure I.23). They can capture nonlinear relationships in the data, offering high adaptability and diagnostic accuracy.

Several techniques have been proposed for MMCs. SVMs classify and locate faults using three-phase current measurements [88], while multi-class SVMs identify shorted switches from extracted features [11]. Hybrid methods combine AI with signal processing, such as wavelet-based ANFIS for short-circuit detection [89] or RNNs with wavelet analysis for improved accuracy [90]. More advanced approaches include mixed-kernel support tensor machines

(MKSTM) optimized by PCA and quantum genetic algorithms [91]. ANNs have been applied for open-circuit fault classification [92], while deep learning models such as LSTM networks [93] capture temporal dependencies in time-series data. Adaptive 1D CNNs [94] go further by eliminating separate feature extraction, simplifying the diagnostic process.

AI-based methods stand out for their flexibility and ability to generalize across operating conditions, unlike model-based or signal-processing methods that rely on detailed models or extra hardware. However, they require large, representative datasets, and their performance is sensitive to data quality. Overall, AI offers a powerful and practical approach for fault detection in MMCs, balancing diagnostic accuracy with reduced hardware complexity.

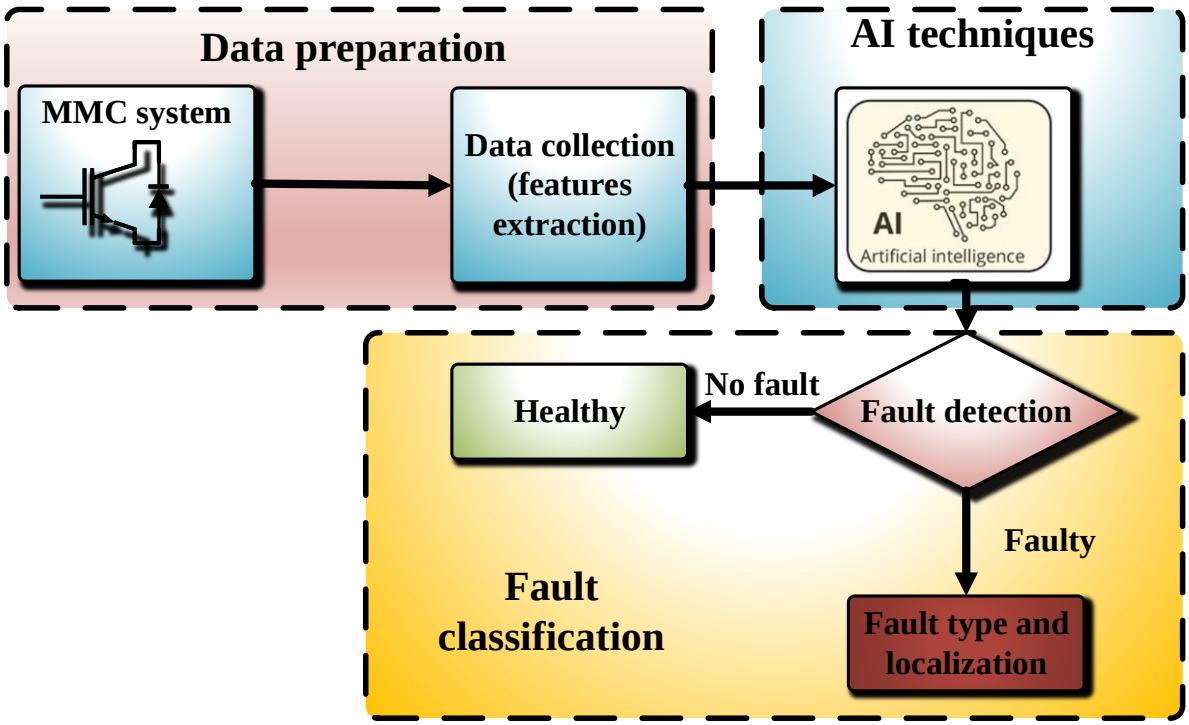


Figure I.23: structure of AI-based approaches

I.8. conclusion

This chapter has reviewed Modular Multilevel Converters (MMCs), covering their topologies, operating principles, modeling, modulation, and control strategies. Reliability challenges were addressed by discussing common faults such as open-circuit, short-circuit, and capacitor failures, along with their effects on system performance. Fault detection and isolation techniques were also summarized, including model-based, signal processing-based, and AI-based methods.

Overall, this background provides the necessary foundation for developing advanced monitoring, diagnostic, and fault-tolerant strategies, which form the focus of the following chapters.

Chapter II

Intelligent Strategies for Open-Circuit Fault Diagnosis in MMCs

II.1. Introduction

Open-circuit faults in submodules represent one of the most common failure modes in MMCs. Several diagnostic techniques have been proposed in the literature to address this issue [5], [8]. However, the majority of existing studies concentrate exclusively on open-circuit faults occurring in the IGBT, while neglecting the potential faults involving the anti-parallel diode [87], [91], [92].

To address this limitation, this chapter presents fault detection and localization strategies capable of monitoring the entire switching device, including both the IGBT and its anti-parallel diode. Two intelligent diagnostic approaches are introduced. The first approach employs an Artificial Neural Network (ANN) for detecting IGBT open-circuit faults. The second approach integrates the Discrete Wavelet Transform (DWT) with Fuzzy Logic to detect open-circuit faults in both the IGBT and diode. These methods are comprehensively discussed and validated through MATLAB/Simulink simulations of a single-phase MMC under various fault conditions. The obtained results confirm that the proposed techniques are fast, accurate, and reliable for detecting and localizing open-circuit faults in MMCs.

II.2. Open-Circuit Fault Characteristics and Impact

IGBTs are exposed to several failures, particularly open-circuit faults (OCFs). An OCF interrupts the current flow, which can cause several issues such as unbalanced capacitor voltages, reduced power output, and distorted waveforms. In severe cases, it may lead to converter malfunction. Therefore, this section presents the main characteristics of OCFs and their impact on the operation of the MMC. [91]

II.2.1. Characteristics of OCF

As explained in Section I.3.1, the half-bridge submodule (SM) includes two IGBTs, each paired with an antiparallel diode. The most common open-circuit faults in these switches are:

- S1 fault (open IGBT in the upper switch)
- S2 fault (open IGBT in the lower switch)

In these cases, the diodes remain unaffected, as shown in Figure.II.1.a.

However, a more severe type of fault can also occur when both the IGBT and its associated diode become open-circuited. This fault can happen in:

- Switch 1 (IGBT + diode)
- Switch 2 (IGBT + diode)
- Or in the electrical connections around them, as illustrated in Figure.II.1.b.

Therefore, open-circuit faults can be classified into two types:

1. Faults affecting only the IGBT, with the diode remaining functional,
2. Faults affecting both the IGBT and its associated diode.

In this chapter, both fault types are analyzed and detection methods are proposed for each.

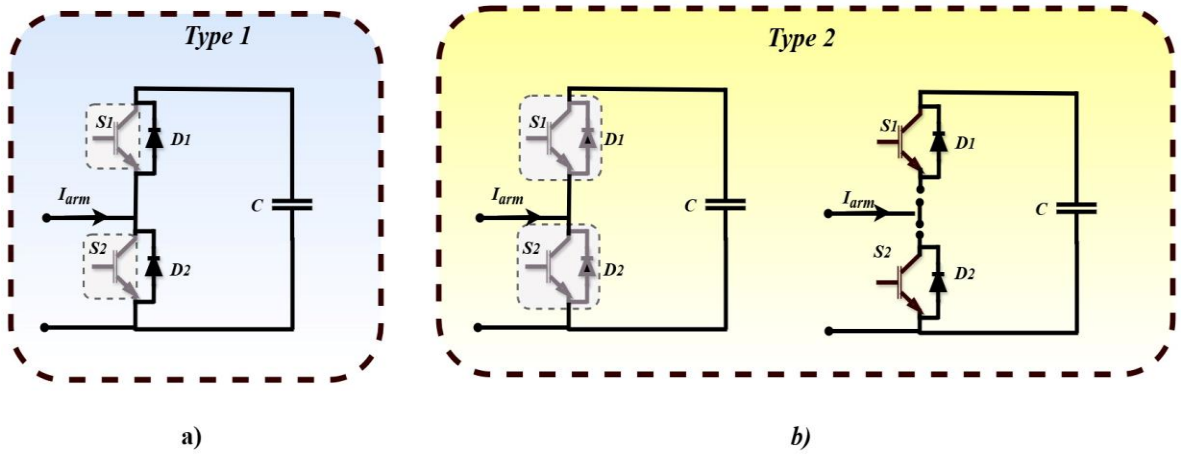


Figure.II.1 open circuit faults , a) type 1 OCF , b) type 2 OFC

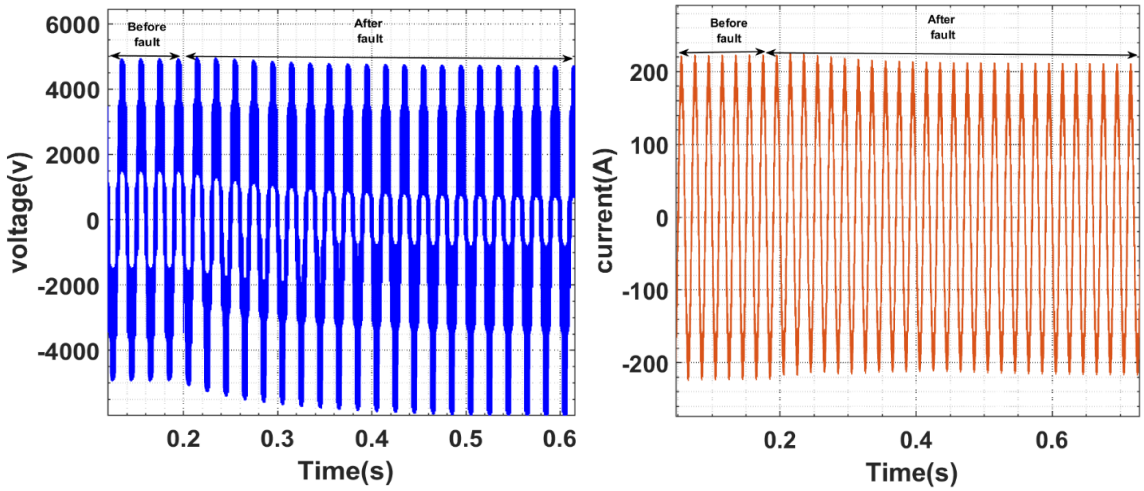
II.2.2. Impact of OCF

To evaluate the impact of open-circuit faults (OCFs) on the reliability and performance of the Modular Multilevel Converter (MMC), various fault scenarios were introduced and analyzed using MATLAB/Simulink. These simulations aim to replicate realistic fault conditions occurring within IGBT switches of MMC submodules and assess their effect on system-level parameters.

In the simulation setup, different scenarios were applied, including:

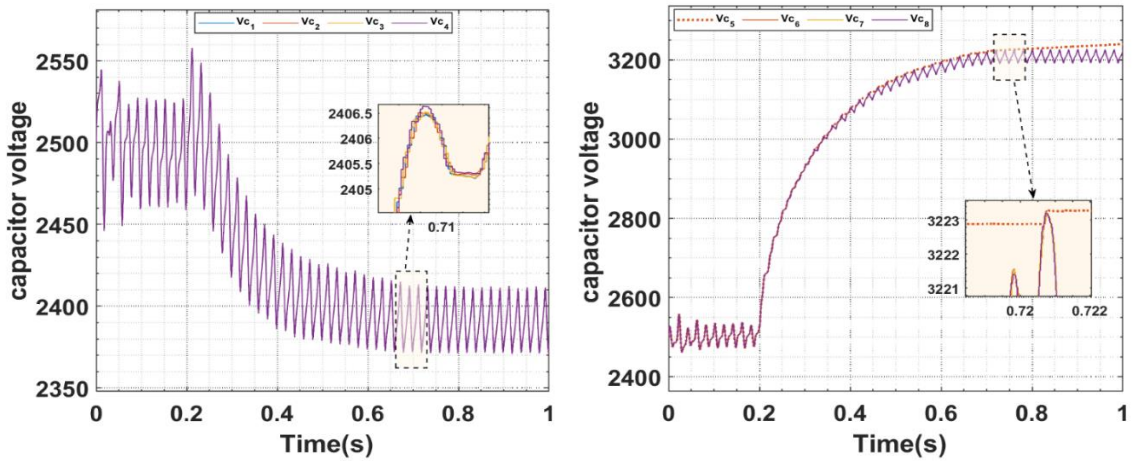
- Lower IGBT open-circuit fault, at (t = 0.2 s) in SM2
- Upper IGBT open-circuit fault, at (t = 0.2 s) in SM5
- switch 1(upper IGBT+ diode) open-circuit fault, at (t = 0.2 s) in SM1
- switch 2 (lower IGBT+ diode) open-circuit faults, at (t = 0.2 s) in SM1

A) Impact of type 1 OCF:



a) b)

Figure.II. 2: a) output voltage under upper IGBT OCF, b) output current under upper IGBT OCF

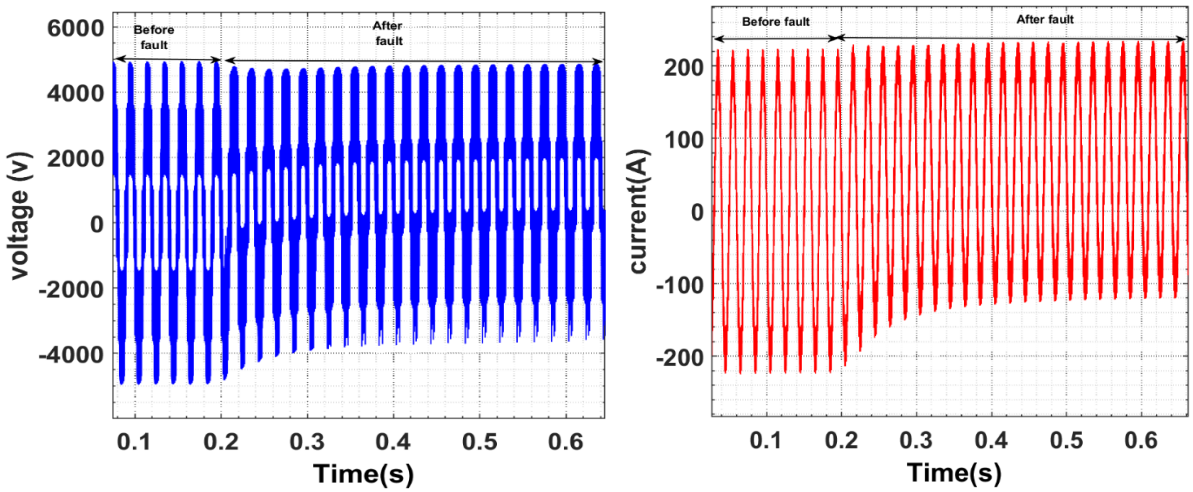


a) b)

Figure.II. 3: capacitor voltage under upper IGBT OCF. a) upper arm, b) lower arm

In this section, the impact of IGBT open-circuit faults on the MMC system is analyzed. Figure.II.2 and 3 illustrate the effects of an open-circuit fault in the upper IGBT, while Figure.II.4 and 5 show the impact of a fault in the lower IGBT.

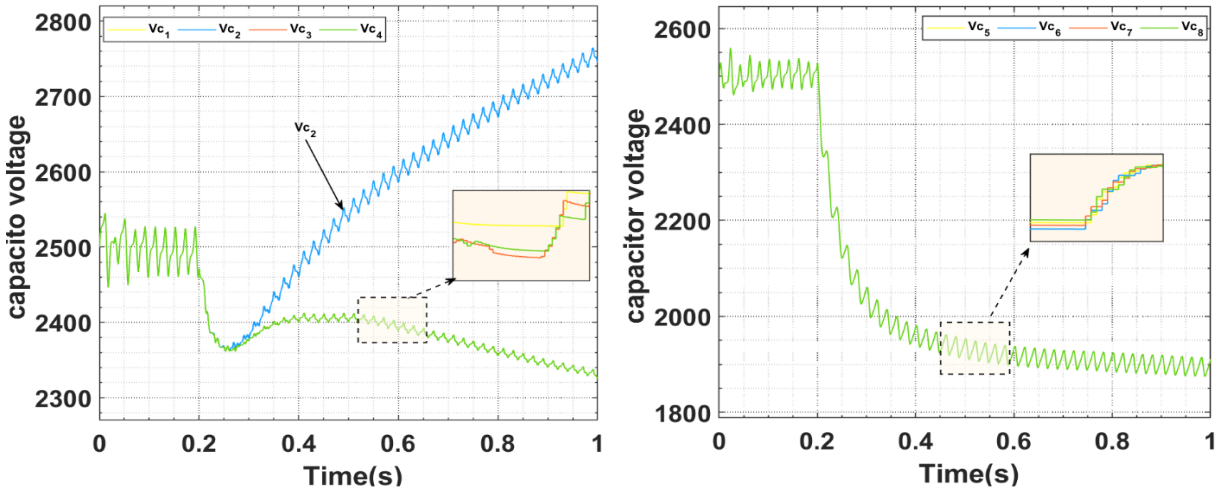
When an upper IGBT fault occurs at $t = 0.2\ s$, the output voltage and current (Figure.II. 2(a), 2(b)) remain largely unaffected, showing minimal system-level disturbance. However, the capacitor voltages experience clear distortions. As shown in Figure.II. 3(a), upper-arm capacitor voltages decrease due to the loss of the charging path under the open-circuit condition, while Figure.II. 3(b) indicates an increase in the lower-arm voltages since proper discharging is prevented. Submodule 5 exhibits the most pronounced overvoltage, directly linked to the faulty IGBT, which disrupts voltage balancing across the submodules.



a) b)

Figure.II. 4: a) output voltage under lower IGBT OCF, b) output current under lower IGBT OCF

For a lower IGBT fault, the system response differs significantly from the upper IGBT case. As shown in Figures.II.4(a) and 4(b), the output voltage and current waveforms display clear distortions due to current path interruption during parts of the switching cycle, reducing effective power transfer.



(a) (b)

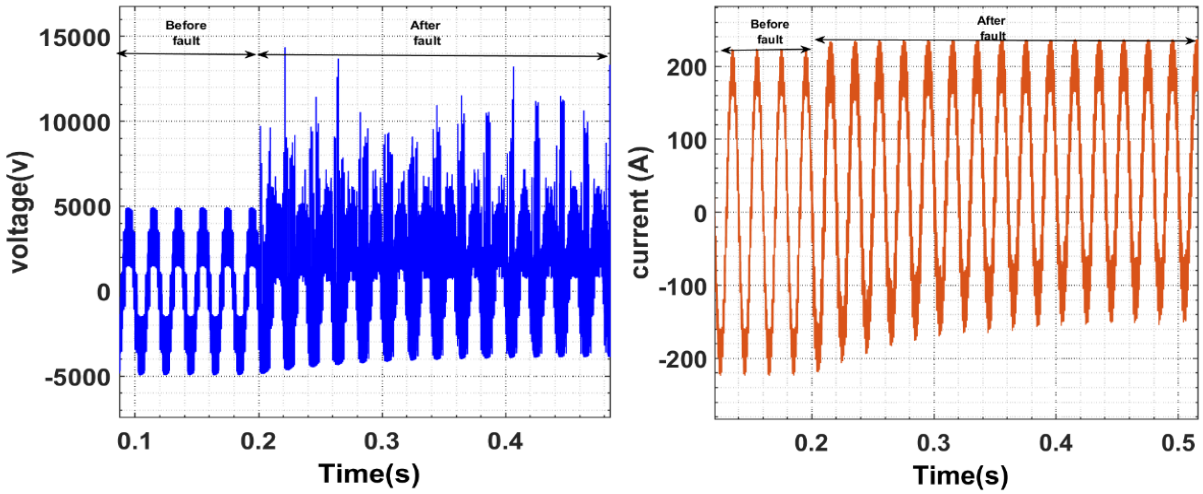
Figure.II. 5: capacitor voltage under lower IGBT OCF. A) upper arm, b) lower arm

The fault in submodule 2 directly affects capacitor voltage Vc2, which rises sharply after t = 0.2 s since the capacitor can no longer discharge during the negative current cycle (Figures.II.5. a) . In contrast, the healthy submodules discharge normally, causing their voltages to decrease (Figures.II.5. b). This divergence in capacitor behavior highlights the imbalance introduced by the fault, making it a reliable indicator for fault detection and localization.

B) Impact of type 2 OCF:

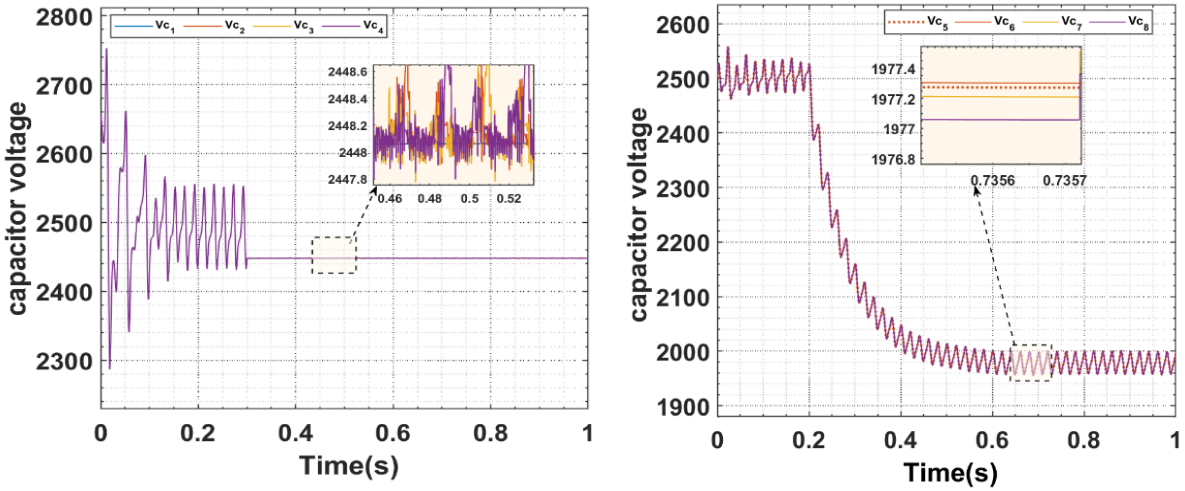
The impact of fault type 2, involving both the IGBT and its anti-parallel diode, is analyzed in this section. Figure.II. 6 and 7 illustrate the effects of a fault in Switch 1 on the MMC system, whereas Figure.II. 8 and 9 present the corresponding impact when the fault occurs in Switch 2.

As shown in Figure.II. 6(a) and 6(b), both the output voltage and current waveforms exhibit significant distortion following the occurrence of a fault in Switch 1. This highlights the substantial impact of fault type 2 on the overall system performance. In contrast, fault type 1 results in no noticeable changes in the output waveforms, indicating a minimal effect on the system's operation.



a) b)

Figure.II. 6:a) output voltage under switch 1 fault, b) output current under switch 1



a) b)

Figure.II. 7 capacitor voltage under switch 1 fault. a) upper arm, b) lower arm

Furthermore, Figure.II. 7(a) illustrates the capacitor voltages of the upper arm (VC1 to VC4). After the fault occurs, the capacitor voltages remain at their respective levels but lose their voltage balancing. The voltages stay fixed, indicating that the fault prevents normal charging and discharging operations within the affected submodules. Similarly, the lower arm capacitors exhibit noticeable deviations following the fault, as shown in Figure.II. 7(b), highlighting the disruptive impact of the fault on the voltage balancing and energy distribution within the arm.

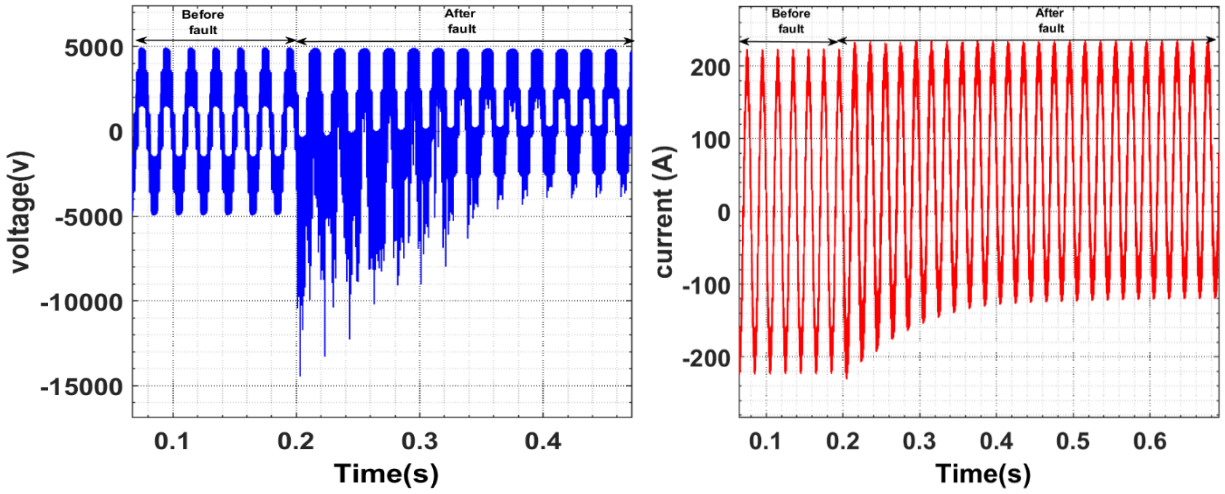
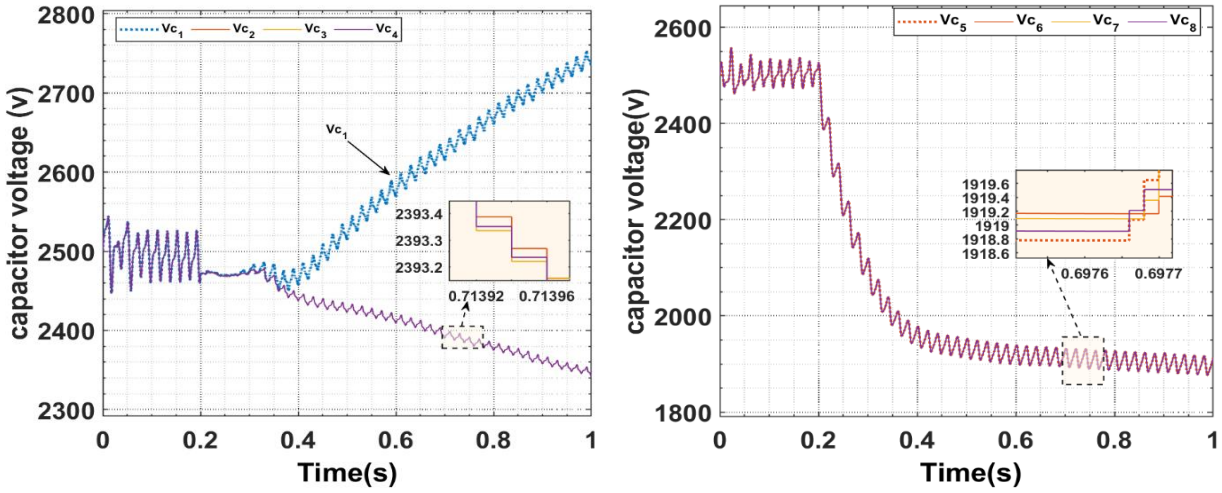


Figure.II. 8:output voltage under switch 2 fault, b) output current under switch 2



(a) (b)

Figure.II. 9: capacitor voltage under switch 2 fault. a) upper arm, b) lower arm

In the case of a fault in Switch 2, the system performance is also significantly affected; however, the waveform distortion differs from that observed in the fault of Switch 1. As shown in Figure.II.8(a) and 8(b), the output voltage and current waveforms exhibit distinct distortion patterns, indicating a different fault propagation behavior and its influence on the MMC system dynamics. In this instance, the upper arm capacitor voltage, presented in Figure.II.9(a), shows a clear increase in VC1, which corresponds to SM1the submodule where the fault occurs. This

behavior is similar to that observed in the case of fault type 1. The distinct rise in VC1 differentiates it from the other capacitor voltages, indicating the localized impact of the fault. Meanwhile, the lower arm capacitors exhibit a response comparable to that seen in the fault type 1 scenario, as illustrated in Figure.II.9(b).

II.3. Fault detection and localization of OFC type 1 based on STD-ANN

II.3.1. overview of the method

In this method, an artificial intelligence-based approach is proposed for the detection and localization of open-circuit faults of type 1. Specifically, an Artificial Neural Network (ANN) is employed to carry out this task. To ensure accurate and reliable results, it is essential to first collect and prepare an appropriate dataset for training the model. Accordingly, the proposed methodology is structured into two main stages: the first stage focuses on data preparation, including fault simulation and feature extraction, while the second stage involves training the neural network using the prepared dataset. This process is illustrated in Figure.II. 10.

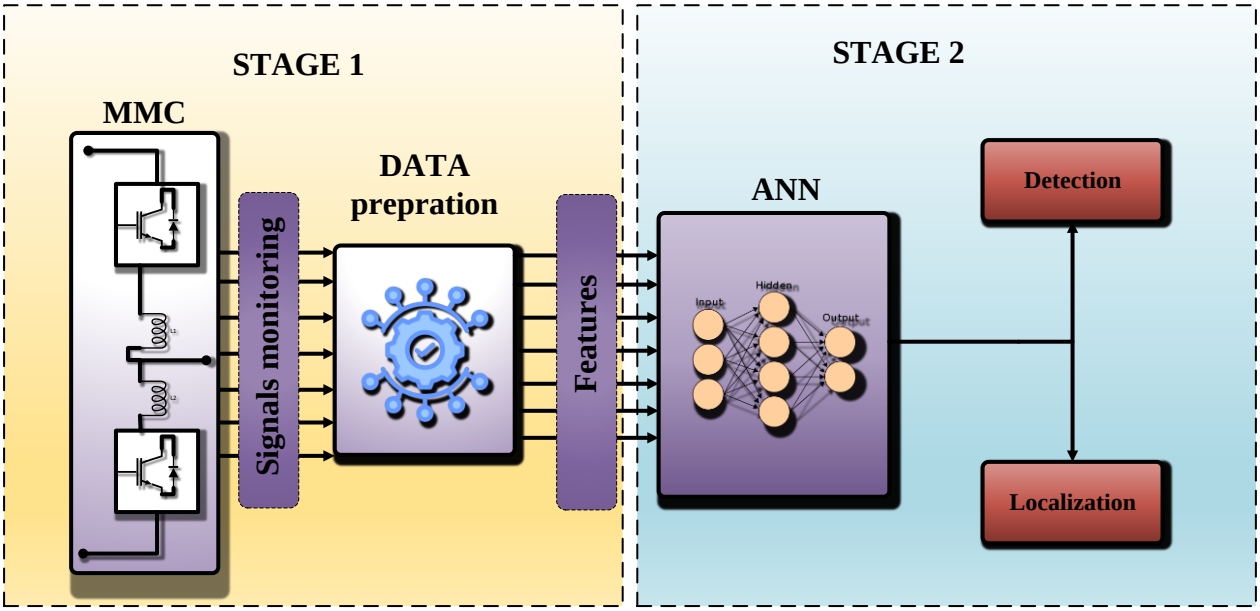


Figure.II. 10:structure of the proposed method based on STD-ANN

II.3.1.1. Data preparation

A well-prepared dataset is essential for training reliable AI-based fault diagnosis systems, as its quality and diversity directly affect detection and localization accuracy [95]. In this study, capacitor voltage is used as the primary fault indicator, since Figures. 4 and 6 show clear deviations

under different fault scenarios abnormal increases or decreases in certain submodules provide distinct fault signatures. To extract meaningful information, feature extraction is applied using the standard deviation (STD), which quantifies voltage variation within a time window. As a sensitive measure of deviations from the mean, STD effectively highlights abnormalities and fluctuations caused by faults. [96].

The standard deviation is calculated using the following equation:

$$STD = \sqrt{\frac{\sum_{i=1}^{n} (x_i - \overline{x_i})^2}{n-1}} \qquad \text{II.1}$$

Where:

x_i : are the data points, $\overline{x_i}$: is the mean of the data, n: is the number of data points,

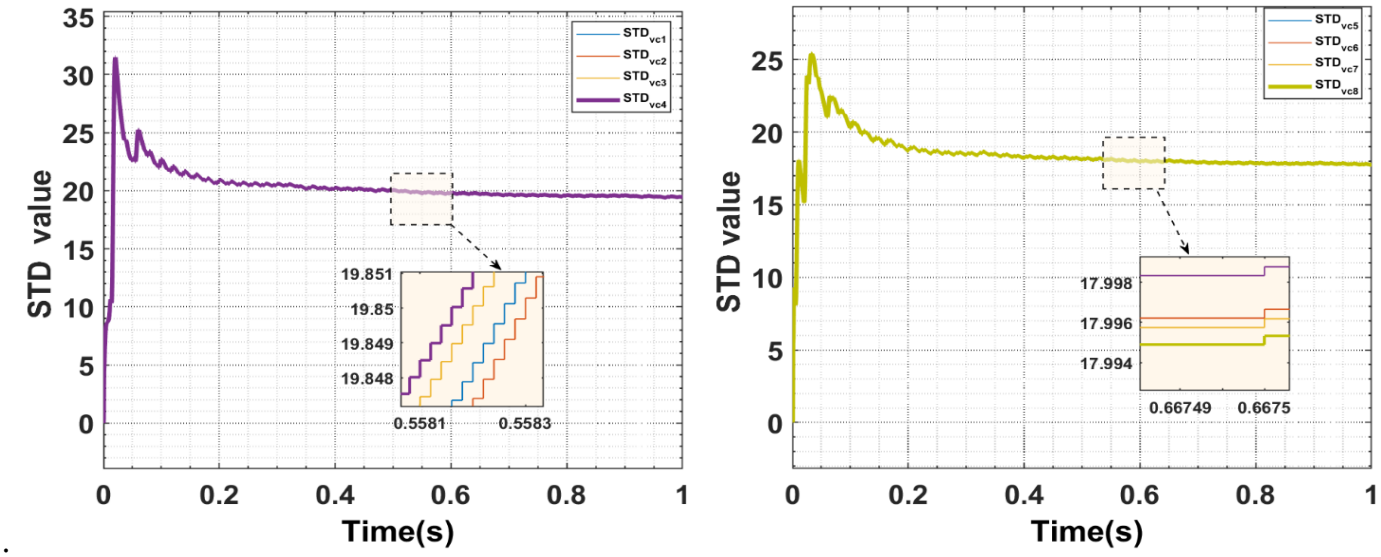
the mean value it can be obtained as follow:

$$\overline{X_i} = \frac{1}{n} \sum_{i=1}^{n} x_i \qquad \text{II.2}$$

The use of standard deviation in this context is motivated by its ability to highlight dynamic changes in the signal that may not be obvious through visual inspection alone. In fault conditions, the statistical distribution of the capacitor voltage becomes irregular, and the standard deviation effectively captures these variations. This makes it a reliable and computationally efficient feature for feeding into the ANN during the training and classification phases.

A) Healthy case (no fault)

Figure.II. 11. presents the standard deviation of the capacitor voltages The standard deviations of both upper and lower arm capacitor voltages stabilize after the transient period, showing nearly identical values (≈20 for the upper arm and ≈18 for the lower arm). This uniform behavior across all submodules confirms that the MMC is operating in a healthy, fault-free state.



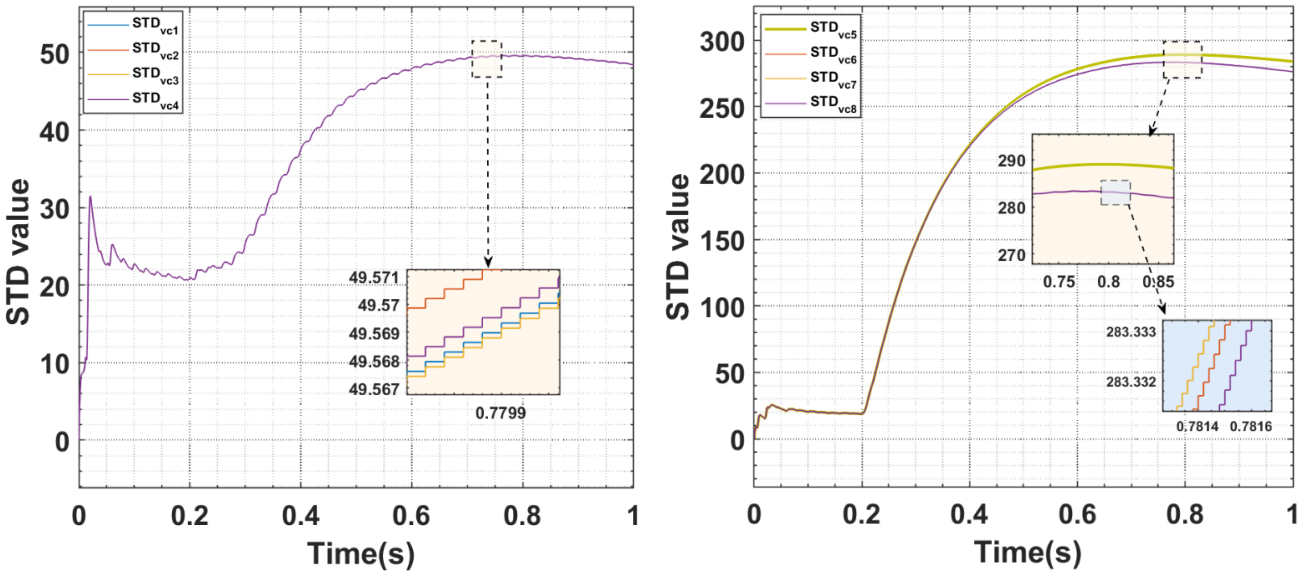
(a) (b)

Figure.II. 11: the standard deviation under healthy conditions ;(a upper arm; (b lower arm

B) Fault of upper IGBT

In the case of an upper IGBT open-circuit fault, Figure.II. 12(a) shows the standard deviation of the upper arm capacitor voltages (VC1 to VC4). It can be observed that all STD values begin to increase simultaneously after the fault occurs at t = 0.2 s, reaching approximately 50. This value is significantly higher than the normal operating value of around 20, and this abnormal rise in STD confirms the presence of a fault.

On the other hand, Figure.II. 12(b) presents the standard deviation of the lower arm capacitor voltages (VC5 to VC8). Similarly, all STD values start to increase after the fault occurs. However, in this case, the STD value of VC5 is noticeably higher, reaching around 285 compared to the others, which stabilize around 275. Since the fault is located in the upper IGBT of Submodule 5, this result strongly supports the use of standard deviation as a reliable fault localization indicator.



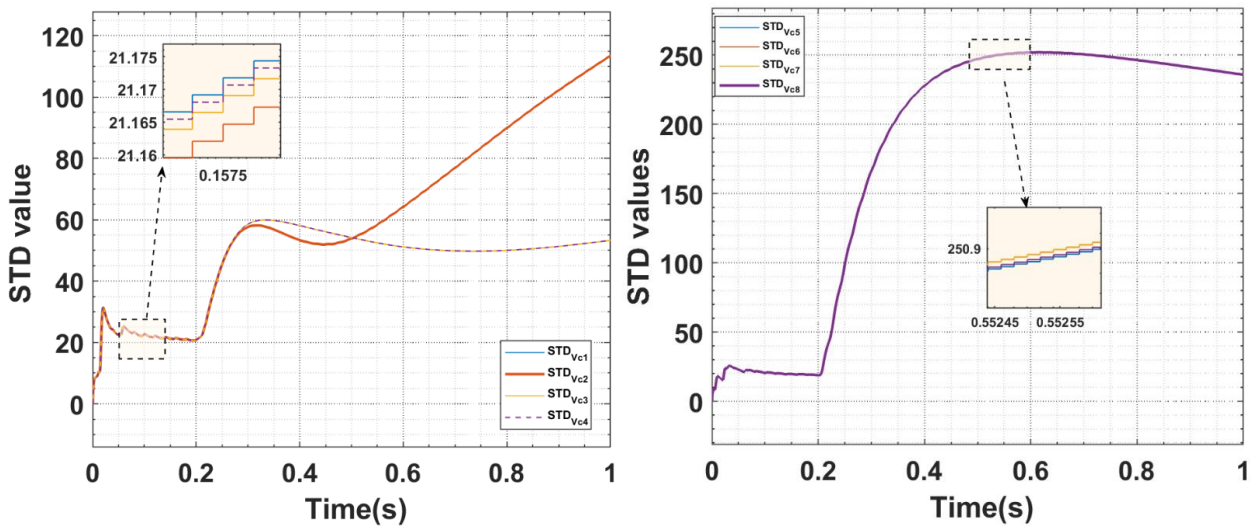
(a) (b)

Figure.II. 12: the standard deviation under Upper IGBT fault ;(a upper arm; (b lower arm

C) Fault of lower IGBT

An OFC was introduced in the lower IGBT of Submodule 2. Figure.II. 13(a) presents the STD of the capacitors voltages in the upper arm voltages (VC1 to VC4). Prior to the fault, all STD values remain stable indicating normal operation. At the moment the fault occurs, a sharp deviation is observed in the STD values of all four capacitors. While VC1, VC3, and VC4 stabilize around a value of 50, the STD value of VC2 rises significantly, exceeding 100. This distinct behavior confirms the presence of a fault in Submodule 2 and demonstrates that the standard deviation is an effective and sensitive indicator for fault detection and localization.

In contrast, Figure.II. 13(b) shows the standard deviation of the lower arm capacitor voltages. After the fault occurs, all STD values increase slightly but in a nearly identical manner. This u indicates that there is no fault in the lower arm, reinforcing the conclusion that the fault is isolated to the upper arm.



a) b)

Figure.II. 13: the standard deviation under lower IGBT fault ;(a upper arm; (b lower arm

The standard deviation method proved effective in capturing signal variations for fault detection. To improve feature diversity and dataset robustness, data were collected under different conditions, including varying resistive loads and fault scenarios at multiple time intervals. This approach generated a comprehensive dataset, enabling effective ANN training and enhancing its generalization across diverse operating conditions.

III.3.1.2. Artificial neural network model

After collecting the necessary dataset using the standard deviation-based feature extraction method under various fault scenarios and loading conditions, an ANN model was developed to detect and localize faults in the MMC. This section provides a theoretical overview of ANNs, followed by the implementation details relevant to the present work.

A) Theoretical Background of Artificial Neural Networks

ANNs are machine learning models that mimic the neural architecture and processing mechanisms of the human brain, illustrated in Figure II.14 [97]. These models are composed of interconnected processing elements, known as neurons, which are organized in layers and are capable of learning complex, non-linear relationships from data. Due to their powerful approximation capabilities, ANNs have been successfully applied in various engineering fields,

including pattern recognition, classification, system identification, and fault diagnosis. [98]. In the context of power electronic systems such as Modular Multilevel Converters (MMCs), ANNs offer a data-driven approach for detecting and localizing faults, particularly when the system dynamics are too complex to be modeled analytically.

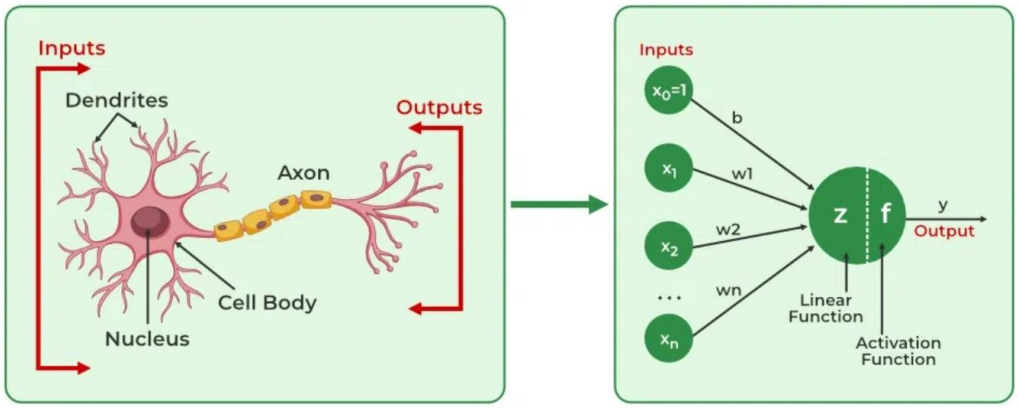


Figure.II. 14 Human neuron VS artificial neuron

An ANN typically consists of three main types of layers: the input layer, one or more hidden layers, and the output layer. Each layer comprises neurons that receive signals, perform a weighted summation, and apply a nonlinear activation function. [97]. [98].

Mathematically, the output of a single neuron can be expressed as:

$$y = f\left(\sum_{i=1}^{n} w_i x_i + b\right) \qquad \text{II.3}$$

where: x_i are the input features, w_i is the corresponding weight, b is the bias term, $f(\cdot)$ is the activation function (e.g., sigmoid, ReLU, or tanh).

The learning process in an ANN involves adjusting the weights and biases through a training algorithm such as backpropagation, typically using optimization methods like gradient descent. The aim is to minimize the loss function, which quantifies the error between the predicted output and the actual target. [98].

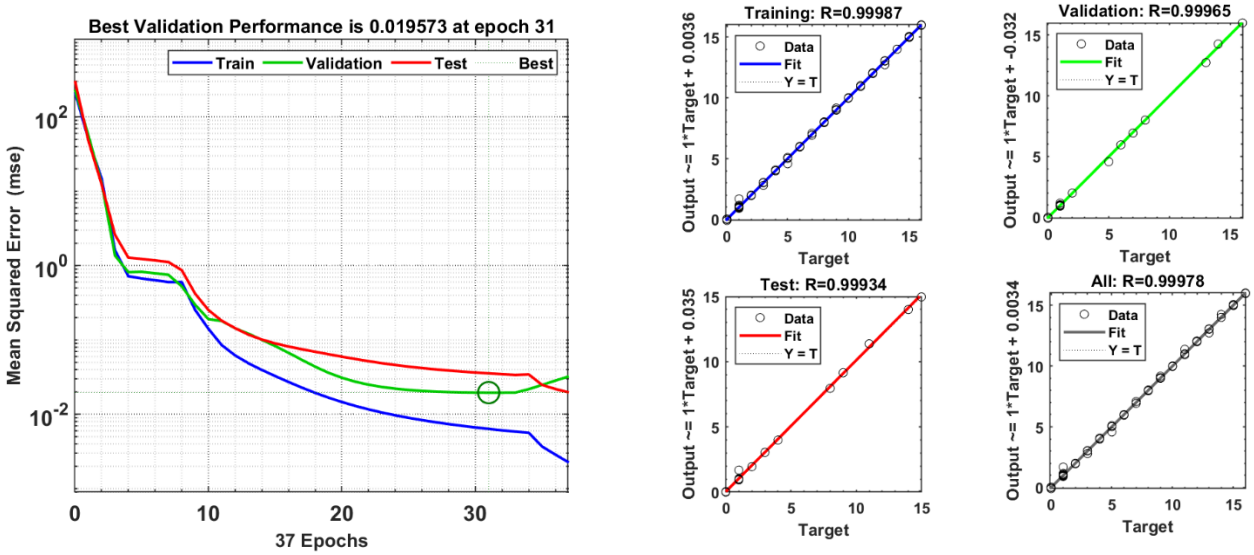
B) Implementation of ANN using in this work

In this work, an Artificial Neural Network (ANN) is employed as it provides a practical trade-off between accuracy, implementation simplicity, and computational efficiency. Coupled with standard deviation–based feature extraction, the ANN enables accurate and reliable fault detection and localization, making it suitable for real-time applications with limited processing capacity. The nonlinear layers in the ANN enhance its ability to capture and classify complex fault patterns effectively [99].

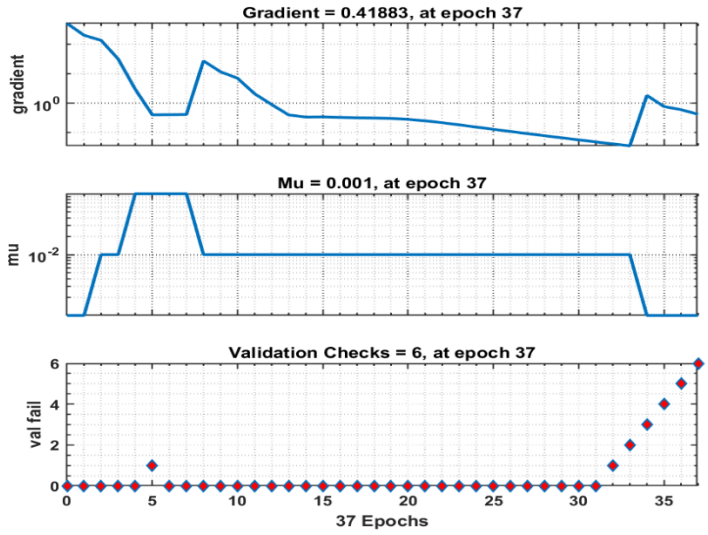
The adopted architecture, summarized in Table.II. 1, is a three-layer feedforward network with a single hidden layer of 25 neurons. A hyperbolic tangent sigmoid (TANSIG) activation function is used in the hidden layer to model nonlinear relationships. The Levenberg–Marquardt algorithm (TRAINLM) is selected for its fast convergence, with *learngdm* employed for weight updates. A hold-out validation strategy is applied to partition the dataset, preventing overfitting and ensuring robust generalization.

Table.II. 1 ANN model parameters

Parameter	Value/method
Number of layers	3
Input layer	8
Hidden layer	25
Output layer	2
Training function	Levenberg–Marquardt (TRAINLM)
Adaptation-learning function	Gradient Descent with Momentum (learngdm)
Transfer function	Hyperbolic Tangent Sigmoid (TANSIG)
Validation approach	Hold-Out Validation



a) b)



c)

Figure.II. 15 ANN evaluation: a) performance, b) regression, c) Training Progress

The ANN model was trained for 37 epochs, with the results summarized in Figure.II.15

- **(a) Regression plots** show strong correlations between predicted and actual values across all datasets, with regression coefficients close to 1 (e.g., R = 0.9993 for test data), confirming high prediction accuracy. (Figure.II.15. b)

- **(b) MSE curve** indicates that the best validation performance occurred at epoch 31 with a minimum MSE of 0.019573. Early stopping was applied thereafter to avoid overfitting. (Figure.II.15. a)
- **(c) Training parameters** illustrate the evolution of the gradient, learning rate, and validation checks. The gradient remained stable, and early stopping was triggered after 6 validation checks at epoch 37. (Figure.II.15.c)

The close alignment of training and validation losses, along with high regression values, demonstrates that the ANN achieved excellent generalization and robustness. These findings validate the proposed ANN architecture as suitable for real-time MMC fault detection and localization using statistical features such as standard deviation.

III.3.2 Results and discussion

This section analyzes the proposed method for fault detection and localization of Type 1 open-circuit faults in Insulated Gate Bipolar Transistors (IGBTs) within a Modular Multilevel Converter (MMC). The evaluation is performed using a MATLAB/Simulink model of a five-level MMC with four submodules (SMs) per arm. To assess the method's effectiveness, three representative scenarios are considered:

- Healthy operating condition (no fault),
- Upper IGBT open-circuit fault in Submodule 5 (SM5) at $t = 0.2\ s$,
- Lower IGBT open-circuit fault in Submodule 2 (SM2) at $t = 0.2\ s$.

Each submodule contains two IGBTs (upper and lower), and with eight submodules in total, the system can exhibit 16 possible fault cases in addition to the healthy case. Accordingly, the ANN is trained and tested to classify 17 conditions in total (16 faults + 1 healthy case).

The classification performance of the trained ANN model across these conditions is summarized in Table.II. 2, which presents the predicted outputs under different test scenarios.

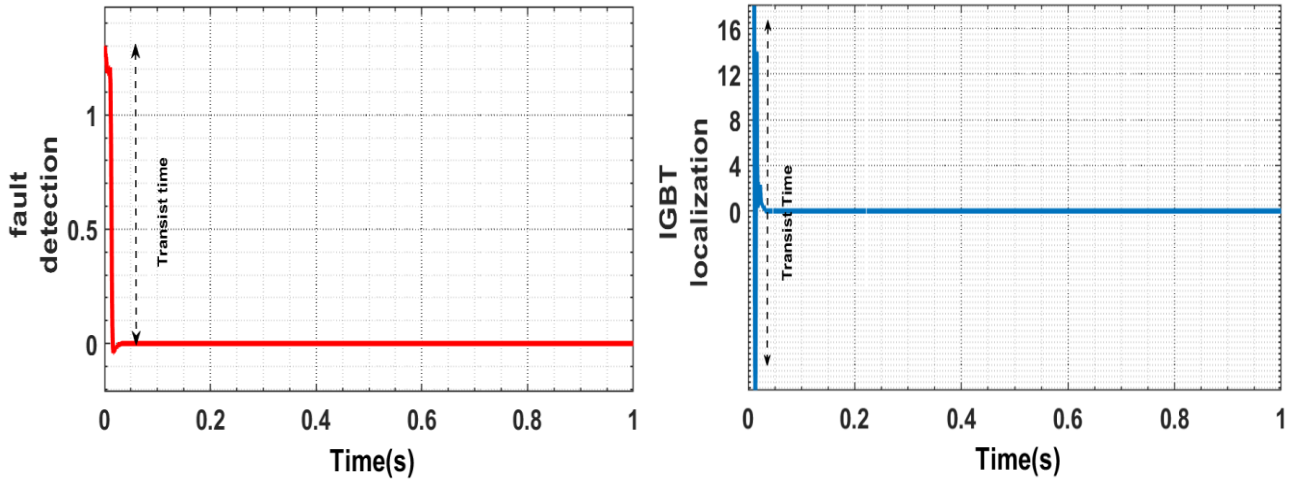
Table.II. 2 faults classification

Case	Detection	Localization
Healthy	0	0
$IGBT_1$	1	1
$IGBT_2$	1	2
$IGBT_3$	1	3
$IGBT_4$	1	4
$IGBT_5$	1	5
$IGBT_6$	1	6
$IGBT_7$	1	7
$IGBT_8$	1	8
$IGBT_9$	1	9
$IGBT_{10}$	1	10
$IGBT_{11}$	1	11
$IGBT_{12}$	1	12
$IGBT_{13}$	1	13
$IGBT_{14}$	1	14
$IGBT_{15}$	1	15
$IGBT_{16}$	1	16

III.3.2.1. healthy case (no fault)

As shown in Figure.II. 16(a)**,** the fault detection output remains consistently at zero throughout the entire simulation period (0–1 s), indicating the absence of any fault occurrence. A minor transient spike appears at the very beginning, which is attributed to initial system stabilization and is quickly damped, posing no diagnostic significance. In Figure.II. 16(b)**,** the IGBT localization output also remains constant at zero, indicating that no faulty component has been identified. This behavior confirms that the ANN does not produce false fault localization signals under healthy operating conditions.

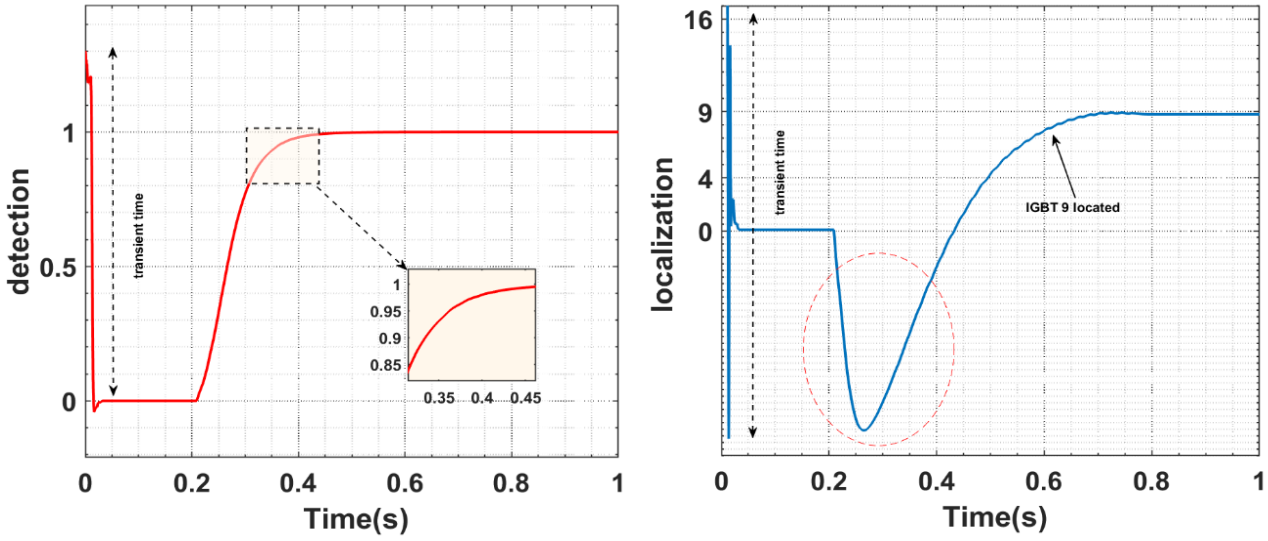
These results demonstrate the robustness and reliability of the ANN model in avoiding false positives. Moreover, the model's ability to maintain high precision under normal conditions is critical for real-world applications, ensuring that fault detection is both accurate and trustworthy.



(a) (b)

Figure.II. 16: ANN output under healthy case : a) fault detection signal , b) fault localization signal

III.3.2.2. Fault of type T1

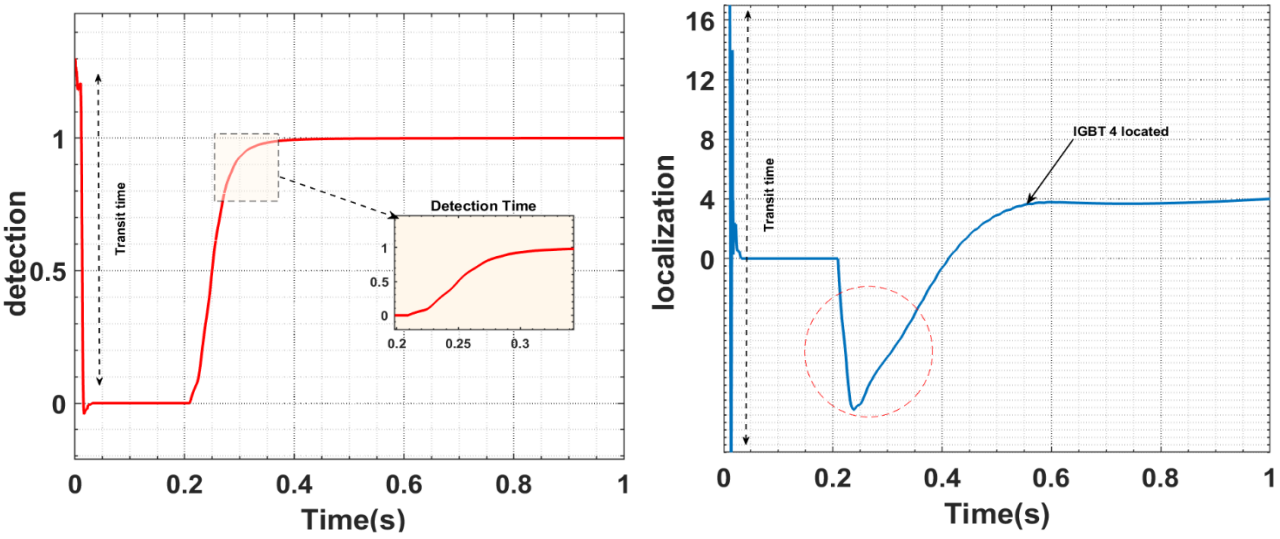


(a) (b)

Figure.II. 17: ANN output under T1 fault case : a) fault detection signal , b) fault localization signal

A fault is injected at approximately 0.2 s**,** followed by a clear and smooth rise in the detection signal, which gradually stabilizes at 1, indicating the successful detection of a fault. This transition reflects a detection delay of approximately 120 ms**,** as illustrated in the inset of Figure.II. 17(a)**.** Immediately after the fault inception, the ANN output exhibits a brief period of instability, as highlighted in the circled region of Figure.II. 17(b)**.** This transient fluctuation is attributed to the system's dynamic response during the initial transition phase and the ANN's temporary uncertainty, likely due to a mismatch between real-time input features and those encountered during training. Additionally, the brief dip into negative values may result from the absence of output constraints in the network's final layer. Despite this initial irregularity, the model quickly stabilizes and accurately localizes the fault in IGBT 9**,** demonstrating its effectiveness and adaptability under fault conditions.

III.3.2.3. Fault of type T2



(a) (b)

Figure.II. 18: ANN output under T2 fault case : a) fault detection signal , b) fault localization signal

A fault is introduced once again at 0.2 s**,** and the ANN detects it more rapidly than in the previous case. The detection occurs at approximately 0.26 s**,** resulting in a faster response time of 60 ms**.** The zoomed-in inset in Figure.II. 18(a) clearly highlights this swift reaction. Upon fault initiation, a noticeable dip is again observed in the localization output; however, the system promptly recovers and correctly converges to IGBT 4 as the identified faulty switch. This localization result

is fully consistent with the injected fault scenario, thereby confirming the accuracy, responsiveness, and reliability of the ANN-based diagnostic model, as shown in Figure.II. 18(b).

The ANN demonstrates superior responsiveness to lower IGBT faults, likely due to their more pronounced impact on system behavior. The faster detection compared to the upper IGBT case underscores the model's ability to distinguish between fault severities. Accurate and prompt localization reinforces the suitability of this approach for real-time monitoring.

II.4. Fault detection and localization of OFC type 2 based on DWT-fuzzy logic

II.4.1. Overview of the method

In this method, a hybrid approach combining Fuzzy Logic with the Discrete Wavelet Transform (DWT) is proposed for the detection and localization of open-circuit fault type 2. This type of fault has received relatively limited attention in previous research, creating a gap that this work aims to address. The overall structure of the proposed method is illustrated in Figure.II. 19. As shown, the method is divided into two main stages. Part 1 focuses on feature extraction, where the DWT is employed to analyze the system signals and extract fault-sensitive features. Part 2 is dedicated to fault detection and localization, in which the extracted features serve as inputs to a Fuzzy Logic system to identify and localize the faulty switch with high accuracy.

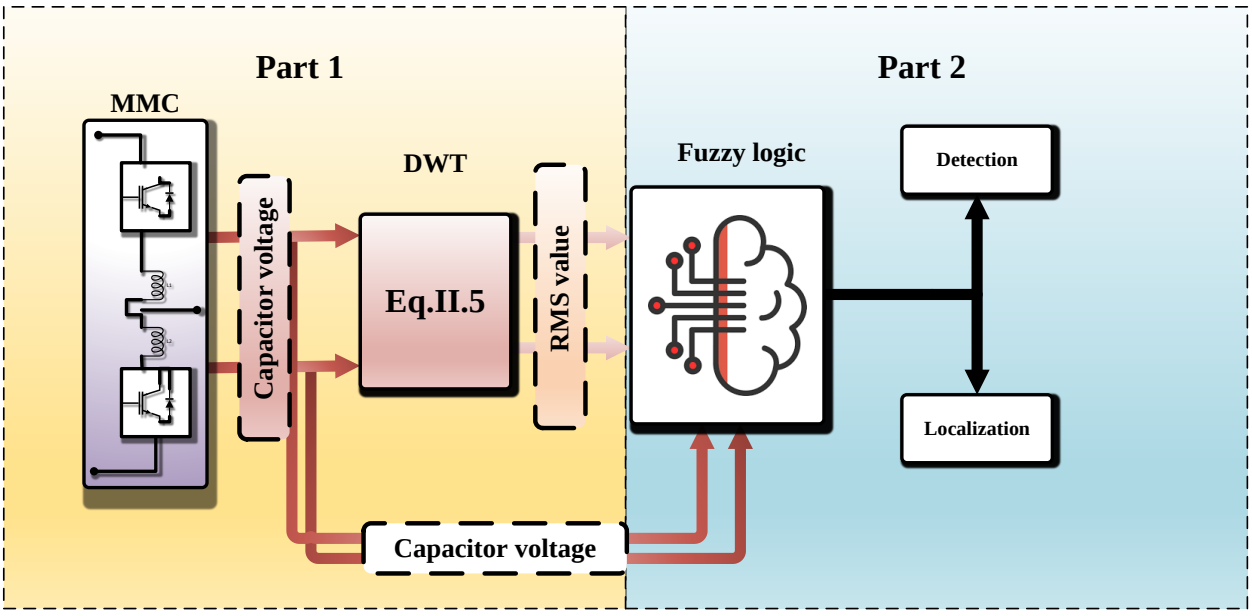


Figure.II. 19: structure the proposed method based on DWT-fuzzy

II.4.1.1. Part 1: Feature extraction

As discussed in Section II.2.2.B, the impact of a type 2 open-circuit fault (OCF) is illustrated in Figure.II. 7(a) and 7(b). When the upper switch is faulty, all the capacitor voltages in the corresponding arm remain constant after the fault occurs, while the capacitor voltages of the healthy arm gradually decrease. This characteristic behavior enables the detection of the fault. However, just using the changes in capacitor voltage signals makes it impossible to accurately locate the faulty switch. To address this limitation, the Discrete Wavelet Transform (DWT) is employed to analyze the capacitor voltage signals, providing additional information necessary for fault localization.

A) the Discrete Wavelet Transform (DWT)

The Discrete Wavelet Transform (DWT) is an advanced signal analysis method that breaks down a signal into various frequency bands at different resolutions. In contrast to the Fourier Transform, which provides only frequency information, the DWT delivers both time and frequency details. This feature makes it highly effective for detecting transient and short-duration events in a signal, which is especially valuable when dealing with non-stationary signals like capacitor voltages in power electronic converters. The decomposition is achieved by processing the signal through two filters, as depicted in Figure.II. 20 [100].

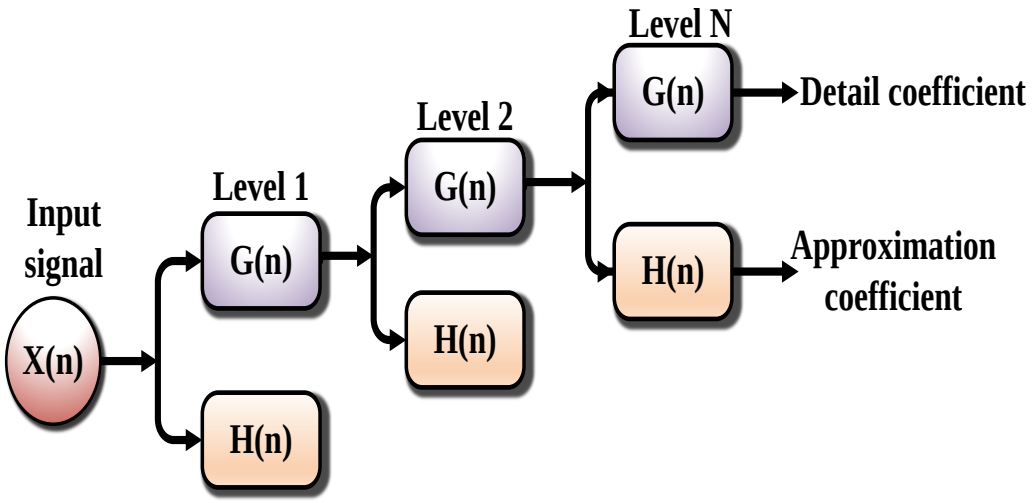


Figure.II. 20: DWT structure

Low-pass filter: This filter captures the approximation coefficients, which represent the smooth, low-frequency components of the signal. These coefficients provide a generalized view of the signal, focusing on its overall shape and trend

$$A[n] = \sum_{k} x[k].\, h[k - 2n] \qquad \text{II.4}$$

Where A[n]: represents the approximation coefficients, x[k]: is the original signal, h[k]:is the low-pass filter kernel, n is the discrete index of the resulting coefficients

High-pass filter: This filter extracts the detail part of the signal. Detail coefficients represent the high-frequency information, capturing abrupt changes, sharp transitions, or fault signatures in the signal. These coefficients are particularly useful for detecting transients or faults in systems like MMCs.

$$D[n] = \sum_{k} x[k].\, g[k - 2n] \qquad \text{II.5}$$

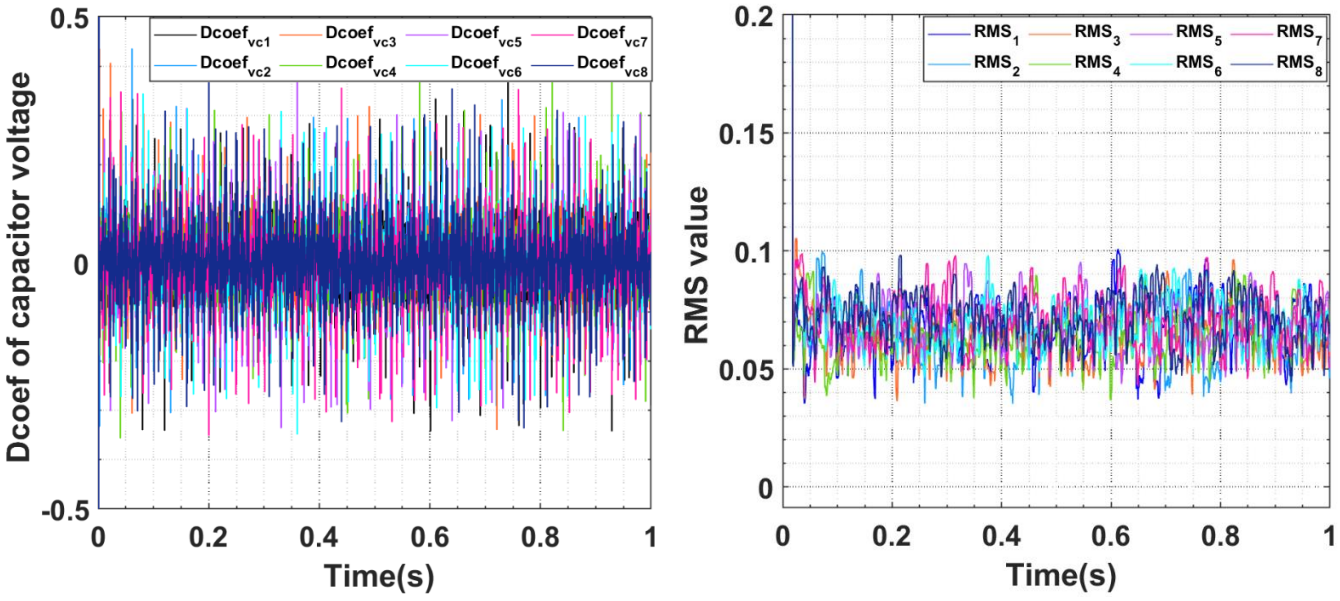
Where D[n]: represents the detail coefficients g[k]:is the high-pass filter kernel.

B) Signal decomposition using Discrete wavelet transform

In the case of a fault in the upper switch, the resulting fault signature in the capacitor voltage signal is not clearly distinguishable due to the similarity between healthy and faulty submodules as shows in Figure.II. 7.a. To address this challenge and extract meaningful features, multiple fault scenarios involving the upper switches (S1, S3, S5, S7, S9, S11, S13, and S15) were monitored and analyzed. For each scenario, the capacitor voltage signal was processed using a four-level Daubechies Discrete Wavelet Transform (DWT). This wavelet decomposition method was selected because of its ability to simultaneously provide time and frequency localization, enabling the detection of subtle, transient variations in the signal that are often associated with faults.

From the decomposition, the detail coefficients were selected as fault indicators. Because These coefficients are particularly effective in capturing abrupt changes, sharp transitions, and other fault-related disturbances that may be difficult to observe directly in the raw voltage waveform. To quantify these variations, the Root Mean Square (RMS) value of the detail coefficients was calculated for each case. The RMS metric provides a robust measure of signal energy in the high-frequency band, which exhibits significant changes in the presence of faults.

A threshold value was established by analyzing the RMS values of the detail coefficients under both healthy and faulty operating conditions. As illustrated in Figure.II.21(a), the detail coefficients of the capacitor voltages in the healthy case remain consistently bounded within approximately 0.5 to 0.5. This narrow range demonstrates the stability of the signals when no fault is present. In addition, Figure.II.21(b) shows the corresponding RMS values of the detail coefficients, which lie between 0.05 and 0.1 for all submodules. The uniformity of these values across the different signals, without any noticeable deviation, confirms the absence of abnormal behavior. This stable behavior under healthy conditions is therefore considered as the reference threshold for detecting faults

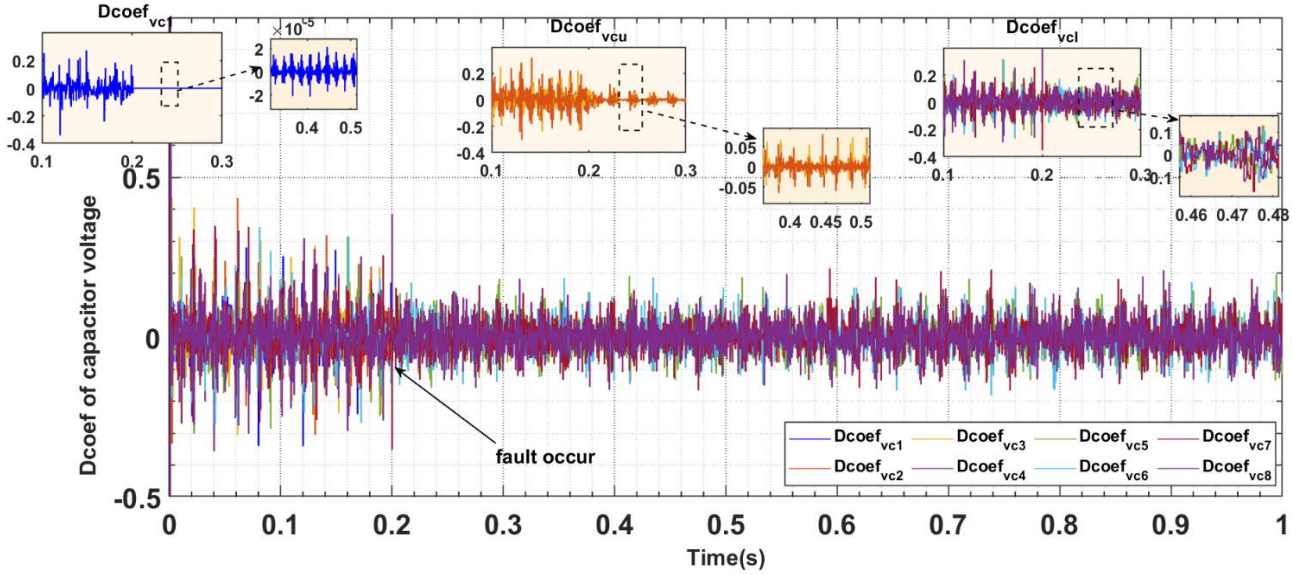


a) b)

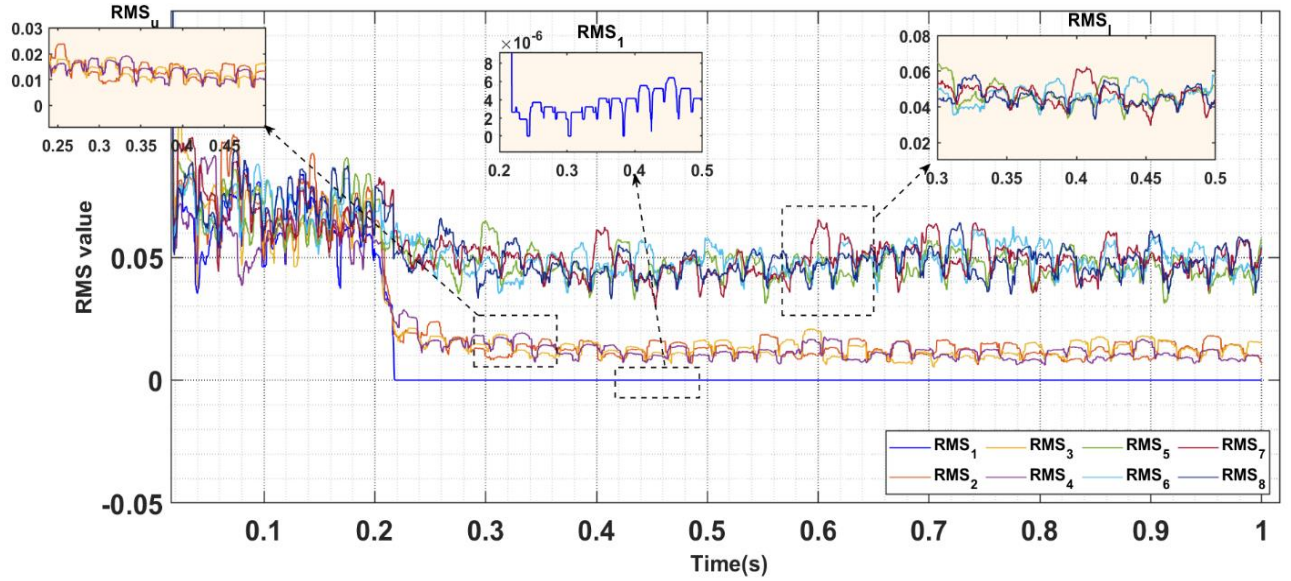
Figure.II. 21: under healthy case: a) details coefficient of VC, b) RMS value of Dcoef VC

On the other hand, Figure.II.22(a) and 22(b) present the detail coefficients and the corresponding RMS values, respectively, under faulty conditions. In this case, a fault was introduced at t = 0.2 s in the upper switch of SM1, as illustrated in Figure.II.22(a). Before the fault occurrence, the values of the detail coefficients remain stable within the range of –0.5 to 0.5, similar to the healthy case. However, after the fault, the detail coefficient corresponding to Vc_1 exhibits a sharp decrease, approaching approximately zero, as highlighted in the inset $Dcoef_{Vc1}$.

For Vc_2, Vc_3, and Vc_4, the values also decrease, but within a smaller range of about –0.05 to 0.05, as shown in the inset Dcoef $_{Vcu}$. On the other hand, the detail coefficients of the healthy arm exhibit only minor deviations, which are not significant, as indicated in the inset Dcoef $_{Vcl}$. These results demonstrate the effectiveness of the DWT technique in detecting even small signal variations, making it a powerful tool for identifying fault-related transitions in the system.



a)



b)

Figure.II. 22 : under upper switch fault: a) details coefficient of VC, b) RMS value of Dcoef VC

Similarly, Figure.II. 22(b) illustrates the RMS values of the detail coefficients in the faulty case. Before the fault occurs, the RMS values remain stable within the range of 0.05 to 0.1, consistent with the healthy condition. After the fault, however, the RMS value corresponding to submodule 1 shows a clear deviation, reaching approximately 0, as highlighted in the inset RMS_1. For the other submodules, the RMS values also deviate but within a smaller range, reaching around 0.02 as shows inset RMS_u. Furthermore, the RMS values corresponding to the healthy arm remain relatively low, with a maximum of about 0.04 inset RMS_l. By comparing the calculated RMS values against the defined threshold, it is possible not only to detect the occurrence of a fault but also to improve the accuracy of fault localization, particularly for upper switches, even in situations where the raw voltage signatures are less distinct.

For lower switch open-circuit faults, the capacitor voltages themselves are directly employed to detect and localize the fault. In this case, the capacitor voltage of the faulty submodule increases beyond the threshold of 2600 V, while the capacitor voltages of the healthy submodules drop below 2400 V, as illustrated in Figure.II.9(a) and 9(b). This distinct divergence between the faulty and healthy submodules provides a clear criterion for fault identification, allowing both detection and localization to be achieved with high reliability.

II.4.2. Part 2: fault detection and localization based on Fuzzy logic

Fuzzy logic is employed as an intelligent tool for detecting and locating faults, serving as a classifier in this study [101]. The fuzzy logic framework, illustrated in Figure.II.23, is composed of four functional blocks: fuzzification, the rule base, the inference mechanism, and defuzzification [102]. In the fuzzification step, crisp values (real numbers) are transformed into fuzzy sets. These are then processed by the inference engine, which applies the if–then rules to determine possible outcomes. Finally, the defuzzification stage converts the fuzzy results back into numerical values. In this work, the fuzzy system is designed with sixteen inputs eight capacitor voltages and eight RMS values of the decomposed voltage signals and two outputs: one indicating whether a fault is present (0 or 1) and another specifying its location (1 to 16).

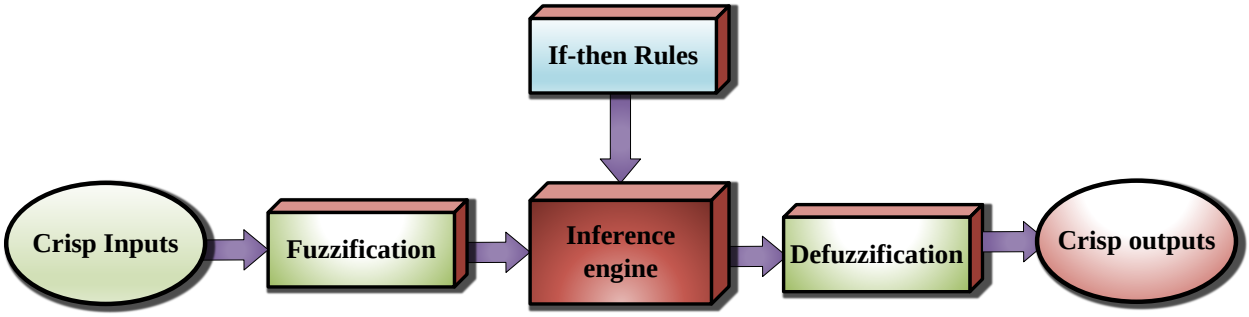


Figure.II. 23: The fuzzy logic framework

A) Fuzzy Input and Output Variable Sets

Triangular and trapezoidal membership functions are employed to fuzzify all input variables. The fuzzy linguistic terms for the capacitor voltage inputs are defined as follows:

- H (High): capacitor voltage above 2600 V
- N (Normal): capacitor voltage between 2400 V and 2600 V
- L (Low): capacitor voltage below 2400 V

For the inputs corresponding to the RMS values of the decomposed voltage signals, the fuzzy sets are:

- N (Normal): values ranging from 0.02 to 0.2
- VL (Very Low): values between 0 and 0.002

Regarding the outputs, two fuzzy variables are defined:

- Fault Detection: with linguistic terms Q0 (healthy/clear system) and Q1 (faulty system).
- Fault Location: with linguistic terms Q0, Q1, Q2 … Q16, where Q0 represents no fault and Q1–Q16 correspond to faults occurring in the respective switc

B) If-the fuzzy rule base

Table.II. 3: Fuzzy rules

№	Vr 1	Vc 1	Vr 2	Vc 2	Vr 3	Vc 3	Vr 4	Vc 4	Vr 5	Vc 5	Vr 6	Vc 6	Vr 7	Vc 7	Vr 8	Vc 8	det	loc
S0	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	N	Q0	Q0
S1	VL	N	N	N	N	N	N	N	N	L	N	L	N	L	N	L	Q1	Q1
S2	N	H	N	L	N	L	N	L	N	L	N	L	N	L	N	L	Q1	Q2
S3	N	N	VL	N	N	N	N	N	N	L	N	L	N	L	N	L	Q1	Q3
S4	N	L	N	H	N	N	N	N	N	L	N	L	N	L	N	L	Q1	Q4
S5	N	N	N	N	VL	N	N	N	N	L	N	L	N	L	N	L	Q1	Q5
S6	N	N	N	N	VL	N	N	N	N	L	N	L	N	L	N	L	Q1	Q6
S7	N	N	N	N	N	N	VL	N	N	L	N	L	N	L	N	L	Q1	Q7
S8	N	L	N	L	N	L	N	H	N	L	N	L	N	L	N	L	Q1	Q8
S9	N	L	N	L	N	L	N	L	VL	N	N	N	N	N	N	N	Q1	Q9
S10	N	L	N	L	N	L	N	L	N	H	N	L	N	L	N	L	Q1	Q10
S11	N	L	N	L	N	L	N	L	N	N	VL	N	N	N	N	N	Q1	Q11
S12	N	L	N	L	N	L	N	L	N	L	N	H	N	L	N	L	Q1	Q12
S13	N	L	N	L	N	L	N	L	N	N	N	N	VL	N	N	N	Q1	Q13
S14	N	L	N	L	N	L	N	L	N	L	N	L	N	H	N	L	Q1	Q14
S15	N	L	N	L	N	L	N	L	N	N	N	N	N	N	VL	N	Q1	Q15
S16	N	L	N	L	N	L	N	L	N	L	N	L	N	L	N	H	Q1	Q16

The rule base represents the knowledge of an expert operator regarding the system under study, and it forms the foundation of decision-making in the fuzzy logic framework. Each fuzzy rule follows an *if–then* structure, consisting of two parts: the antecedent, which defines the conditions of the input variables (capacitor voltages and RMS values), and the consequent, which specifies the corresponding outputs (fault detection and location). The fuzzy variables within the antecedent are connected using the logical operator AND**,** allowing multiple input conditions to be evaluated simultaneously. In this context, linguistic labels such as *N, H, L,* and *VL* describe the qualitative

states of the input signals. Table.II.3 presents the constructed fuzzy rules, where the column det indicates the fault status (Q0 for healthy, Q1 for faulty), and Loc identifies the faulty submodule (Q1–Q16). This systematic mapping ensures accurate and interpretable fault detection and localization within the Modular Multilevel Converter.

C) Defuzzification

The final stage of the fuzzy inference process is defuzzification**,** where the fuzzy outputs are converted into crisp numerical values. In this work, the centroid method is employed, as expressed in equation II.6

$$C = \frac{\sum_{i=1}^{n} h_i u_i}{\sum_{i=1}^{n} u_i} \qquad \text{II.6}$$

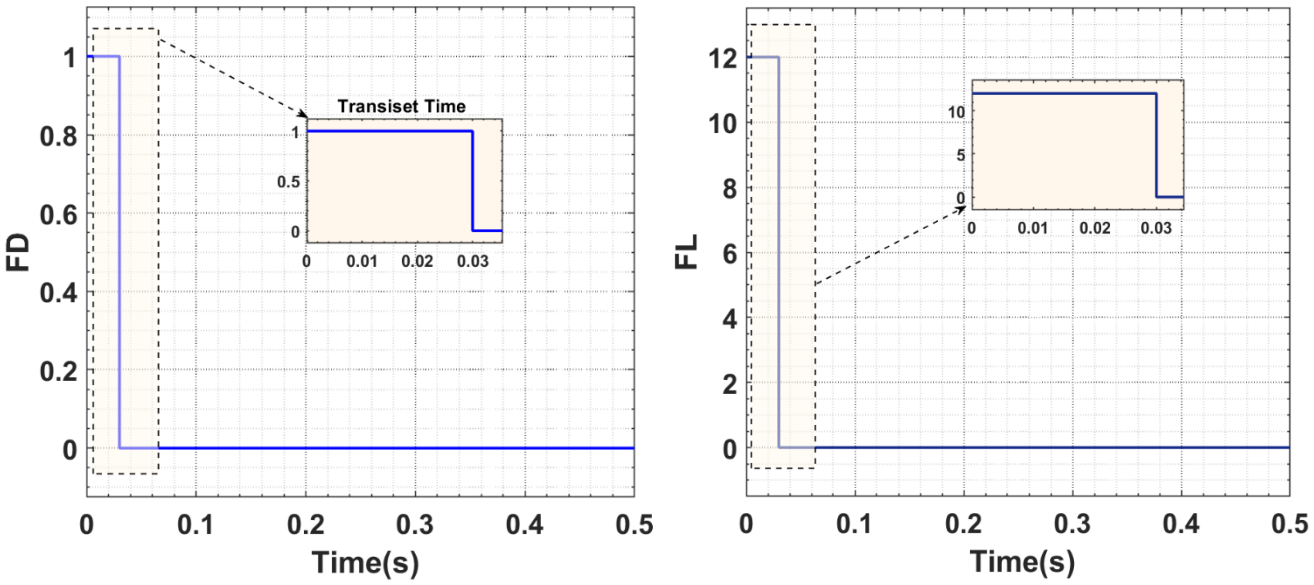
where h_i represents the center of the i^{th} fuzzy set and u_i denotes its corresponding membership function. This method calculates the weighted average of all possible outputs, ensuring a balanced and precise crisp output for both fault detection and localization.

II.4.2. Results and discussion

After designing the fuzzy inference system for fault detection and localization in the MMC, the next step is to assess its performance. This section reports the obtained results, highlighting the behavior of the system under normal operation and different fault scenarios. The effectiveness of the proposed method is demonstrated through simulation studies and comparative analysis.

A) Healthy case

Figure.II. 24 illustrates the fault detection (FD) and fault localization (FL) signals under healthy operating conditions. As shown in Figure.II.24 (a), the FD signal initially exhibits a short transient response at the start of the simulation due to switching and initialization effects. After a few milliseconds, it stabilizes at zero and remains constant throughout the entire simulation, confirming the absence of faults. Similarly, Figure.II.24 (b), shows the FL signal, which also undergoes a brief transient before converging to zero. The stable zero value of both FD and FL signals throughout the operation verifies that the system operates under normal conditions without any false detections or mis localizations.



a) b)

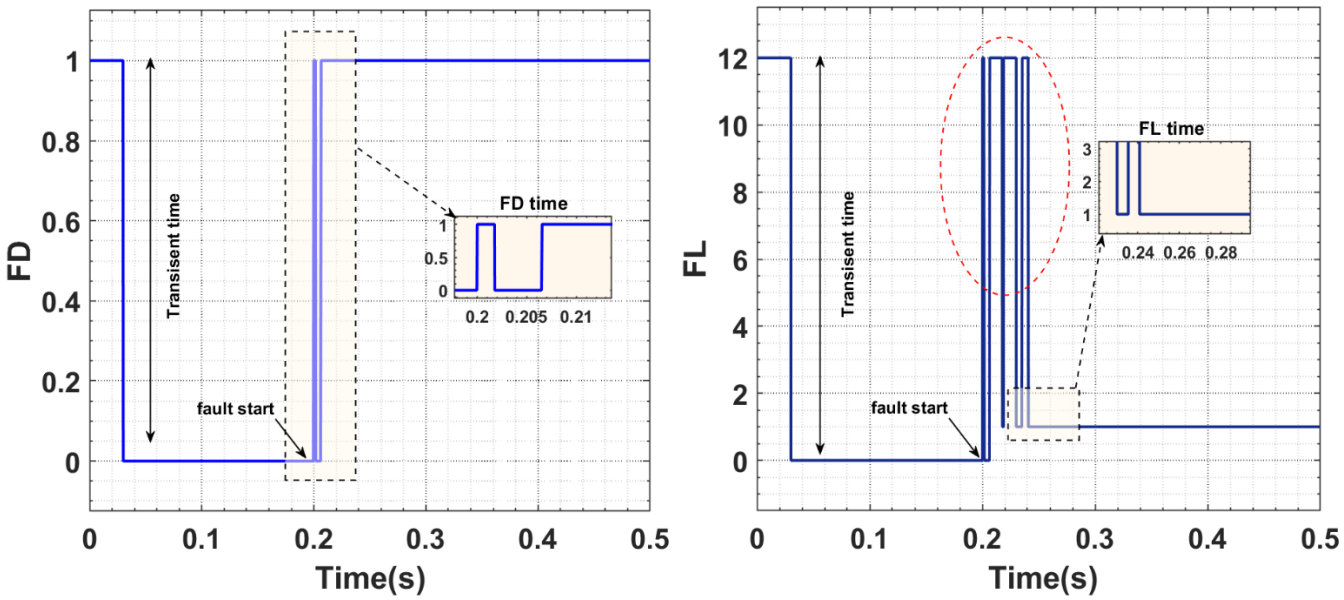
Figure.II.24: Fuzzy output under healthy case, a) FD signal, b) FL signal

B) Upper switch fault

In this case, an open-circuit fault was applied to the upper switch (IGBT 1+ diode) of SM1 at *t* = 0.2 s. The corresponding fault detection (FD) and fault localization (FL) signals are illustrated in Figure.II. 25

Figure.II.25 (a) shows the FD signal. At the beginning of the simulation, a short transient period appears, during which the signal briefly fluctuates before stabilizing at zero. At the fault initiation instant (*t* = 0.2 s), the FD signal transitions from 0 to 1 after a brief transient, confirming the successful detection of the fault. The zoomed view emphasizes this rapid response of approximately 5 ms , highlighting the efficiency of the proposed detection method.

Figure.II.25. (b) presents the FL signal, which identifies the specific faulty switch. Immediately after the fault occurs, transient oscillations are observed, as expected due to the sudden switching disturbance. Shortly afterward, the signal stabilizes and converges to the value 1, correctly indicating the fault in switch 1 of SM1. The zoomed section shows that the localization process is completed around *t* = 0.24 s, corresponding to a total fault localization time of approximately 40 ms.



a) b)

Figure II.25. Fuzzy output under upper switch fault case, a) FD signal, b) FL signal

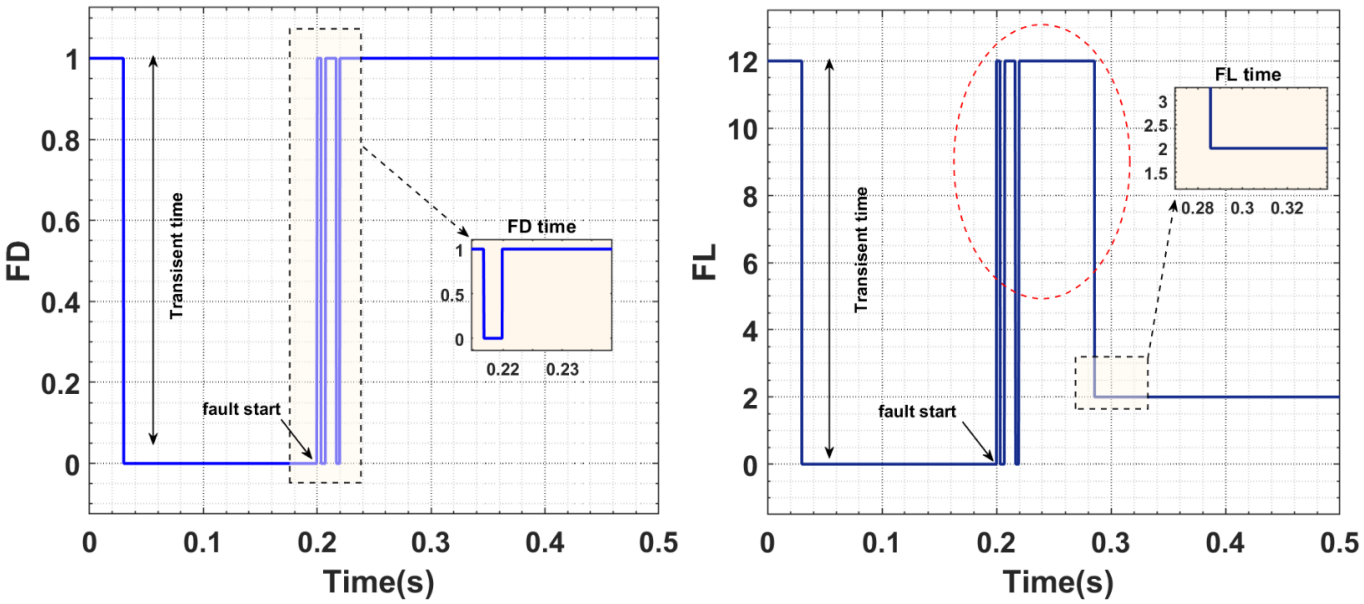
C) Lower switch fault

In this scenario, an open-circuit fault is introduced in the lower switch (IGBT2 + diode) of SM1 at t = 0.2 s, and the associated fault detection (FD) and fault localization (FL) signals are shown in Figure.II.26

Figure.II.26 (a) depicts the FD response. During the initial stage of the simulation, the signal undergoes a brief transient before settling at zero. Once the fault occurs at t = 0.2 s, the FD signal begins to rise and eventually reaches the value of 1, indicating that the fault has been detected. Compared with the previous case, the detection delay is noticeably longer, with the zoomed window showing that the method requires about 20 ms to confirm the fault.

Figure.II.26 (b) presents the FL behavior. Following the fault instant, the signal exhibits stronger oscillations than in the earlier scenario. This is mainly due to the capacitor voltage imbalance triggered by the fault event. After this transient stage, the signal converges to the steady value of 2, which correctly corresponds to switch 2 of SM1. From the zoomed section, it can be observed

that the localization process settles around t = 0.28 s, giving a total localization time of approximately 80 ms.



a) b)

Figure. II.26. Fuzzy output under upper switch fault case, a) FD signal, b) FL signal

II.4.2.1Comparison between different fault diagnosis method for open circuit fault

The comparison presented in the Table II.4 highlights the evolution of fault detection strategies for open-circuit faults (OCF). Earlier studies such as [5] and [8] rely on model-based approaches, while [87] adopts a signal-based technique; all of them exhibit moderate computational complexity and moderate detection speed when addressing Type 1 OCF. More recent works like [91] employ AI-based methods, which significantly improve detection speed, achieving fast response times, but at the expense of high computational complexity, potentially limiting real-time implementation in resource-constrained systems. In contrast, the proposed STD-ANN method achieves fast fault detection with only moderate complexity, offering a balanced compromise between performance and computational demand. Furthermore, the proposed DWT-Fuzzy Logic hybrid technique demonstrates even lower complexity while maintaining fast detection capability and extending applicability to Type 2 OCF. Overall, the proposed methods provide an improved trade-off between speed and computational burden, enhancing practical feasibility for real-time fault diagnosis in power converter systems.

Table.II. 4: Comparison between different fault diagnosis method for open circuit fault

Ref	Method	Complexity	Fault type	Time
[5]	Model based	Moderate	Type 1 OCF	Moderate
[8]	Model based	Moderate	Type 1 OCF	Moderate
[87]	Signal based	Moderate	Type 1 OCF	Moderate
[91]	AI based	High	Type 1 OCF	fast
STD-ANN	AI based	Moderate	Type 1 OCF	fast
DWT-FL	Hybrid technique	Low	Type 2 OCF	fast

II.5. Conclusion

In conclusion, the presented study extends fault diagnosis in Modular Multilevel Converters by addressing not only IGBT open-circuit faults but also faults in the anti-parallel diode, which are often overlooked in existing works. By employing two complementary intelligent strategies ANN-based detection for IGBTs and a hybrid DWT–Fuzzy Logic approach for the entire switching device the proposed methods demonstrate high effectiveness in fault detection and localization. Simulation results in MATLAB/Simulink confirm their capability to provide fast, accurate, and reliable diagnostic performance, thereby enhancing the overall reliability and safety of MMC systems.

Chapter III

Advanced Strategies for Short-Circuit Fault Diagnosis in MMCs

III.1. Introduction

the complex structure of MMCs, composed of multiple submodules with numerous semiconductor switches and capacitors, makes it more exposed to different types of faults. One of the most dangerous problems is the short-circuit (SC) fault, especially when it happens in Insulated Gate Bipolar Transistors (IGBTs). These faults can seriously damage the system, cause shutdowns, and create safety risks. [103],

To keep the system safe and running well, it is very important to detect such faults quickly and correctly. Traditional fault detection methods often respond slowly [11,89,90], miss early signs of faults [11], or cannot accurately identify the faulty part. Because of these limits, this chapter focuses on improving the detection and identification of short-circuit faults in MMCs, particularly those that affect power switches.

Two methods are proposed in this chapter. The first one uses Discrete Wavelet Transform (DWT) to extract useful features from the capacitor voltage, which are then used by a Radial Basis Function Neural Network (RBFNN) to detect and locate the faulty switch. The second method relies on signal processing techniques applied to the system's current and voltage waveforms for identifying the fault. Both methods are tested through simulations of a single-phase MMC system under different fault conditions. The results show that the proposed approaches are fast, accurate, and reliable in detecting and locating faults. This work helps move closer to building real-time monitoring systems for MMCs and supports ongoing efforts to make multilevel converters safer and more reliable.

III.2. Short-Circuit Fault Characteristics and Impact

Insulated Gate Bipolar Transistors (IGBTs) are vital switching devices in Modular Multilevel Converters (MMCs), where they regulate energy flow by controlling the insertion or bypassing of submodules. These switches, due to their repetitive switching operations and high voltage stresses, are susceptible to failures particularly short-circuit (SC) faults. An IGBT short-circuit can lead to significant system disruptions, including unbalanced arm voltages, overcurrent damage to submodules, overheating, or even total system shutdown if not detected promptly [103],

III.2.1. Characteristics of SCF

In a typical half-bridge MMC submodule, two IGBTs (T1 and T2) are configured in a complementary manner with an energy storage capacitor. Short-circuit faults may occur in either T1, T2, or both, (Figure.III.1), leading to the following operating conditions [104]:

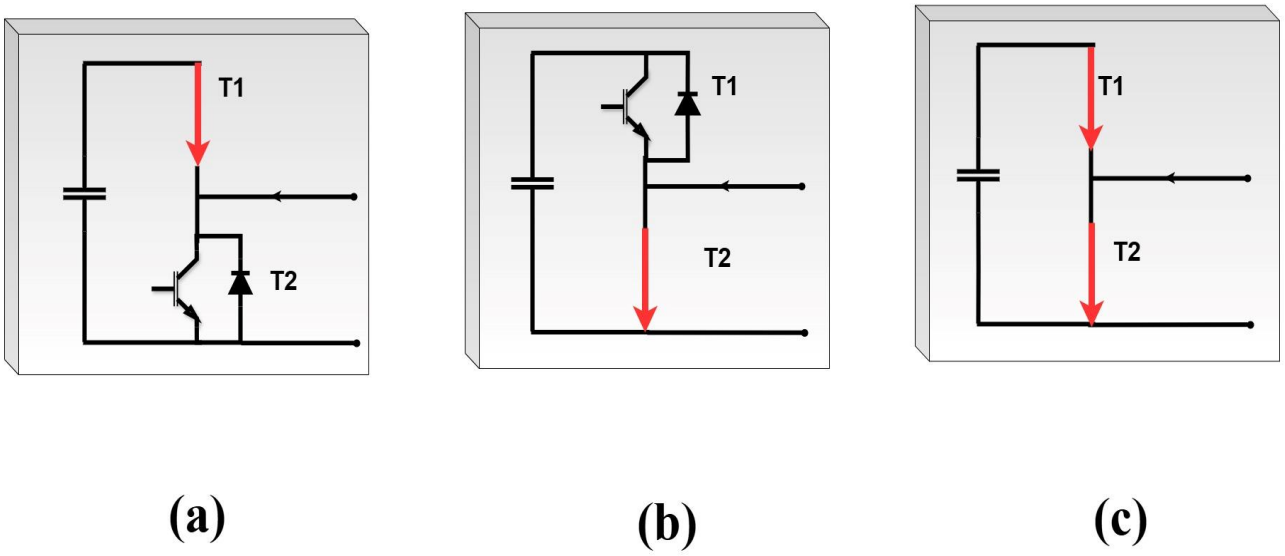


Figure.III. 1: SCF modes a) T1 Fault , b) T2 Fault ,c) T1&T2 Fault

- **T1 Short-Circuit Fault**

When the upper switch (T1) experiences a short-circuit, the submodule remains permanently connected to the capacitor. As a result, the output voltage of the submodule becomes equal to the capacitor voltage V_C regardless of the control signals. This unintentional and continuous insertion of the submodule disturbs the voltage balancing mechanism and may cause overcharging or overheating of the capacitor if not managed correctly

- **T2 Short-Circuit Fault**

If the lower switch (T2) is short-circuited, the submodule is permanently bypassed, and the output voltage drops to zero. This means the submodule does not contribute to the total output voltage, leading to a drop in phase voltage and disturbance in the converter's output waveform. If several submodules are affected this way, the MMC's ability to synthesize a multilevel waveform is compromised

- **Both T1 and T2 Short-Circuited**

In the worst-case scenario, where both switches are short-circuited simultaneously, a direct path is created between the upper and lower terminals, effectively shorting the capacitor. In this case, the output voltage also becomes zero, but more dangerously, a large circulating current may flow through the arm, causing severe thermal and electrical stress. This can lead to catastrophic failure if not interrupted quickly

III.2.2. Impact of SCF

To evaluate the impact of short-circuit faults (SCFs) on the reliability and performance of the Modular Multilevel Converter (MMC), various fault scenarios were introduced and analyzed using MATLAB/Simulink. These simulations aim to replicate realistic fault conditions occurring within IGBT switches of MMC submodules and assess their effect on system-level parameters.

In the simulation setup, different scenarios were applied, including:

- T1 IGBT short-circuit fault in one submodule, at (t = 0.3 s) in SM1
- T2 IGBT short-circuit fault in one submodule, at (t = 0.3 s) in SM1
- Simultaneous faults in both upper and lower switches (T1 and T2) of a submodule. (t = 0.3 s) in SM1

Figure.III. 2 and 3 illustrate the impact of a T1 short-circuit fault on the MMC system, while Figure.III. 4 and 5 present the consequences of a T2 short-circuit fault. The effects of a simultaneous short-circuit fault in both T1 and T2 are shown in Figure.III.s 6 and 7.

As illustrated in Figures.III.2a and 2b, the output voltage and current waveforms experience severe distortion immediately after the occurrence of the T1 short-circuit fault, demonstrating its strong impact on system performance. Likewise, Figure.III. 3 shows that the capacitor voltage in Submodule 1 exhibits a pronounced deviation from its normal operating behavior (Figure.III. 3a). The other capacitor voltages also display noticeable deviations, but with distinct fault signatures

(Figurs.III. 3b and 3c). These observations confirm that short-circuit faults pose a significant risk to the safe and reliable operation of the system.

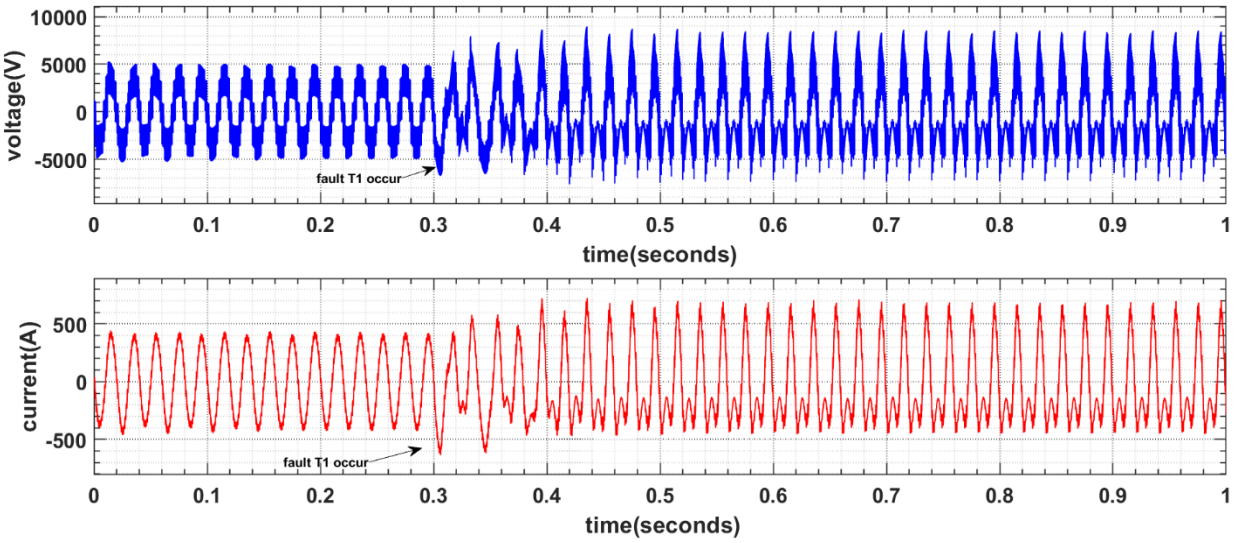


Figure.III. 2 : AC output under T1 fault

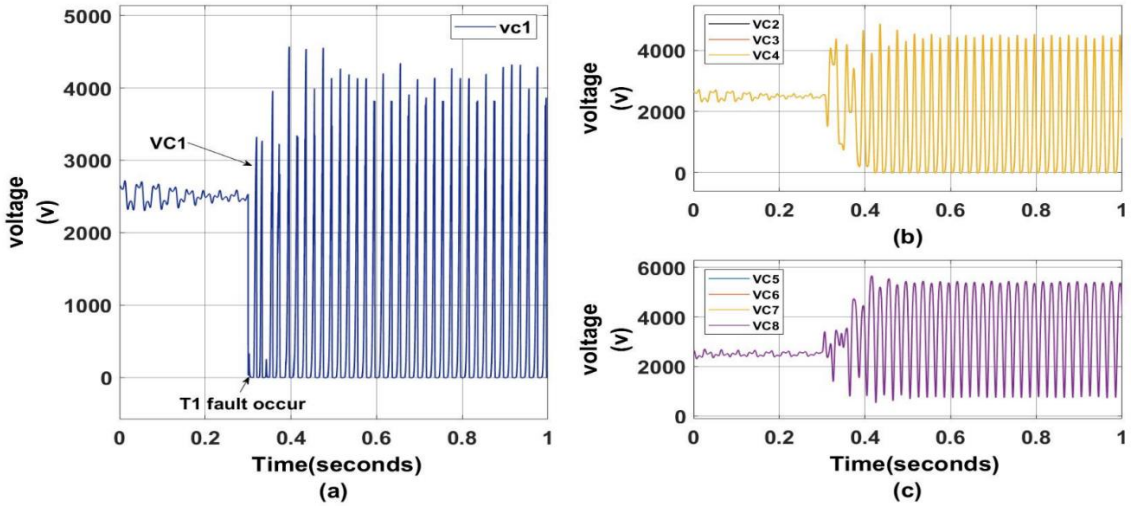


Figure.III. 3: capacitor voltage under T1 fault

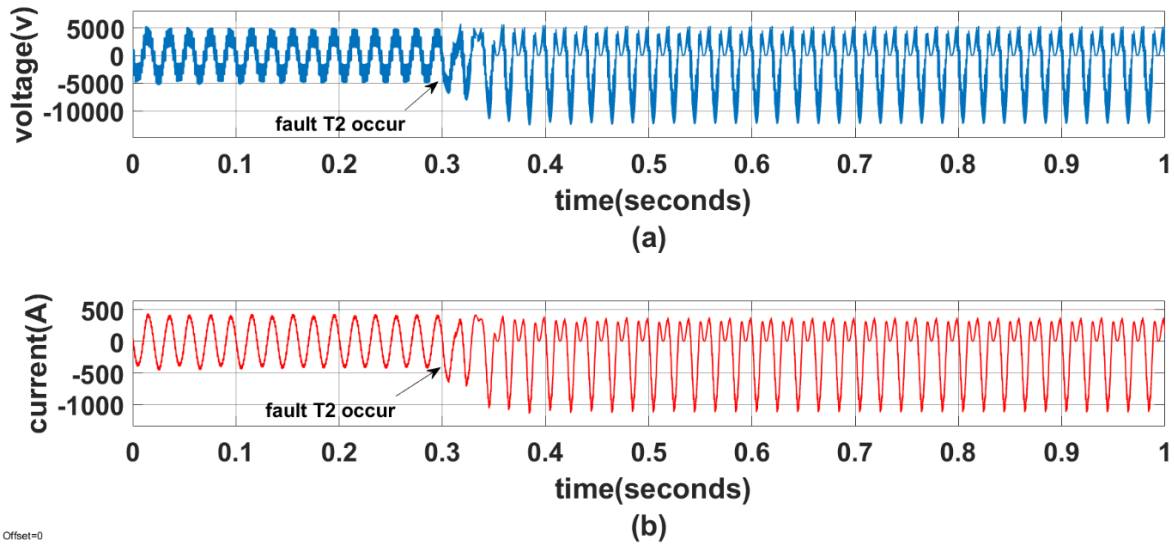


Figure.III. 4:AC output Under T2 fault

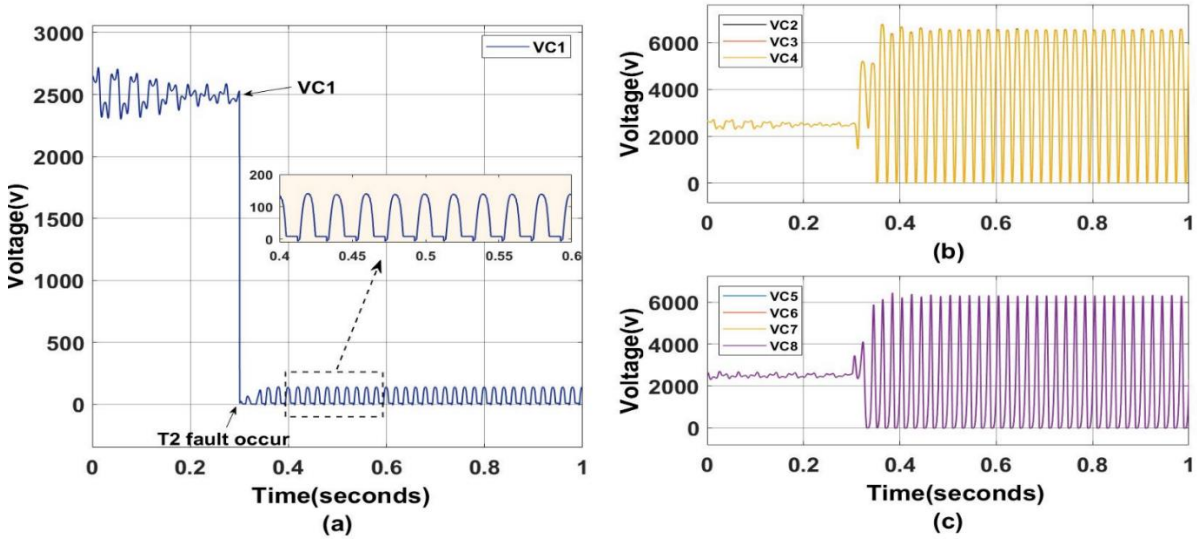


Figure.III. 5:capacitor voltage under T2 fault

Similarly, under a T2 short-circuit fault, the system performance is severely affected, as illustrated in Figure.III. 4. However, the resulting waveform distortion differs from that observed in the T1 fault case. As shown in Figure.III. 5a, the capacitor voltage of Submodule 1 (Vc1) experiences a sharp decline, approaching zero immediately after the fault occurs. This behavior indicates that the capacitor is effectively bypassed, thereby disrupting energy storage and voltage

regulation within the submodule. In addition, the other capacitor voltages exhibit noticeable deviations with distinct fault signatures, as presented in Figure.III.s 5b and 5c.

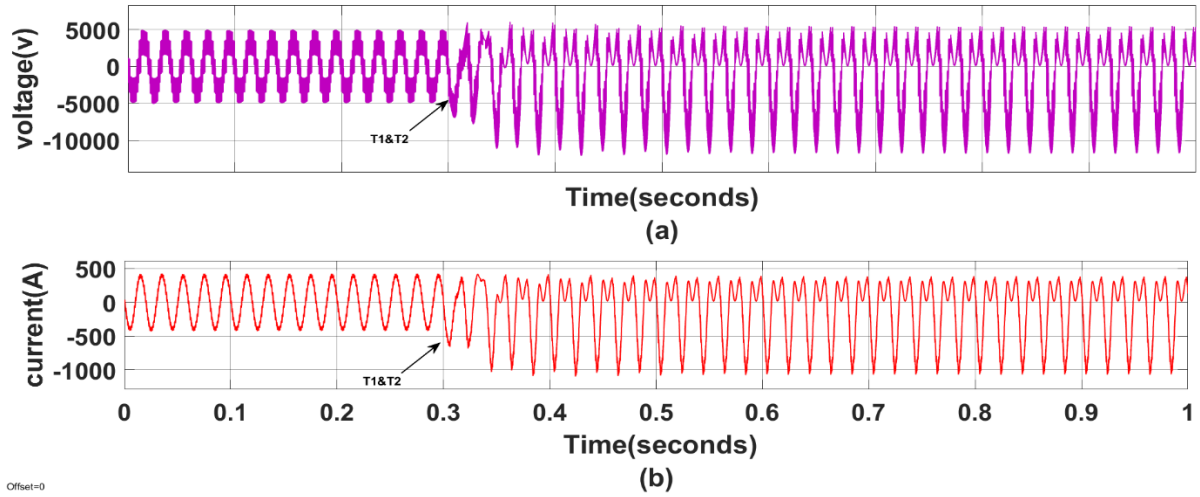


Figure.III. 6 :AC output under T1&T2 fault

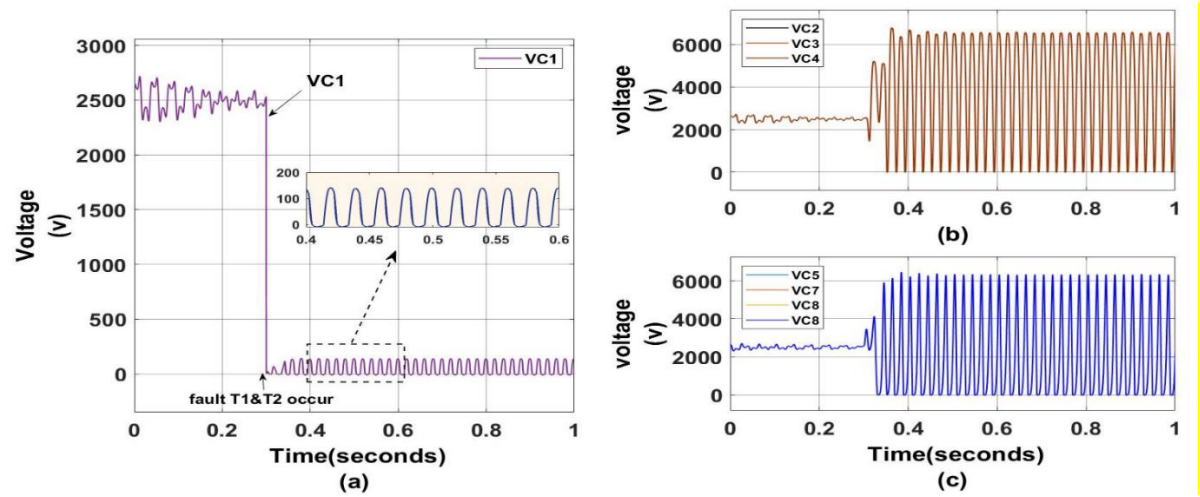


Figure.III. 7: capacitor voltage under T1&T2 fault

In the case where both T1 and T2 are short-circuited, the system exhibits behavior similar to that of a T2 fault, but with even more severe consequences. Since both IGBT switches are permanently conducting, the submodule becomes completely bypassed, and the output voltage drops to zero regardless of control signals. This results in the full current flowing through the fault path, leading

to excessive stress on other components and a potential risk of thermal damage or catastrophic failure. As shown in Figure.III. 6 and 7, the capacitor voltage is rapidly drained, and the output current becomes highly distorted. The bypass path also takes longer to stabilize, increasing the risk of propagation of the fault to neighboring submodules or the entire MMC system. This scenario highlights the critical need for rapid detection and isolation mechanisms to prevent system-wide collapse.

III.3. Fault detection and localization of SCF based on DWT-RBFNN

III.3.1. overview of the method

In this method, the capacitor voltages of the MMC are employed as the primary indicators for fault detection, as they exhibit characteristic variations under different fault scenarios. These voltages are inherently monitored for control and voltage balancing, eliminating the need for additional sensing hardware. To isolate relevant fault features, the Discrete Wavelet Transform (DWT) is used to decompose the voltage signals and extract key frequency components. These features are subsequently fed into a Radial Basis Function Neural Network (RBFNN), which performs fault classification and accurately identifies the specific faulty submodule. The overall diagnostic approach, depicted in Figure.III. 8, combines DWT-based feature extraction with RBFNN-based classification to enable efficient and precise fault detection and localization within the converter.

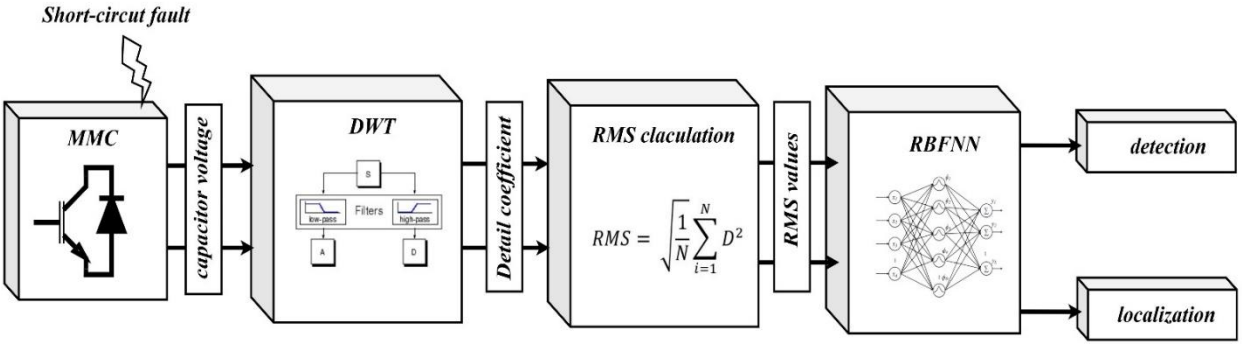


Figure.III. 8:The proposed method based on DWT-RBFNN

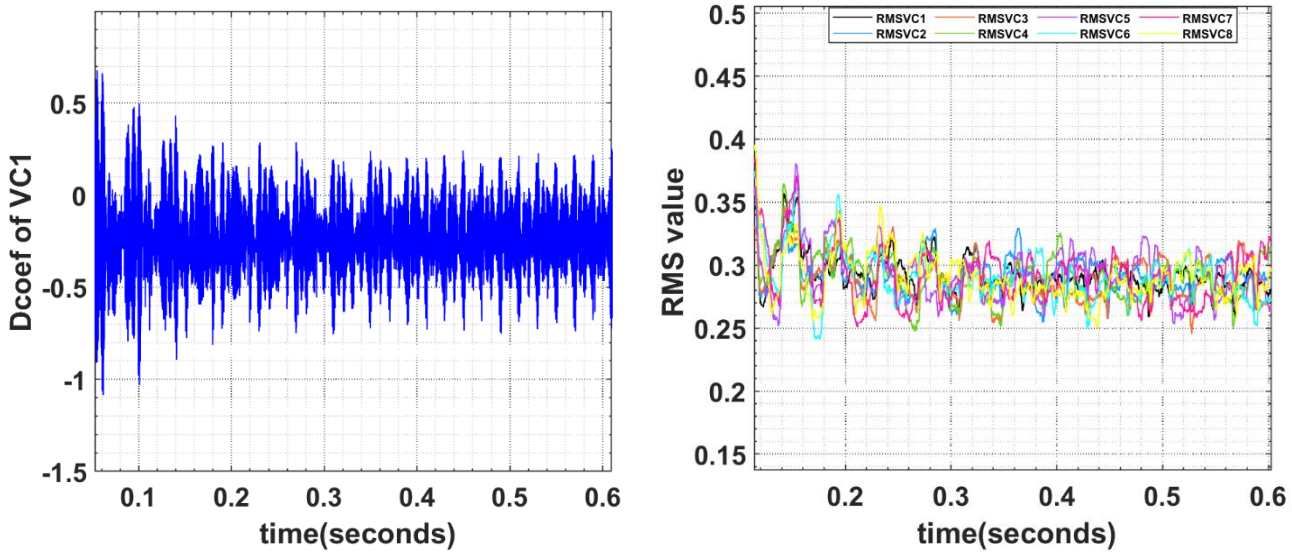
III.3.1.1. Features extraction based on DWT

In this methodology, the feature extraction process is based on the same Discrete Wavelet Transform (DWT) technique introduced in Chapter II section II.4. (DWT-Fuzzy logic). However,

unlike the previous application, which used a four-level decomposition to capture subtle variations in capacitor voltages associated with gradual degradation, the short-circuit fault detection requires only a one-level DWT decomposition. This is due to the abrupt and high-frequency nature of short-circuit faults, which manifest clearly in the first-level detail coefficients. Therefore, the detail coefficients obtained from a single-level DWT are sufficient to capture the transient characteristics of the capacitor voltage signals under fault conditions. These extracted features are then used as inputs for the classification model described in the subsequent section.

The results of the feature extraction process demonstrate the effectiveness of the proposed method in fault detection. This approach identifies faults by analyzing the Root Mean Square (RMS) values of the detail coefficients obtained through DWT under both healthy and faulty operating conditions. This comparison not only enables the detection of fault occurrence but also offers insight into the fault's severity. Furthermore, the temporal evolution of the capacitor voltage, particularly in Submodule 1 (SM1), is closely monitored. This time-domain analysis enhances fault characterization by revealing noticeable changes in signal patterns, allowing for a clearer distinction between normal and fault states.

A) Healthy case (no fault)

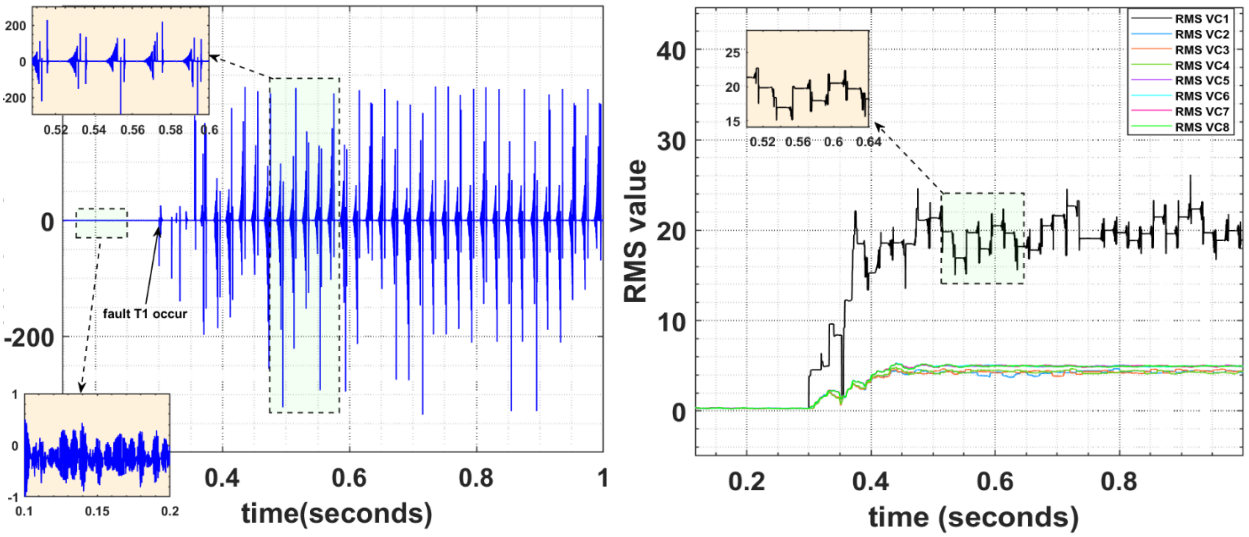


a) b)

Figure.III. 9 : healthy cases: a) detail coefficient, b) RMS value

Figure.III. 9.a presents the detail coefficients of Submodule 1 (SM1) obtained via the Discrete Wavelet Transform (DWT) over a 1-second duration under healthy operating conditions. Correspondingly, Figure.III..9.b illustrates the Root Mean Square (RMS) values of the DWT detail coefficients for all eight capacitor voltage signals. Under normal conditions, these RMS values consistently fall within the range of 0.25 to 0.35, establishing a baseline threshold. Any deviation from this range indicates the presence of a fault in the corresponding submodule. It is important to note that the time interval from 0 to 0.25 seconds represents the system's transient phase, which is considered part of normal operation and not indicative of a fault.

B) Fault of type T1



a) b)

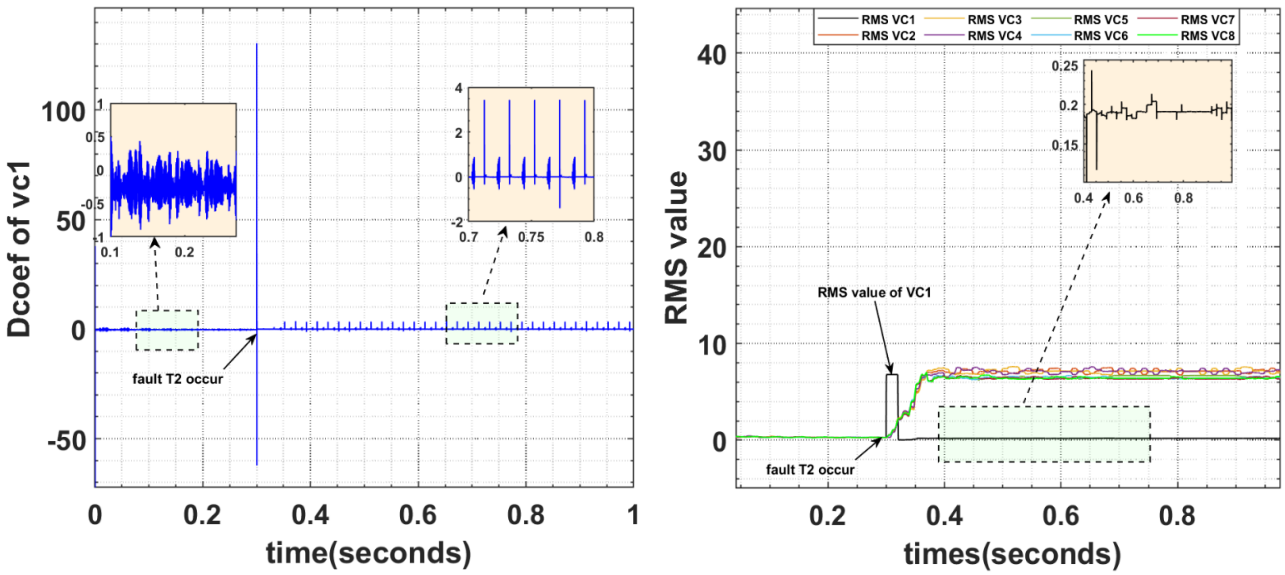
Figure.III. 10: Under T1 fault a) detail coefficient, b) RMS value

Before the fault occur at 0.3s seconds, the detail coefficient values remain stable, with a range of -0.5 to 0.5, reflecting the behavior the normal behavior of capacitor voltage (Vc1). However, after the fault T1 occur (0.3s), the detail coefficient values undergo a dramatic change, ranging from -200 to 200 as illustrate Figure.III. .10. a This large shift highlights the impact of the fault on the capacitor voltage and effectively demonstrates the DWT's ability to detect fault signatures.

Figure.III.10.b presents the root mean square (RMS) variations of the detail coefficients for the voltage signals of eight capacitors under T1 fault. Before the fault occurs, the RMS variations for

each signal are similar, converging between 0.2 and 0.3, indicative of healthy operation., with the occurrence of the T1 fault at 0.3 seconds, a notable deviation appears in the RMS value of Vc1, which sharply increases to 18. In contrast, the RMS values of the detail coefficients for the healthy capacitors remain unchanged. This stark contrast in the RMS values confirms the presence of the T1 fault specifically in SM1, reinforcing the effectiveness of the proposed method for fault detection.

C) Fault of type T2



a) b)

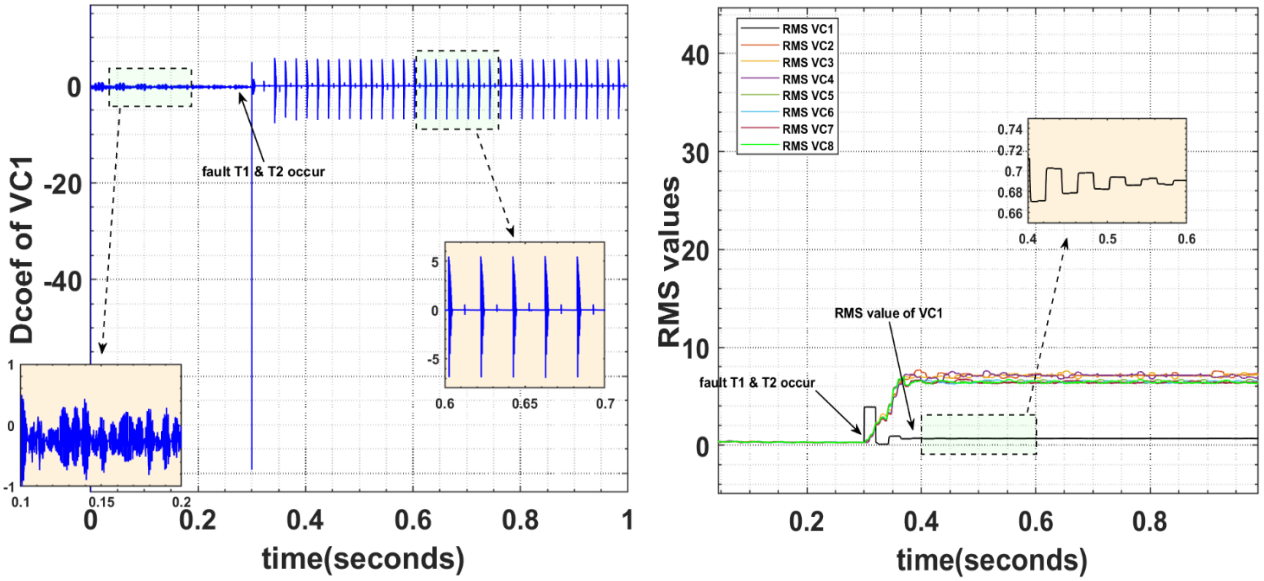
Figure.III. 11. Under T2 fault a) detail coefficient, b) RMS value

Similarly, to the previous case, Figure.III. 11.a illustrates the detail coefficients of the capacitor voltage for SM1 under a T2 fault condition. Between 0 s and 0.3 s, the detail coefficients of Vc1 fluctuate within the range of -0.5 to 0.5, indicating normal operation. However, upon the occurrence of the T2 fault at 0.3 s, the coefficients shift and stabilize between approximately -2 and 4, highlighting a deviation from healthy behavior.

Correspondingly, Figure.III. 11.b presents the RMS values of the detail coefficients. Before the fault occurs, the RMS values for all capacitor voltages fall within the range of 0.2 to 0.3, consistent with healthy operation. After the T2 fault occurs, the RMS values for Vc2 to Vc8 increase significantly, reaching around 7, while the RMS value of Vc1 decreases steadily to approximately

0.18. This contrast indicates that the fault affects SM1 and alters the system dynamics, supporting the effectiveness of the proposed method in detecting and localizing faults.

D) Simultaneous T1 and T2 fault



a) b)

Figure.III. 12: Under T1&T2 fault a) detail coefficient, b) RMS value

Figure.III. 12.a displays the detail coefficients of the capacitor voltage for SM1 under a simultaneous T1 and T2 fault condition, while Figure.III. 12.b presents the corresponding RMS values for Vc1 to Vc8. Similar to the previous cases, no significant changes are observed in the RMS values prior to the fault occurrence at 0.3 seconds, indicating normal operation. However, once the simultaneous T1 and T2 fault is introduced, a noticeable deviation is observed. Specifically, the RMS value of Vc1 increases markedly to approximately 0.7, as shown in Figure.III. 12.b. This shift highlights the impact of the simultaneous fault on SM1 and further confirms the sensitivity and effectiveness of the proposed method in detecting multiple fault conditions.

III.3.1.2. Radial Basis Function Neural Network (RBFNN)

After extracting the necessary features, a Radial Basis Function Neural Network (RBFNN) was employed to train these features for the purposes of fault detection and localization. RBFNNs

are a type of feedforward neural network that are particularly effective in function approximation, pattern recognition, and classification tasks [105]. As illustrated in Figure.III. 13, the architecture of an RBFNN consists of an input layer, a single hidden layer composed of radial basis function neurons, and an output layer [106]. Each neuron in the hidden layer utilizes a radial basis function most commonly a Gaussian function to measure the similarity between the input vector and the neuron's center [107]. The output layer then aggregates these weighted similarities to generate the final output [108].

The primary computation in an RBFNN is defined by the following equation:

$$\emptyset_i(x) = exp\left(-\frac{\|x-\mu_i\|^2}{2\sigma_i^2}\right) \quad \text{III.1}$$

Where: ϕ_i : the radial basis function, μ_i : is the center of the *i*-th node, σ_i : is the spread width of the *i*-th node, x represents the input vector, The RBFNN output is calculated as a weighted sum of the hidden layer outputs:

$$y = f(x) = \sum_{i=1}^{k} w_i \, \emptyset_i(x) \quad \text{III.2}$$

Where: $f(\mathbf{x})$: is the final outputw_i: the hidden-to-out put weight corresponding to the *i*-hidden node$\emptyset_i$:the radial basis function of the *i*-th hidden node *K:* is the Total number of hidden nodes.

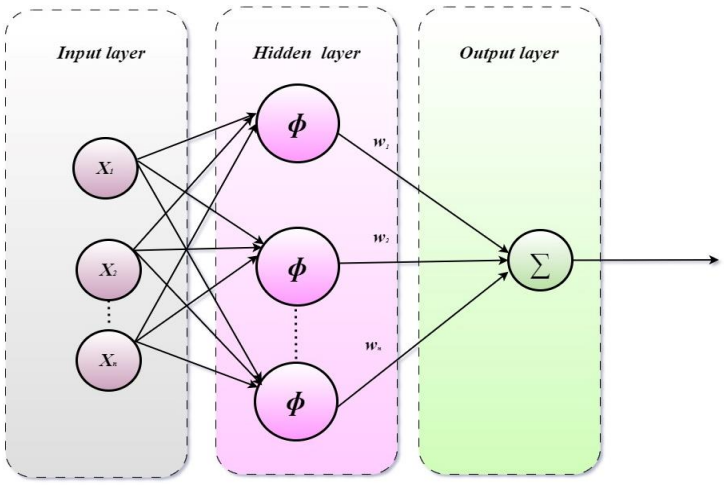


Figure.III. 13 :RBFNN structure

A) Architecture of the RBFNN Used in This Work

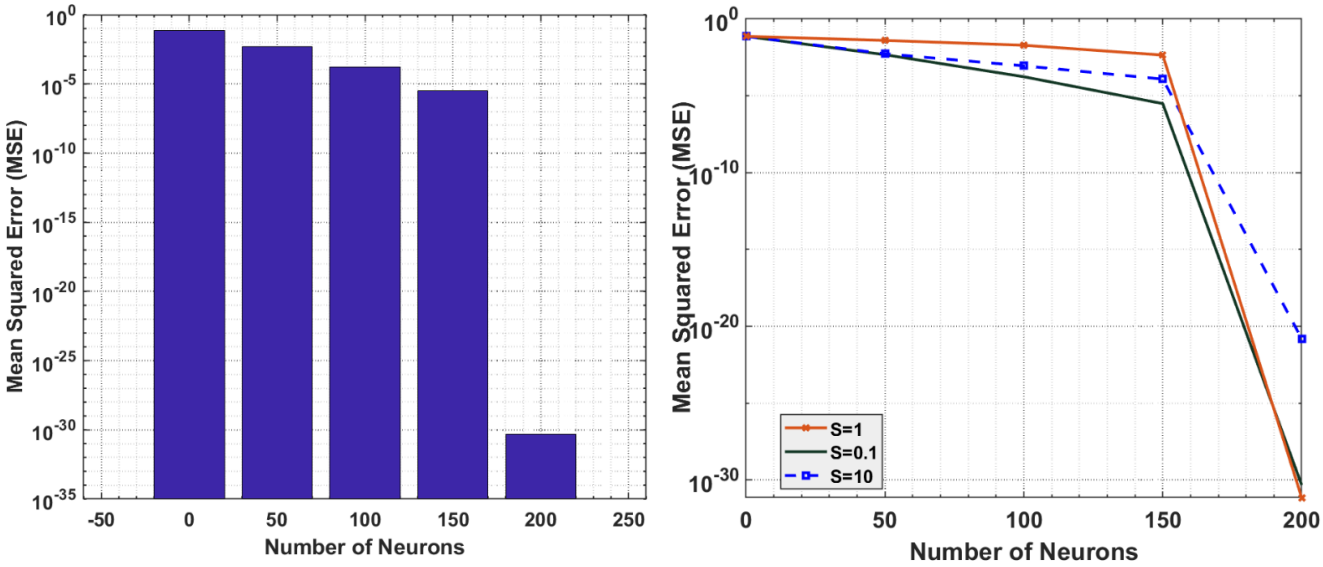
In this study, the Radial Basis Function Neural Network (RBFNN) is structured as follows:

- **Input Layer**: The network receives an input dataset of dimensions 200×8, where each of the 200 samples is represented by an 8-dimensional feature vector extracted from the signal processing stage.
- **Hidden Layer**: A single hidden layer composed of radial basis neurons computes the similarity between the input vectors and predefined centers using radial basis functions. The number of neurons in this layer is determined adaptively during training to achieve a specified performance criterion.
- **Output Layer**: The output layer produces results with dimensions 200×16, where each output vector indicates the network's classification or localization of faults. These outputs are compared against the corresponding 16-dimensional target vectors during the training phase.

B) RBFNN Training

To train the RBFNN model, MATLAB's `newrb` function was utilized. This function builds the network incrementally by adding neurons to the hidden layer until a predefined Mean Squared Error (MSE) goal is achieved, as illustrated in Figure.III. 14.a. As additional neurons are introduced, the model's capacity to approximate the target function improves, resulting in a progressive reduction in MSE.

A key parameter in this process is the spread (σ), which was set to 1 in this study. This parameter significantly affects the shape and width of the Gaussian radial basis functions used by the hidden neurons. As shown in Figure.III. 14.b, the choice of the spread parameter plays a vital role in determining the model's performance. A spread that is too small may cause the network to overfit the training data, capturing noise and reducing generalization capability. Conversely, an excessively large spread can lead to underfitting, where the model fails to capture important patterns in the data.



a) b)

Figure.III. 14.RBFNN evaluation. a) impact of neurons, b) impact of spread

III.3.2 Results and discussion

To assess the effectiveness of the proposed fault detection and localization approach, a MATLAB/Simulink model of a 5-level Modular Multilevel Converter (MMC) was developed. The simulated MMC features four submodules (SMs) per arm, with each SM incorporating two Insulated Gate Bipolar Transistors (IGBTs), resulting in a total of 16 IGBTs across the system. This setup allows for the emulation of various fault scenarios, which are classified into the following categories:

- **T1-Type Faults**: Eight scenarios involving faults affecting only the T1 switch.
- **T2-Type Faults**: Eight scenarios where only the T2 switch is faulty.
- **Simultaneous T1 & T2 Faults**: Eight cases where both T1 and T2 are concurrently faulty within the same submodule.
- **Healthy Condition**: A reference scenario representing standard converter operation without any faults.

In total, 25 simulation cases were performed 24 representing distinct fault conditions and one reflecting normal operation. For clarity and to emphasize the proposed method's performance,

results from four representative scenarios are presented: the healthy condition and three fault cases occurring in Submodule 1 (SM1).

III.3.2.1. healthy case (no fault)

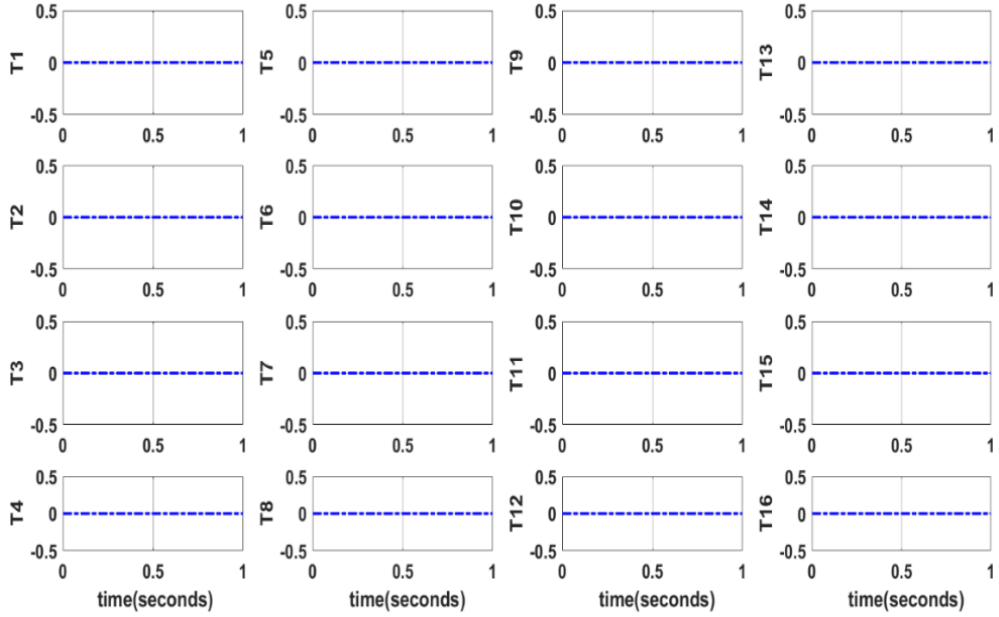


Figure.III. 15:RBFNN output Under healthy case

the healthy operating condition of the Modular Multilevel Converter (MMC) is first analyzed. This scenario is essential for characterizing the system's nominal behavior and serves as a reference for identifying deviations under fault conditions the output of the Radial Basis Function Neural Network (RBFNN) is shown in Figure.III. 15. It can be observed that all 16 outputs of the RBFNN each corresponding to one of the 16 IGBT switches are equal to 0, where '0' indicates a healthy state and '1' denotes a fault. This result confirms that the MMC is free of faults and operating under normal conditions.

III.3.2.2. Fault of type T1

In this section, fault type T1 is analyzed based on the data of DWT technique. As previously noted, the fault is introduced at 0.3 seconds. The proposed detection and localization method promptly identifies and isolates the fault. As illustrated in Figure.III. 16, the fault is detected at 0.34 seconds, indicated by a binary output transition from 0 (no fault) to 1 (fault detected). The same Figure.III.16 further shows that the fault is localized to Submodule 1 (SM1)**,** with a rapid localization interval of just 0.04 seconds**.** This swift and accurate response demonstrates the effectiveness of the proposed method in enhancing the reliability and safety of the MMC system by enabling timely fault detection and precise localization.

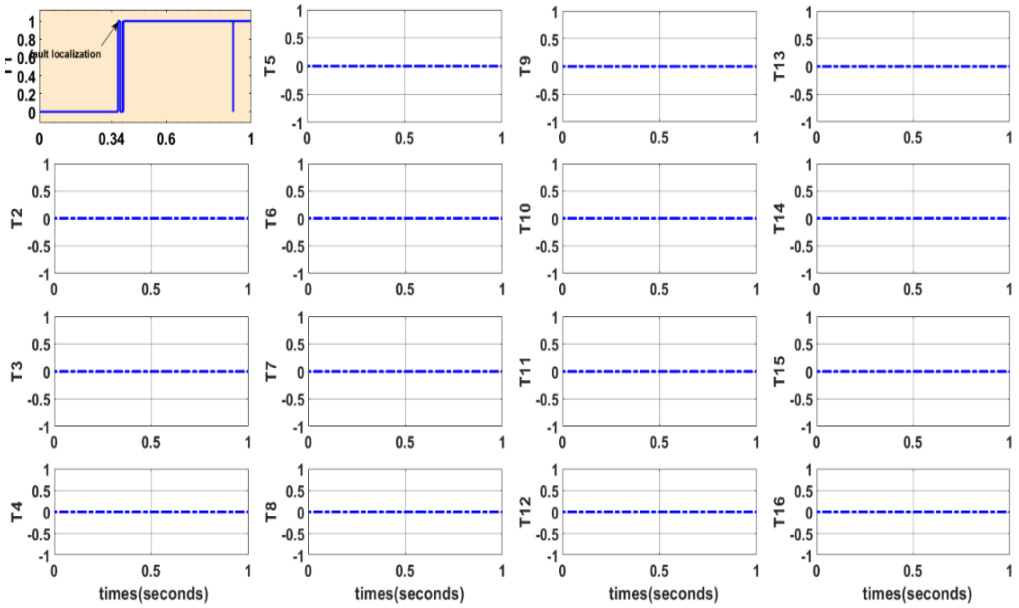


Figure.III. 16:RBFNN output Under T1

III.3.2.3. Fault of type T2

Similar to the previous case, this section analyzes fault T2. As shown in Figure.III. 17, the output of the RBFNN indicates that the fault is detected at 0.36 seconds, and it is accurately localized to the corresponding faulty IGBT. Although the detection and localization process are slightly slower compared to the T1 case, it still demonstrates a rapid and reliable response. This reinforces the effectiveness of the proposed method in achieving timely fault diagnosis and maintaining the overall safety and robustness of the MMC system.

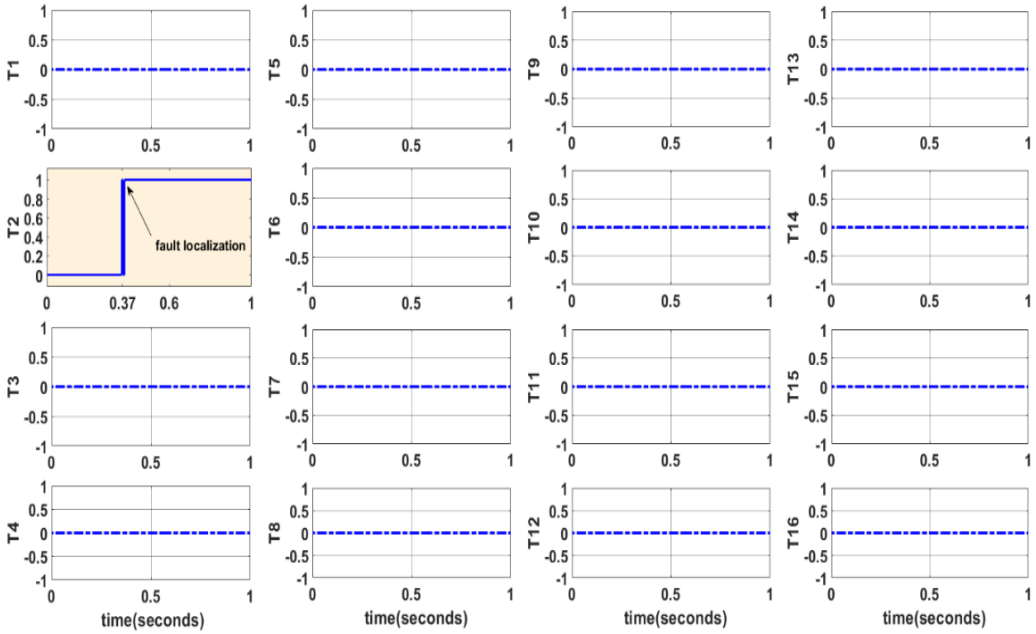


Figure.III. 17:RBFNN output Under T2 fault

III.3.2.4. simultaneous T1 and T2 fault

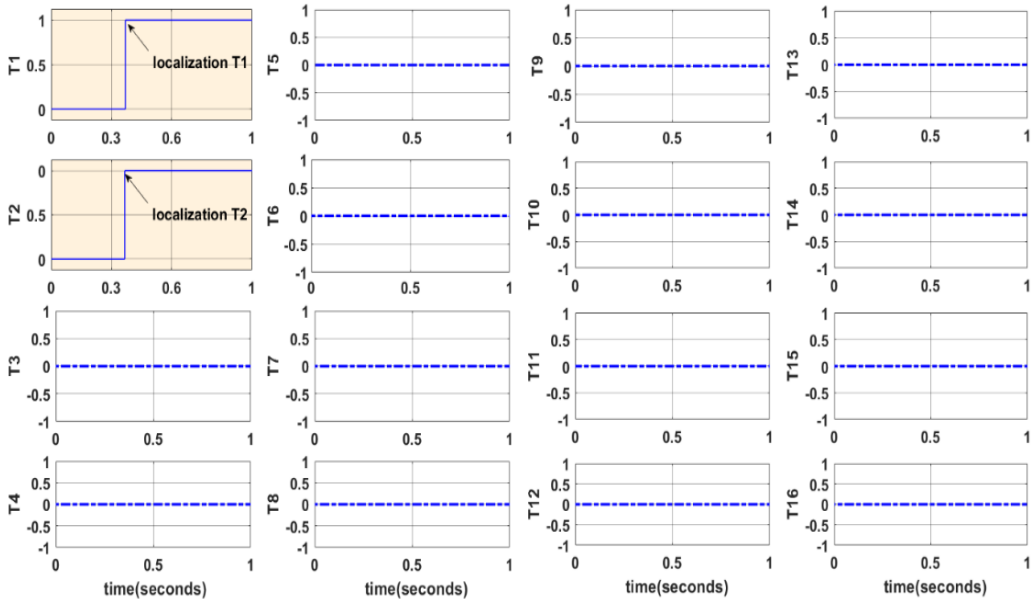


Figure.III. 18:RBFNN output Under T1&T2 fault

To validate the effectiveness of the proposed approach, simultaneous T1 and T2 faults are introduced. As in the previous cases, the RBFNN output in Figure.III. 18 illustrates the method's rapid detection of these concurrent faults, demonstrating its capability for real-time fault identification. Furthermore, the proposed strategy successfully localizes both T1 and T2 faults,

highlighting its ability to accurately distinguish between multiple simultaneous faults within the Modular Multilevel Converter (MMC) system. This level of precision is essential for maintaining the reliability and robustness of the fault detection and localization process.

III.4. Fault detection and localization of SCF based on RMS-CC & HLT

III.4.1. Overview of the method

Another short-circuit fault (SCF) detection method based on signal processing has been developed. The proposed strategy is structured into two main steps:

- **Step 1 – Fault Detection:** Identify the occurrence of a fault within the MMC system.
- **Step 2 – Fault Localization:** Determine the exact submodule and switching device where the fault has occurred.

III.4.1.1. step 1: fault detection

At this stage, the Root Mean Square (RMS) method is applied to detect faults using the differential current defined in Equation (I.16). The process consists of computing the RMS values of the MMC current signal, which represent its effective magnitude. These values are compared against reference RMS levels established under healthy operating conditions. Any significant deviation from the reference serves as an indicator of a possible fault. To improve reliability, a predefined threshold is introduced to distinguish between normal variations and actual faults. As illustrated in Figure III.19, this technique provides robust and consistent fault detection while reducing the likelihood of false positives

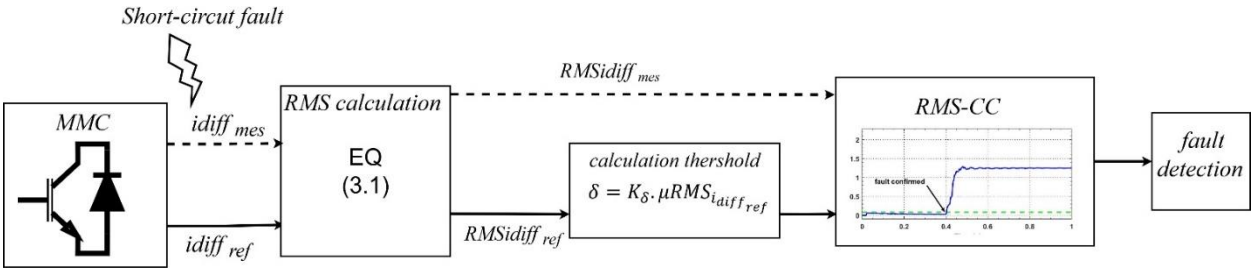


Figure.III. 19:structure of step 1

The method is defined according to the following criteria

$$\begin{cases} RMS_{i_{diff_{mes}}} \geq \delta \\ \delta = K_{\delta}.\mu RMS_{i_{diff_{ref}}} \end{cases} \quad \text{III.3}$$

Where $RMS_{i_{diff_{mes}}}$ is the measured value, $\mu RMS_{i_{diff_{ref}}}$ is mean RMS current during normal operation, δ is the threshold value, K_{δ} is tuning factor.

III.4.1.2. step 2: fault localization

The precise identification of a faulty IGBT depends on recognizing the instant when the capacitor voltage departs from its normal behavior. These departures generally appear as transient disturbances within the voltage waveform. To detect such variations, the Hilbert Transform is employed, as it can extract the instantaneous signal envelope, which serves as a reliable indicator of amplitude fluctuations

In contrast to the Fourier Transform, which gives an overall representation of a signal's frequency content, the Hilbert Transform provides localized amplitude information over time, making it well-suited for transient studies, While the Fast Fourier Transform (FFT) may overlook or blur short-duration events, and wavelet-based methods often demand careful basis selection and involve high computational cost, the Hilbert Transform efficiently generates an analytic signal in the time domain with minimal computational effort. This makes it especially advantageous for real-time monitoring and fault detection applications [109.110].

the Hilbert Transform $H\big(x(t)\big)$ is defined as:

$$H\big(x(t)\big) = \frac{1}{\pi} P.V \int_{-\infty}^{\infty} \frac{x(\tau)}{t-\tau} d\tau \quad \text{III.4}$$

In this context, P.V. refers to the Cauchy principal value. Through this operation, every frequency component of the signal undergoes a 90° phase shift while its amplitude remains unchanged, producing what is known as the quadrature counterpart of the signal [111,112].

Combining the original signal $x(t)$and its Hilbert Transform $H\big(x(t)\big)$ yields the analytic signal $z(t)$defined as:

$$z(t) = x(t) + jH\big(x(t)\big) \quad \text{III.5}$$

Through this complex signal, it becomes possible to extract the instantaneous envelope $|z(t)|$ instantaneous phase $\emptyset(t)$and instantaneous frequency $f(t)$which are defined as [111,112].

$$|z(t)| = \sqrt{x^2(t) + H^2\big(x(t)\big)} \quad , \emptyset(t) = tan^{-1}\left(\frac{H\big(x(t)\big)}{x(t)}\right) \quad \text{III.6}$$

$$f(t) = \frac{1}{2\pi}\frac{d\emptyset(t)}{dt}$$

In this approach, the capacitor voltages $v_{ci}(t)$ from the submodules (SMs) are continuously observed. To detect irregularities caused by faults, the Hilbert Transform is applied to each $v_{ci}(t)$ generating the corresponding analytic signal**:**

$$h(t) = v_{ci}(t) + jH\big(v_{ci}(t)\big) \quad \text{III.7}$$

The instantaneous envelope is employed as the fault indicator since it reliably reflects real-time amplitude variations in the capacitor voltage. Disturbances appear as clear deviations or spikes within the envelope, which makes fault identification straightforward. Functionally, the Hilbert envelope behaves like an amplitude demodulator: it attenuates the high-frequency switching ripple while highlighting the lower-frequency modulations linked to abnormal events. In rotating machinery diagnostics, this technique has been shown to suppress high-frequency oscillations and enhance the visibility of periodic fault-related impulses [113].

the envelope, is given by:

$$|h(t)| = \sqrt{{v_{ci}}^2(t) + H^2\big(v_{ci}(t)\big)} \quad \text{III.8}$$

A Max block is applied to the envelope signal to find the submodule with the greatest voltage value. The localization condition can be written as

$$v_{ci,faulty} = \max(|h_i(t)|), \qquad \forall i \in \{1,2,\dots,n_{sm},\} \quad \text{III.9}$$

A fault is classified as Type T1 if:

$$\max(|h_i(t)|) > \alpha \qquad and\ persists\ for\ t_k > T_{th} \quad \text{III.10}$$

A fault is classified as Type T2 if:

$$\beta < \max(|h_i(t)|) \leq \alpha \quad and\ persists\ for\ t_k > T_{th} \qquad \text{III.11}$$

Here, α and β denote the first and second thresholds, respectively, while t_k represents the time during which the fault condition persists, and $T_{th}$is the minimum time duration required to confirm a fault. These thresholds were selected based on experimental analysis and further validated through mathematical scaling in relation to the maximum Hilbert envelope observed during normal operation. This configuration ensures that Type T1 faults generate values that exceed α, whereas Type T2 faults fall within the range between β and α

$$\begin{cases} \alpha = \gamma_{1.\max(|h_i(t)|)_{normal}} \\ \beta = \gamma_{2.\max(|h_i(t)|)_{normal}} \end{cases} \qquad \text{III.12}$$

Where γ_1 , γ_2 are scaling factors chosen based on fault behavior; $\max(|h_i(t)|)_{normal}$ is the maximum value of the envelope in normal operation, The complete fault localization methodology is depicted in Figure.III. 20

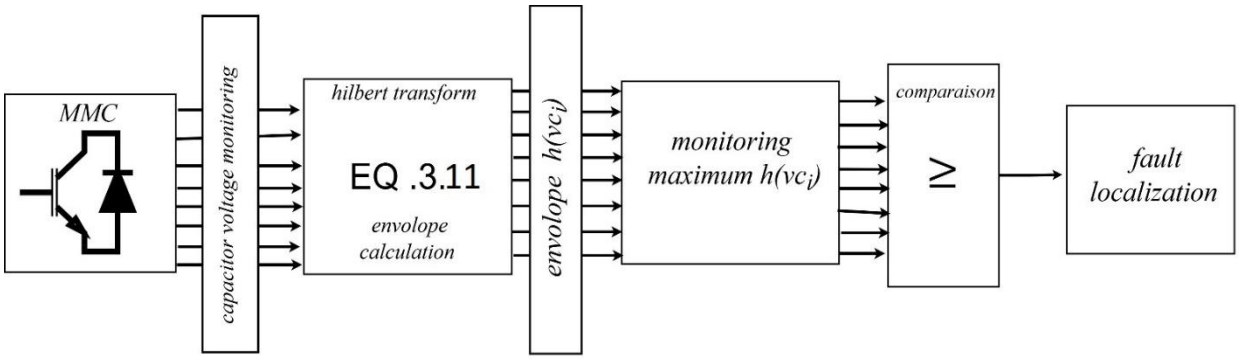


Figure.III. 20: structure of step 2

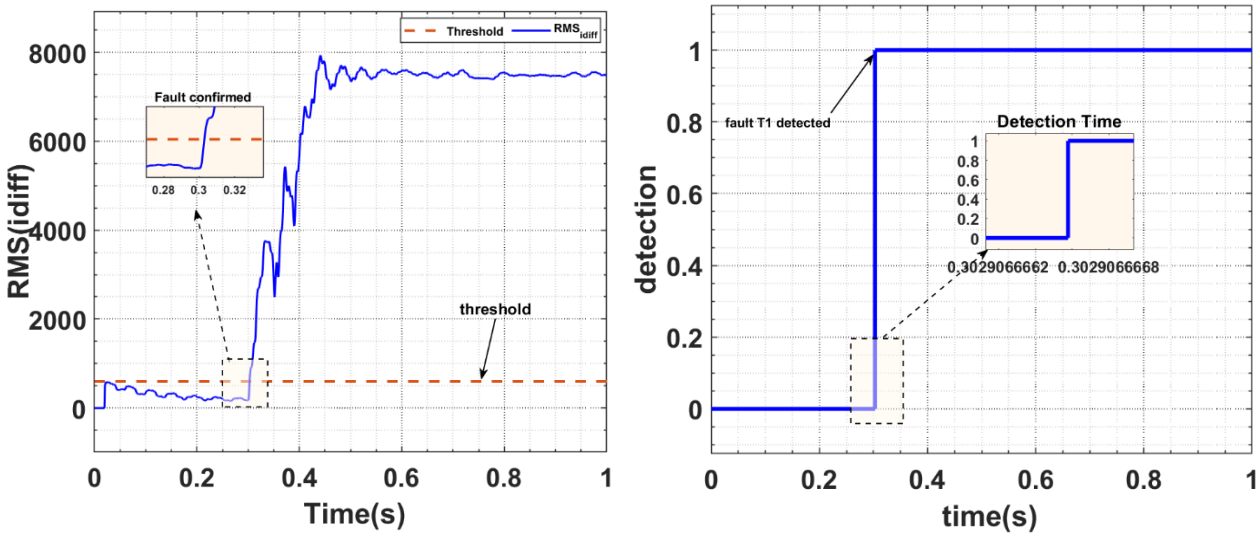
III.4.2. Results and discussion

- The effectiveness of the proposed method was tested using the same MMC setup as in Method 1, with two fault scenarios examined
- **Case 1**: A SCF in T1 of SM1 occurs at **t = 0.03 s**.
- **Case 2**: A SFC in T2 of SM1 occurs at **t = 0.05 s**

III.4.2.1. Faults detection

Timely detection of faults is vital to avoid system damage and maintain reliable operation. This section assesses the efficiency of the proposed RMS-CC-based fault detection method. The results, depicted in Figure.III.s 21 and 22, demonstrate the approach's accuracy, responsiveness, and robustness under diverse operating scenarios.

In Figure.III.s 21 (a), the detection of a T1-type fault is illustrated. Before the fault occurs, the RMS value of the differential current RMS (i_{diff_f}) remains consistently around 200 A, indicating stable and fault-free operation. At t = 0.30 s, a sudden and sharp rise in the RMS value is observed, reaching approximately 8000 A, which exceeds the predefined threshold of 600 A. This significant deviation signals the presence of a fault. Figure.III.s 21 (b) shows the corresponding detection signal shifting from 0 to 1 at t = 0.302 s, precisely identifying the fault initiation. The inset highlights that the fault is detected within nearly 2 ms.



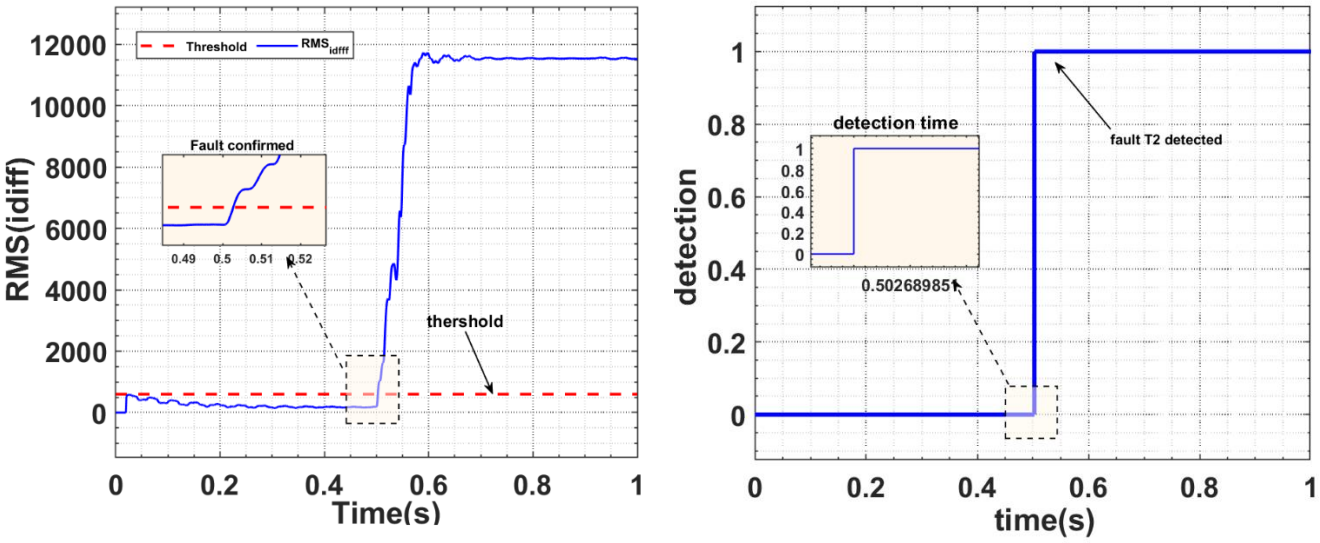
(a) (b)

Figure.III. 21: a) RMS-CC method under T1 fault; b) detection signal

Figure.III.s 22 (a) presents the fault detection process for a T2-type fault. the RMS value of the differential current RMS (i_{diff_f}) remains stable around 200 A during normal operation. However, at t = 0.5027 s, a sudden surge occurs, with the RMS current spiking to nearly 12,000 A

significantly exceeding the defined threshold. This substantial deviation clearly indicates the occurrence of a fault.

Figure.III.s 22 b) shows the detection signal transitioning from 0 to 1 at t = 0.5027 s, precisely pinpointing the occurrence of the T2 fault. As emphasized in the inset, the detection time is approximately 2 ms. These results demonstrate the rapid response and effectiveness of the proposed method in detecting faults, ensuring timely intervention and system protection.



a) b)

Figure.III. 22:a) RMS-CC Methods Under T2 fault; b) detection signal

III.4.2.2. Faults localization:

This section introduces the fault localization strategy, developed as an extension of the previously discussed detection method. In this study, the Hilbert Transform is realized through the Hilbert Filter block available in MATLAB/Simulink. This block implements a discrete-time finite impulse response (FIR) filter that serves as an approximation of the continuous Hilbert Transform

This filter design offers a reliable approximation of the ideal Hilbert Transform across the relevant frequency spectrum, particularly suited for the dynamic and high-frequency nature of capacitor voltage signals in an MMC. Through this FIR-based approach, the analytic signal is generated in

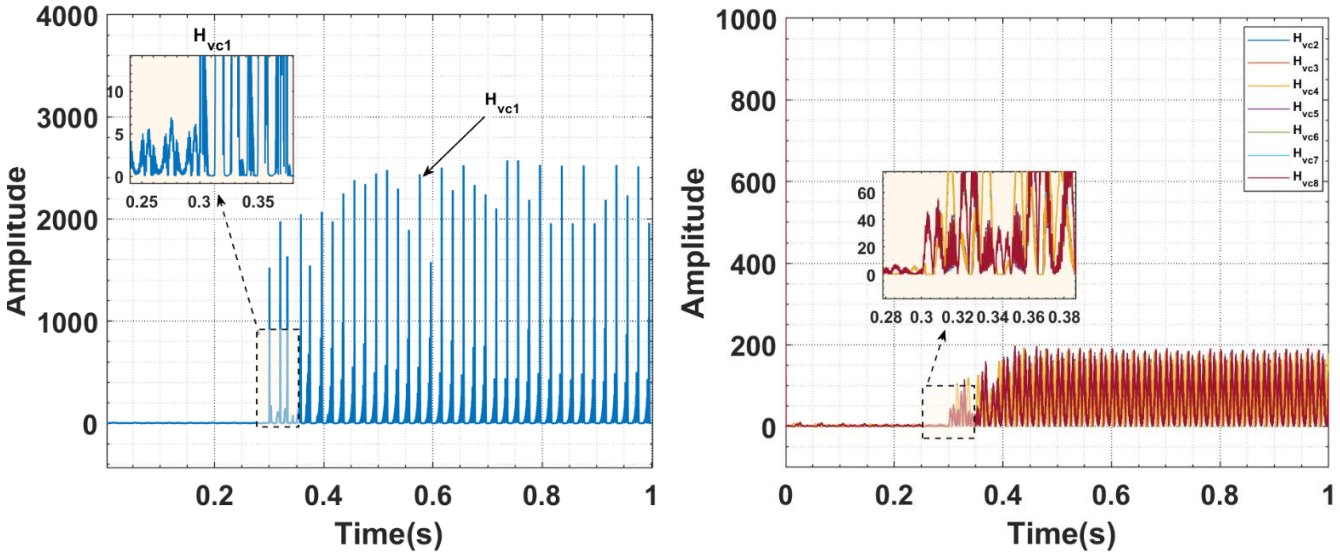
real time, enabling precise extraction of the envelope $|h(t)|$This envelope reveals critical fault-related characteristics that may remain hidden in the original, unprocessed voltage waveform.

A) case 1: A short-circuit fault in T1:

Figure III.23 depicts the capacitor voltage envelopes of all submodules (VC1–VC8). In Figure III.23(a), a sharp rise is observed in the envelope of VC1 (hVC1) at approximately *t = 0.3 s*, which marks the occurrence of the T1 fault. The amplitude of hVC1 reaches nearly 3000, significantly exceeding the values of the other submodules (hVC2–hVC8) shown in Figure III.23(b), where the variations remain close to 200. This clear discrepancy allows easy identification of the faulty submodule (SM1), as the distinct deviation in VC1's envelope serves as a reliable indicator of the fault location.

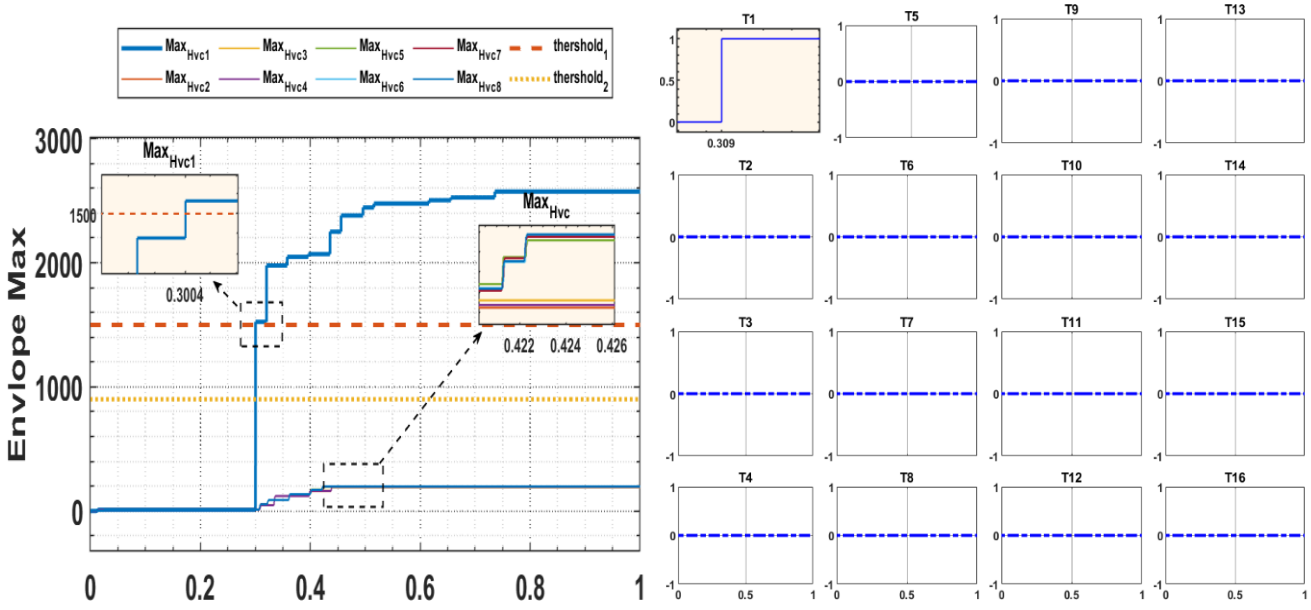
Based on these findings, Figure III.24(a) illustrates the maximum Hilbert Transform envelope values (MAXh) of each submodule over time. A predefined threshold is employed to distinguish between healthy and faulty conditions. At *t = 0.3 s*, MAXhVC1 exceeds this threshold, thereby fulfilling the condition specified in Equation (III.10) and confirming the presence of a fault. Meanwhile, the maximum envelope values of the remaining submodules remain well below the threshold, verifying that the fault is isolated to SM1

Following this, Figure III.24(b) presents the locating signal, which switches from 0 to 1 once the faulty IGBT is identified. This change occurs at *t = 0.3097 s*, correctly pinpointing the defective device (T1 in SM1) with a localization delay of about 0.01 s (10 ms) after the fault occurs. Importantly, the locating signals of all other IGBTs remain at 0, confirming the absence of false detections. These observations demonstrate that the proposed method achieves fast response, high accuracy, and strong reliability in fault localization.



(a) (b)

Figure.III. 23: envelopes under T1 fault; a) The envelope hVC1; b) The envelope hVC's



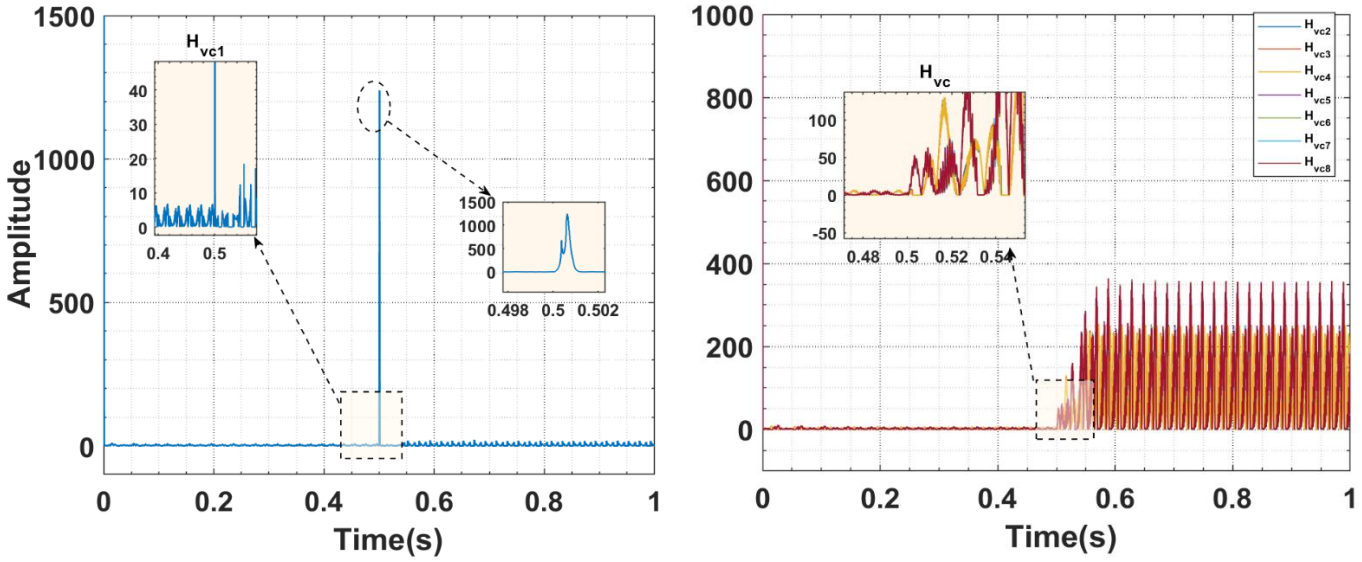
a) b)

Figure.III. 24:a)the maximum values of envelopes under T1 fault, b) the localization signals

B) case 2: A short-circuit fault in T2:

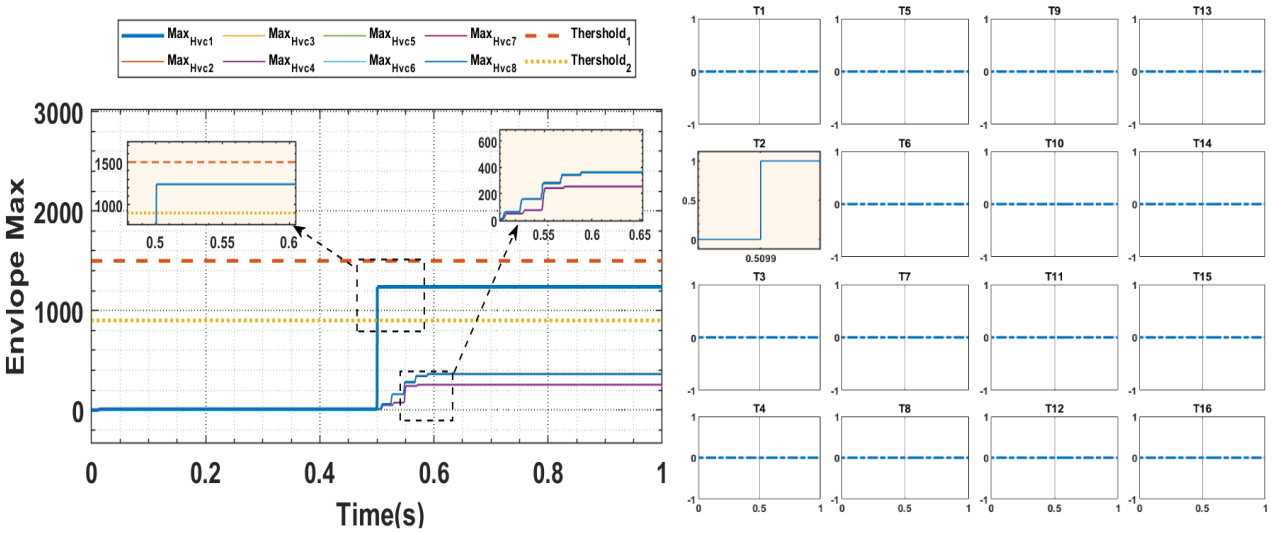
the envelopes of the capacitor voltages for all submodules (VC1–VC8) are shown in Figure III.25. Unlike the previous case, the envelope of VC1 (hVC1) displays a distinct pulse at $t = 0.5\ s$, reaching an amplitude close to 1000, as seen in Figure III.25(a). This pronounced pulse clearly signifies a fault in VC1. Furthermore, Figure III.25(b) demonstrates that the envelope of hVC1 is significantly different from those of the remaining submodules (hVC2–hVC8), reinforcing its reliability in identifying the faulty submodule

The results are reinforced by the analysis of the maximum envelope values shown in Figure III.26(a). At $t = 0.5\ s$, the maximum value of MAXhVC1 increases sharply, surpassing Threshold 2 but remaining below Threshold 1, as defined in Equation (III.11). This behavior is a clear indicator of a T2 fault. Conversely, the maximum envelope values of the other submodules remain well below both thresholds, confirming their healthy operation. Further validation is provided by the localization results in Figure III.26(b), where the signal switches at $t = 0.5098\ s$, precisely identifying the T2 fault. The localization delay is around 0.01 s (10 ms), consistent with Case 1. This fast and accurate localization is essential for the timely mitigation of IGBT short-circuit faults, significantly enhancing the protection, reliability, and robustness of the MMC system.



(a) (b)

Figure.III. 25 :envelopes under T1 fault; a) The envelope hVC1; b) The envelope hVC's



a) b)

Figure.III. 26 a) the maximum values of envelopes under T2 fault, b) localization signal

III.4.2.3. Comparison between different fault diagnosis method for short circuit fault

The comparison table for short-circuit fault detection and localization clearly highlights the advantages of the proposed methods over existing approaches. Reference [11], which combines SVM with Wavelet Transform (WT), does not report detection (FD) or localization (FL) times and achieves only moderate accuracy with moderate complexity. In [89], ANFIS combined with WT provides high accuracy, but both FD and FL times are 30 ms, and the computational complexity is high. Similarly, [90] employs RNN with WT for T1 and T2 faults, but it requires 50 ms for both detection and localization and still maintains high complexity with only moderate accuracy. In contrast, Method 1 (DWT-RBFNN) improves performance by handling T1, T2, and simultaneous T1&T2 faults with high accuracy and moderate complexity, while reducing FD and FL times to 40 ms. More significantly, Method 2 (RMS-CC with Hilbert Transform-based localization) demonstrates a substantial improvement, achieving extremely fast detection (2 ms) and localization (10 ms) with high accuracy and low computational complexity. Overall, the proposed methods especially Method 2—offer a superior trade-off between speed, accuracy, and implementation cost, making them highly suitable for real-time short-circuit fault diagnosis in modular multilevel converters.

Table.III.1: Comparison between different fault diagnosis method for short circuit fault

Ref	Method	Fault type	FD time	FL time	Accuracy	complexity
[11]	SVM +WT	T1, T2	NR	NR	moderate	moderate
[89]	ANFIS +WT	T1	30ms	30ms	high	high
[90]	RNN +WT	T1, T2	50ms	50ms	moderate	high
Method 1	DWT-RBFNN	T1, T2, T1&T2	40ms	40ms	high	moderate
Method 2	RMS-CC HLT	T1, T2	2ms	10ms	high	Low

III.5. Conclusion

In this chapter, two advanced methods for detecting and localizing short-circuit faults in Modular Multilevel Converters (MMCs) were developed and evaluated. The first combines Discrete Wavelet Transform (DWT) for feature extraction with a Radial Basis Function Neural Network (RBFNN) for fault classification, while the second applies direct signal processing to capacitor voltage and current waveforms. Simulation results confirm that both approaches offer fast and accurate detection, effective localization of faulty switches, and adaptability to varying operating conditions. These methods enhance the reliability and safety of MMCs by enabling early and precise fault diagnosis, thereby reducing downtime and preventing system damage.

Chapter IV

Design of Fault-Tolerant Control Strategy for Capacitor Failure

IV.1. Introduction

The reliability of MMCs is highly dependent on the condition of their submodule capacitors, which are fundamental for energy storage, voltage balancing, and ensuring the overall stability of the system [114]. Malfunction or degradation of one or more capacitors can significantly impair converter performance, introduce arm voltage imbalances, and in severe cases, result in system failure. To guarantee continuous and secure operation under such conditions, the adoption of fault-tolerant control (FTC) strategies becomes indispensable [114]. This chapter addresses the design and development of control schemes that enhance the fault tolerance of MMCs against capacitor failures. The discussion begins with an overview of the different types of capacitor faults and their consequences on converter dynamics. Subsequently, methods for fault detection, fault isolation, and system reconfiguration are examined. Finally, a fault-tolerant control framework is proposed, based on logical operators (AND, OR, NOT) integrated with intelligent decision-making strategies, to strengthen system resilience and ensure reliable operation under faulty scenarios.

IV.2 Capacitor Failure: Characteristics and Impact

Capacitor failures in Modular Multilevel Converters (MMCs) exhibit distinct fault characteristics that directly influence system dynamics and reliability. Understanding these characteristics and their impact on converter performance is essential for developing effective fault-tolerant control strategies. This section provides an overview of the typical failure modes of capacitors and examines their consequences on voltage balance, current flow, and overall system stability.

IV.2.1. Characteristics of Capacitor failure

As mentioned in Section I.6.2, capacitor failures in MMCs can generally be classified into three primary fault modes: OCFs, SCFs, and WOFs. Each mode presents distinct electrical signatures and operational consequences, ranging from voltage imbalance and increased ripple to potential converter shutdown. [71].

Capacitor open-circuit faults (OCF): Electrically, when a submodule (SM) capacitor experiences an open-circuit fault (OCF)**,** the faulty capacitor is effectively removed from the arm**.**

As a result, the equivalent capacitance of the arm decreases **(Ceq ↓),** as described in equations (I.9) and (I.10)

With a smaller capacitance, the voltage ripple across each healthy capacitor increases, according to equations (I.11) and (I.12).

The rise in capacitor voltage ripple leads to an abrupt change in the arm voltage waveform [115,116].

Capacitor short-circuit faults (SCF): Electrically, when a short circuit occurs across the capacitor terminals, the voltage across the capacitor is forced to zero because the short circuit provides a very low-impedance path

$$v_c \approx 0 \qquad \text{IV.1}$$

A capacitor stores energy in its electric field:

$$E = \frac{1}{2} C v_c{}^2 \qquad \text{IV.2}$$

As soon as the short circuit appears, the stored energy is released rapidly through the low-impedance path. This results in: The arm voltage imbalance generates a transient circulating current and leading to spikes and harmonic distortion in the load current, Furthermore the Sudden energy dissipation results in local heating and possible device destruction if the fault is not cleared promptly. [117,118].

Capacitor wear-out faults (WOF)

Long-term aging in MMC capacitors leads to a reduction in capacitance (C ↓) and an increase in equivalent series resistance (ESR ↑). These effects degrade the electrical performance by producing higher ripple voltage and additional internal heating within the capacitor. As the degradation is often unequal among submodules, an imbalance in the circulating energy appears, which in turn causes arm voltage imbalance unless active balancing strategies are applied. Over time, the progressive thermal stress further accelerates the aging process, eventually resulting in complete capacitor failure. [114,117].

IV.2.2. Impact of Capacitor failure (open circuit)

In this work, capacitor failure is modeled as an open-circuit fault (OCF). To investigate its effect on the reliability and performance of the Modular Multilevel Converter (MMC), a fault is applied at t=0.25 s in submodule 2 and analyzed using MATLAB/Simulink. This scenario emulates practical capacitor faults within submodules and allows for evaluating their impact on critical system parameters, The open-circuit fault (OCF) was selected for this study because it represents the most frequent and practically observed failure mode in submodule capacitors. In comparison with short-circuit faults (SCFs), which usually result in catastrophic damage and trigger immediate protective shutdown, OCFs tend to occur more progressively and allow the converter to continue operating, albeit with degraded performance. This makes them particularly relevant for analyzing system reliability and fault-tolerant control strategies. Wear-out faults (WOFs), on the other hand, are associated with gradual aging effects such as capacitance reduction or ESR increase; while important, these are long-term degradations that evolve slowly and can often be mitigated by preventive maintenance. By contrast, OCFs can appear suddenly during operation, cause significant imbalance in arm voltages, and strongly affect circulating currents and waveform quality [71,114]. For these reasons, OCFs provide a representative and challenging fault scenario for evaluating the performance of MMC fault-tolerant control schemes.

In Figure.IV. 1, the capacitor voltages of the eight submodules are illustrated. It can be observed that when the fault occurs, Vc_2 exhibits an extreme deviation, almost ten times higher than in normal operation. Such a sharp increase can potentially damage the capacitor and even deactivate the corresponding submodule. The remaining healthy submodules also deviate slightly from their nominal values, dropping from approximately 2500 V to 2200 V, which indicates a loss of voltage balancing across the arm.

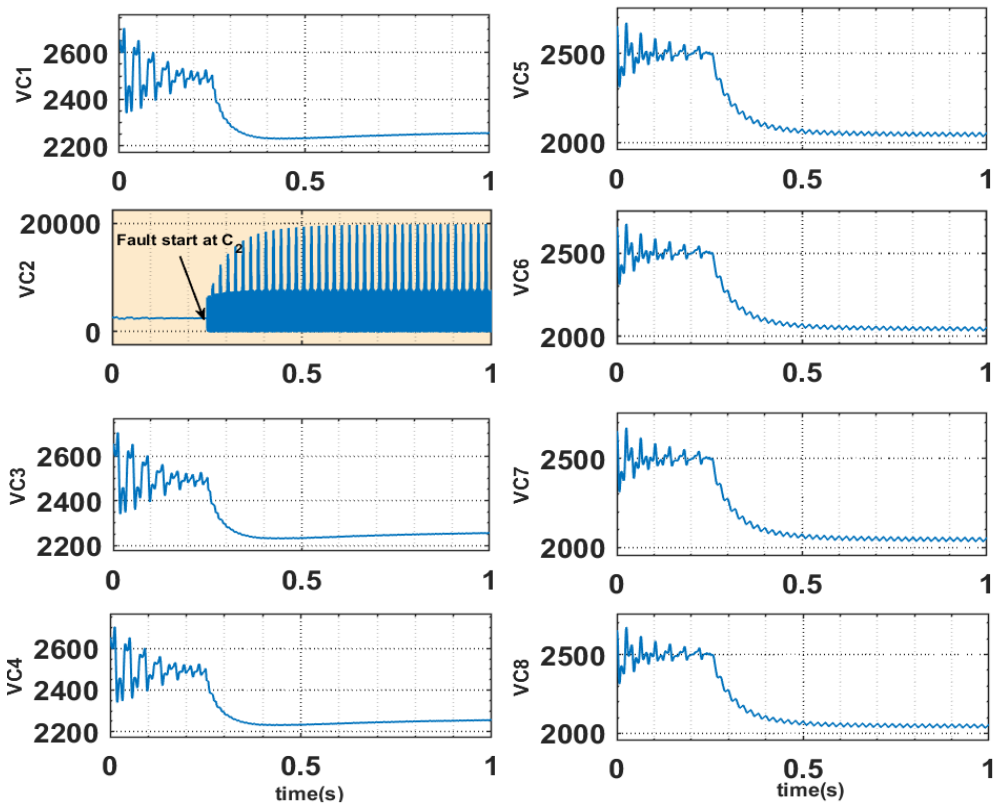


Figure.IV. 1 capacitor voltage under capacitor OFC

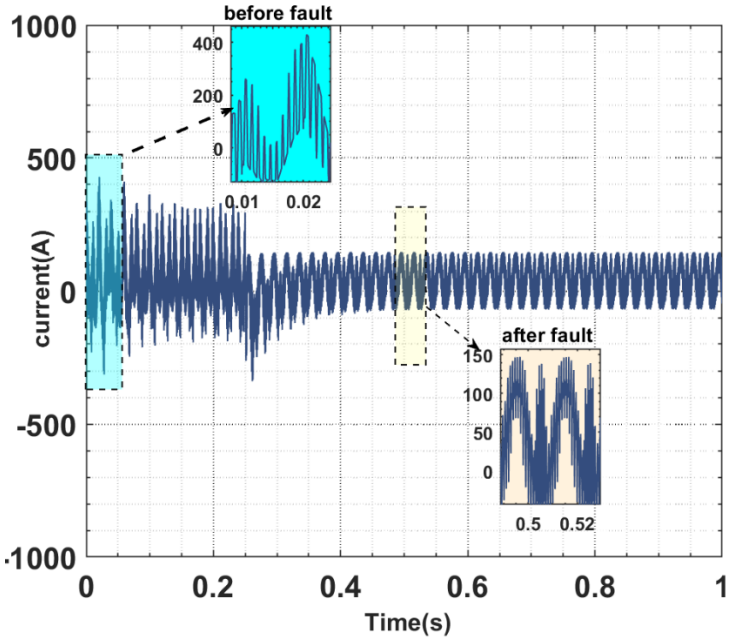


Figure.IV. 2 circulation current under capacitor OCF

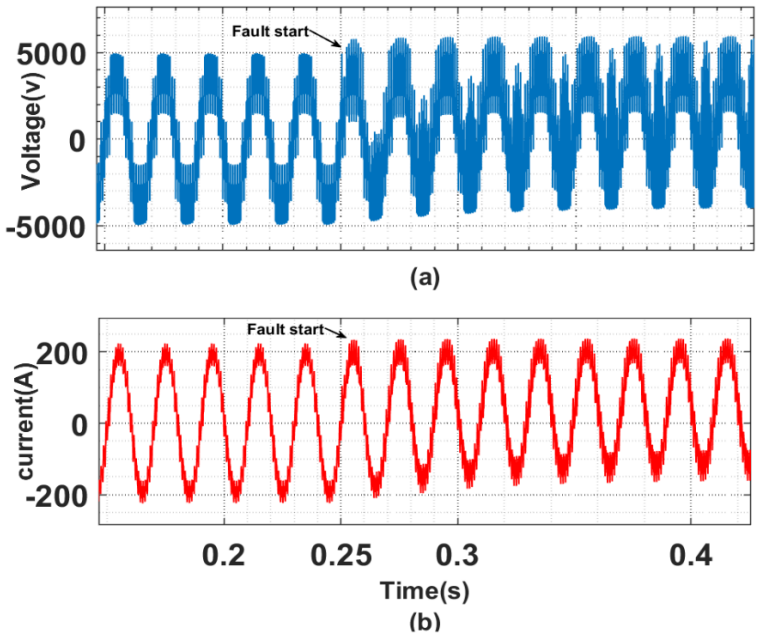


Figure.IV. 3 a) AC voltage b) AC current

On the other hand, Figure.IV. 2 presents the circulating current waveform. As discussed in the previous section, the fault significantly distorts the circulating current, and a clear change in its waveform can be noticed following the fault occurrence. Similarly, Figure.IV.s 3(a) and 3(b) illustrate the AC output voltage and current, both also exhibit waveform distortion, confirming the detrimental effect of a capacitor open circuit fault on the overall performance of converter.

IV.3. Fault Tolerant Control: concept and utilization in MMC

Recently, Fault-Tolerant Control (FTC) has attracted significant attention, as it plays a vital role in improving the reliability, safety, and availability of engineering systems by enabling them to operate continuously under fault conditions. FTC methods are typically classified into two groups: passive and active strategies [119].

IV.3.1. passive strategies

In passive Fault Tolerant Control (PFTC), the controller is designed and tuned in the offline stage, that mean before the system starts operating. Once implemented, it maintains a fixed control behavior under both healthy and faulty conditions. This means that the system does not require a separate fault detection and isolation (FDI) process, since the same control law is applied whether a fault occurs or not see Figure.IV..4. The main advantage of this approach is avoiding fault detection and isolation and its response is very fast due to the elimination of the part of FDI. [120,121].

However, the major limitation is that a single passive FTC design cannot effectively handle a wide variety of faults. Since the controller parameters are pre-determined in the offline design phase, the system may become less efficient or even unstable if the fault type or severity differs from those considered during design. Therefore, while passive FTC offers robustness against certain predefined faults, it lacks the adaptability needed for dealing with unexpected or diverse fault scenarios. [119].

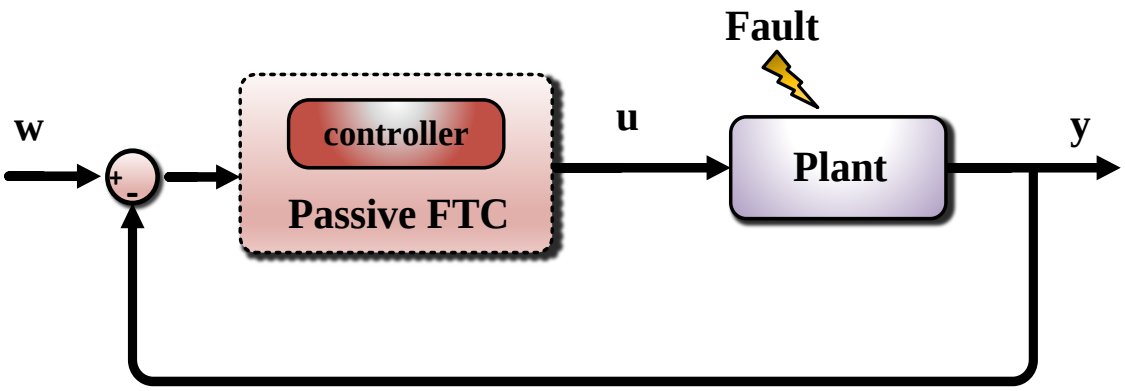


Figure.IV. 4 passive FTC structure

IV.3.2. Active strategies

Active fault-tolerant control (AFTC) methods rely on close interaction with the fault detection strategies, which provides continuous information about the system's health. Once a fault is detected, the control system is reconfigured online to isolate the faulty part and keep the overall plant stable as shows Figure.IV. 5. This online redesign makes the system more flexible and able to deal with unexpected conditions. In some cases, the process may introduce small changes in the desired control behavior or cause slight performance loss, but the system remains operational. A known limitation of active FTC is that it usually takes extra time for fault detection and controller adjustment, which can slow down the response compared to passive solutions. However, the major strength of active FTC lies in its adaptability and wide fault coverage, as it can identify and react to different types of faults, making it highly suitable for complex and safety-critical applications. [122,123].

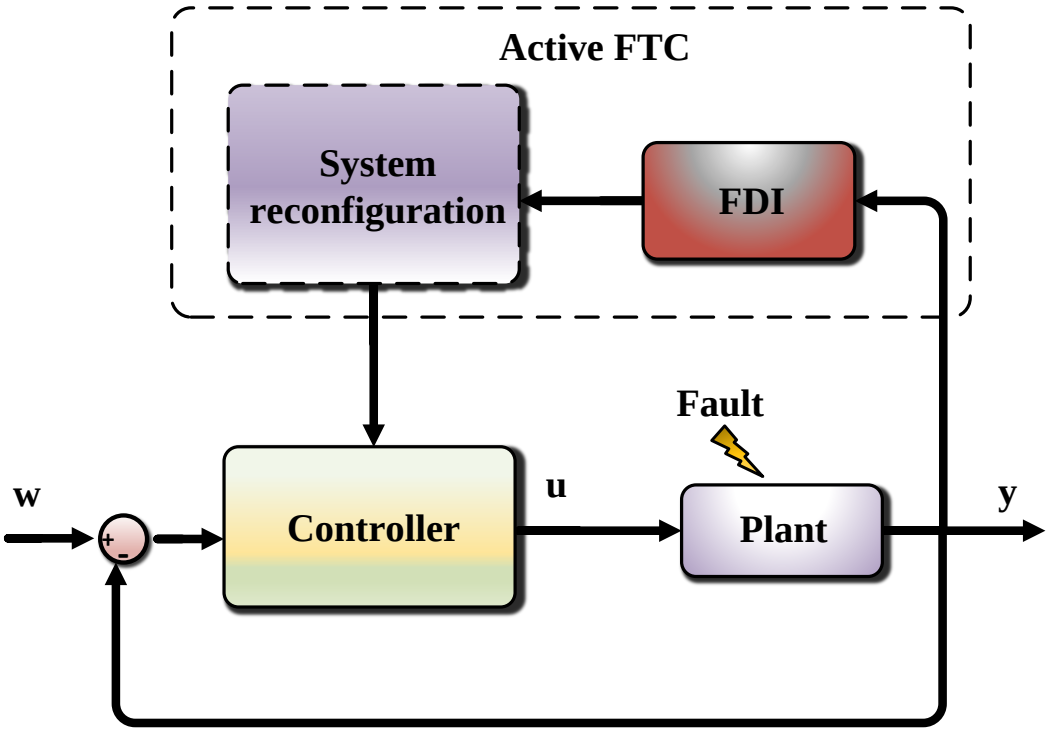


Figure.IV. 5 Active FTC structure

IV.3.3. Fault Tolerant Control in MMC

The Modular Multilevel Converter (MMC) is highly vulnerable to various types of faults, as highlighted in the previous chapters. Since MMCs are often deployed in critical applications where uninterrupted power transfer is essential, ensuring high reliability is a primary concern [124]. To address this challenge, researchers have increasingly focused on developing fault-tolerant control (FTC) strategies tailored for MMCs. Broadly, these strategies can be categorized into two groups: control-based methods, which rely on adaptive reference voltage adjustment and advanced modulation techniques to maintain stable operation, and hardware-based methods**,** which use redundancy mechanisms, such as additional submodules or spare components, to continue operation in the presence of faults. [125].

IV.3.3.1. Control-based methods

According to the literature, control-based fault-tolerant methods in MMCs can generally be categorized into two main approaches**:** adaptive reference voltage control and modulation-based control**.** [125].

A) adaptive reference voltage control

This category mainly focuses on adjusting the reference voltage of the converter to compensate for faulty submodules. Two main techniques are commonly reported:

Capacitor Voltage Increasing (CVI) Method: The capacitor voltage of one or more healthy SMs in the faulty arm is adjusted to balance the missing voltage [126,127]. Although straightforward, this approach reduces the total number of available voltage levels and can stress the SM switches and capacitors, especially in high-voltage applications. [128].

Zero-Sequence Voltage Injection (ZSVI) Method: A DC offset or third-harmonic component is injected into the phase voltages to achieve balanced output under fault conditions [129]. Variants such as the Third-Harmonic Voltage Injection (THVI) and Neutral-Shift (NS) methods are widely studied, as they allow better utilization of healthy SMs while keeping the system balanced. [130,131].

These approaches are attractive for their ability to maintain operation without major hardware modifications. However, they may introduce additional voltage stress and harmonic distortion if not carefully designed.

B) Modulation based control

Modulation adjustments provide another path to fault tolerance by altering how submodules are switched during faults. Two common approaches are:

PWM-Based Methods: Modified space vector modulation (SVM) and phase-shifted carrier PWM (PSC-PWM) are used to bypass faulty SMs while maintaining a balanced three-phase output [132,133]. Sorting algorithms are often combined with PWM schemes to determine which SMs to insert dynamically, reducing computational burden and ensuring faster fault response [134].

Overmodulation Methods: For high-voltage DC (HVDC) applications, MMCs may operate in overmodulation mode to maximize AC voltage. Under fault conditions, operating in this region allows additional voltage headroom and maintains stable. output, though at the cost of increased harmonic distortion [135-137].

These methods enhance the converter's ability to tolerate faults without additional hardware, but they require sophisticated control algorithms and precise coordination between arms which make them complex

IV.3.3.2. Hardware-Based Methods

General hardware-based fault-tolerant methods in MMCs rely primarily on redundancy. This approach is considered one of the most reliable ways to achieve fault-tolerant control, since redundant components (such as extra submodules, switches) can be seamlessly integrated into the converter to replace faulty ones. By reconfiguring the circuit and activating the redundant elements, hardware-based strategies ensure continued operation with minimal disturbance to power quality and system stability. [125].

A) redundant submodules

When employing redundant submodules for fault tolerance, the principle is to bypass the faulty submodule and seamlessly introduce a spare redundant one, while maintaining continuous operation of the MMC. This approach is typically implemented in two main modes [125].

Hot Reserve Mode: In hot-reserve redundancy schemes, the redundant submodules (SMs) are not kept idle but instead remain active during normal operation [138-140]. Their capacitor voltages are maintained at a lower level than those of the primary SMs, which helps distribute the workload more evenly [141,142]. This approach brings several benefits, such as lowering the voltage stress on individual SMs and reducing circulating currents within the converter. In the event of a fault, the faulty module is bypassed, and the output voltages of the remaining healthy SMs are automatically increased to compensate and restore the rated output voltage of the affected phase.

Compared to cold-reserve methods, hot-reserve redundancy provides faster fault recovery since the redundant SMs are already in operation, minimizing transition delays. However, this comes at

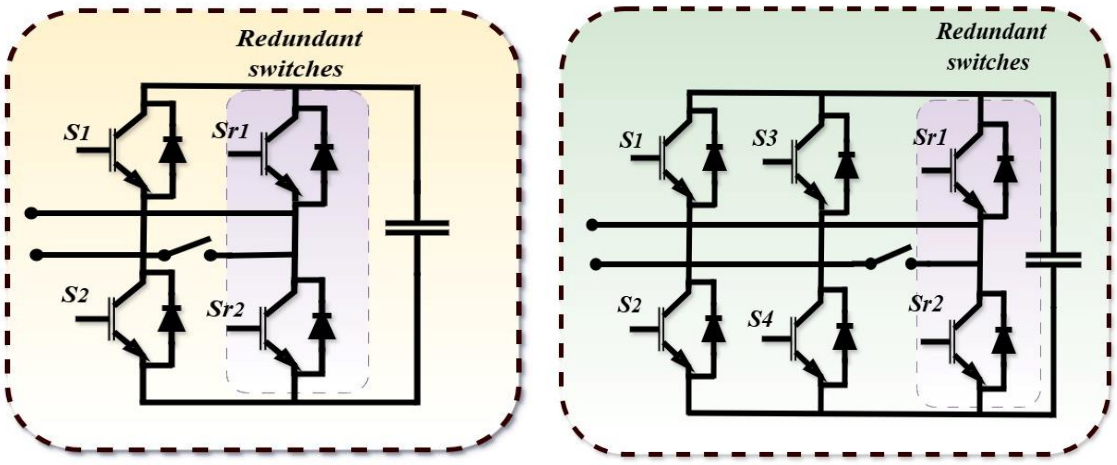
the expense of higher switching and conduction losses due to the continuous involvement of all SMs, including the redundant ones. In addition, the control system becomes more complex, and overall efficiency may be reduced. While harmonic performance remains similar to cold-reserve redundancy, the higher operational losses and the need for tighter voltage balancing among all SMs make hot-reserve strategies less energy-efficient and more costly in long-term operation. [146].

Cold Reserve Mode In cold-reserve redundancy strategies, the capacitors of the active submodules (SMs) are maintained at their rated voltage level, while the redundant SMs remain bypassed during normal operating conditions. This approach has been widely investigated as an effective fault-tolerant technique for Modular Multilevel Converters (MMCs). In such configurations, spare SMs are kept inactive and uncharged under normal conditions and are only inserted into the circuit when a fault is detected in one of the active modules. This operating principle reduces capacitor degradation and extends the service life of redundant SMs, since they are not continuously exposed to electrical stress or thermal cycling [143,144]. When a fault occurs, seamless transition control strategies are employed to insert the cold-reserve SMs rapidly, thereby ensuring uninterrupted power transfer and minimizing transient disturbances [144]. More recently, research has focused on hybrid redundancy concepts that combine both cold- and hot-reserve SMs, enabling a flexible transition between pre-charged (hot) and non-pre charged (cold) modules. Such hybrid topologies provide a balance between fast fault recovery and long-term reliability enhancement [145,146]. In medium-voltage applications, cold-reserve redundancy has proven to be a cost-effective and reliable solution for fault-tolerant operation, particularly in hybrid MMC architectures designed for distributed generation and HVDC systems [147]. Overall, cold-reserve redundancy represents a key enabler for improving fault ride-through capability, converter availability, and operational reliability, while simultaneously mitigating the drawbacks associated with continuous capacitor utilization.

B) Redundant IGBTs

Normally, a Modular Multilevel Converter (MMC) submodule (SM) consists of two IGBTs in the half-bridge configuration or four IGBTs in the full-bridge configuration. A fault in a single IGBT, whether an open-circuit or a short-circuit, can disable the entire submodule and compromise the

operation of the converter. To enhance reliability, redundant IGBT based fault-tolerant strategies introduce additional backup switches into each SM, together with a high-speed AC switch for rapid fault isolation. In this scheme, the number of switching devices increases from 2 to 4 in half-bridge SMs Figure.IV. 6.a , and from 4 to 6 in full-bridge SMs Figure.IV. 6.b [148].



a) b)

Figure.IV. 6 MMC submodule with redundant IGBT: a) half bridge, b) full bridge

The working principle is as follows: under normal operation, only the primary IGBTs conduct, while the redundant devices remain inactive. When a fault occurs in a main switch, the control system detects it and immediately adjusts the gate signals, bypassing the faulty device and activating the redundant IGBT. This seamless transition ensures that the submodule continues to operate without shutting down, thereby maintaining converter performance and system stability [148,149].

One of the main advantages of this approach is that it allows the converter to continue operating without the need to bypass or remove faulty submodules, thereby improving system availability and reliability. However, this benefit comes with certain drawbacks. The use of redundancy management requires additional gate drivers and more complex control logic, which increases the overall system cost and implementation effort. Furthermore, the higher number of devices involved leads to increased switching and conduction losses, which reduce efficiency. As a result,

while the approach enhances fault tolerance, it also makes the overall configuration more complex. [150].

IV.4.the proposed fault tolerant control

IV.4.1. overview of the method

From the previous section, it is evident that most fault-tolerant control (FTC) strategies reported in the literature are either complex to implement or exhibit slow response times. Moreover, the majority of these studies primarily address IGBT faults. This gap has motivated the authors to propose a simple and fast FTC method specifically designed for capacitor failures. Unlike redundant submodule (SM)-based approaches, the proposed method offers faster fault handling while maintaining reliable fault behavior.

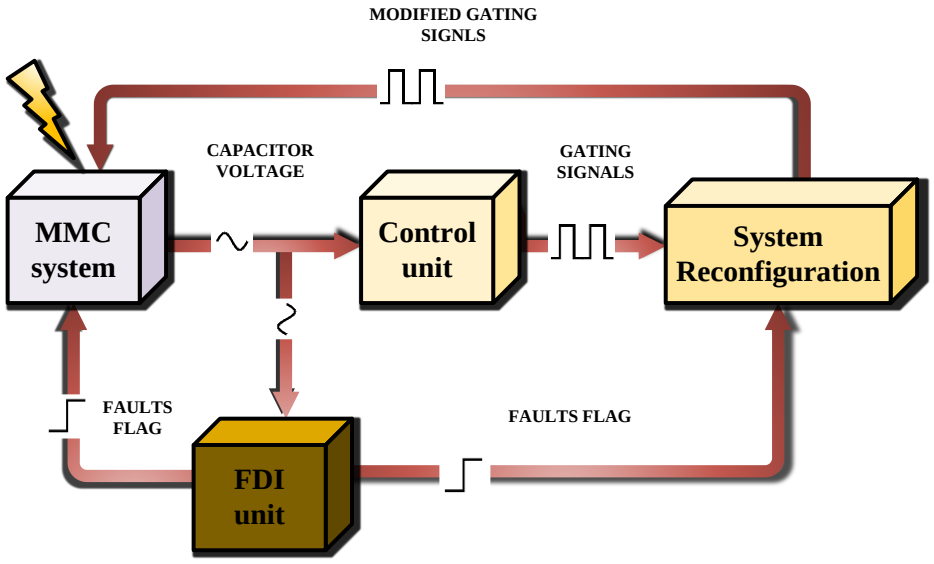


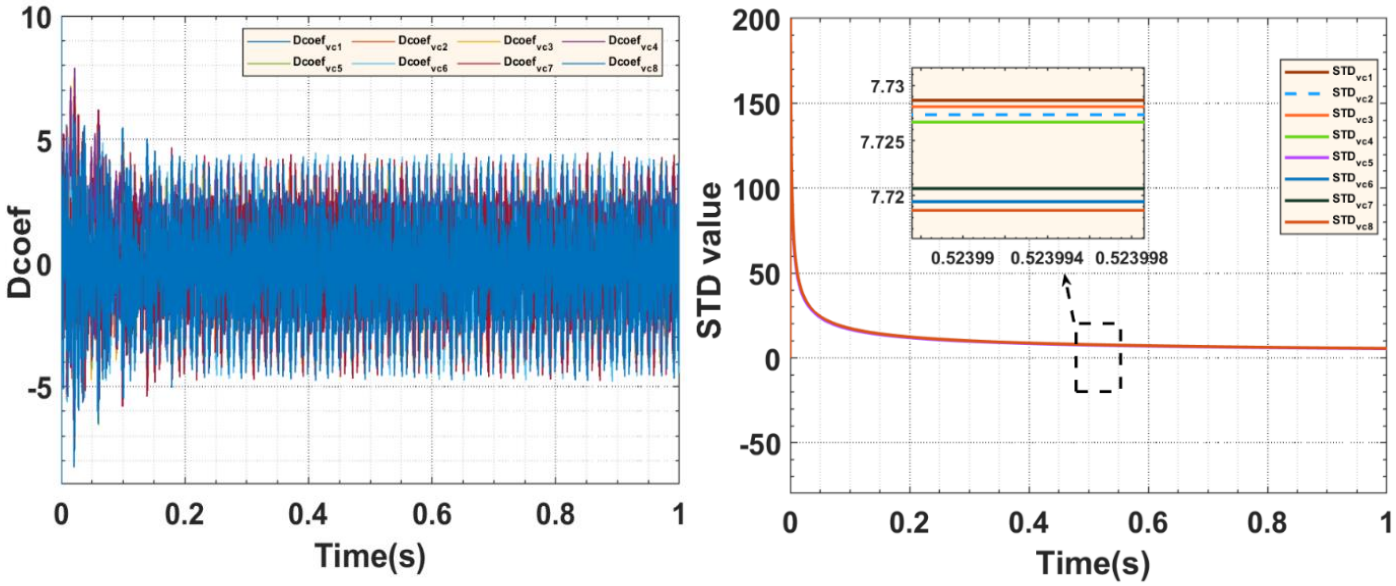
Figure.IV. 7 the overall schema of the proposed FTC strategy

Since the proposed Fault-Tolerant Control (FTC) strategy operates in an online mode, it is organized into three sequential stages. In the first stage, fault detection and identification (FDI)**,** a predefined Artificial Neural Network (ANN) model is utilized to accurately detect and identify capacitor failures in real time. Once a fault is detected, the second stage, fault isolation**,** is immediately activated, where the faulty submodule is bypassed through a fault flag generated by the FDI unit, ensuring that the fault is isolated from the rest of the converter.

Finally, in the third stage, system reconfiguration**,** a logic-gate-based control circuit dynamically manages the switching sequence, enabling the converter to restore normal operation and maintain reliability with minimal performance degradation the overall schema of the proposed strategy is presented in Figure.IV. 7. The detailed design and practical implementation of these three stages are presented in the following sections.

IV.4.1.1. Fault Detection and Identification Unit (FDIU)

The most critical aspect of fault-tolerant control is fault detection and identification (FDI)**,** as it plays a decisive role in the overall effectiveness of the strategy. The detection process must be both fast and accurate to ensure that the subsequent stages of fault isolation and system reconfiguration are carried out correctly. Any mismatch between the FDI unit and the other control units can compromise the entire process, leading to unreliable operation. To fulfill this requirement, an Artificial Neural Network (ANN) model is employed for detecting capacitor failures, providing high accuracy and real-time performance.

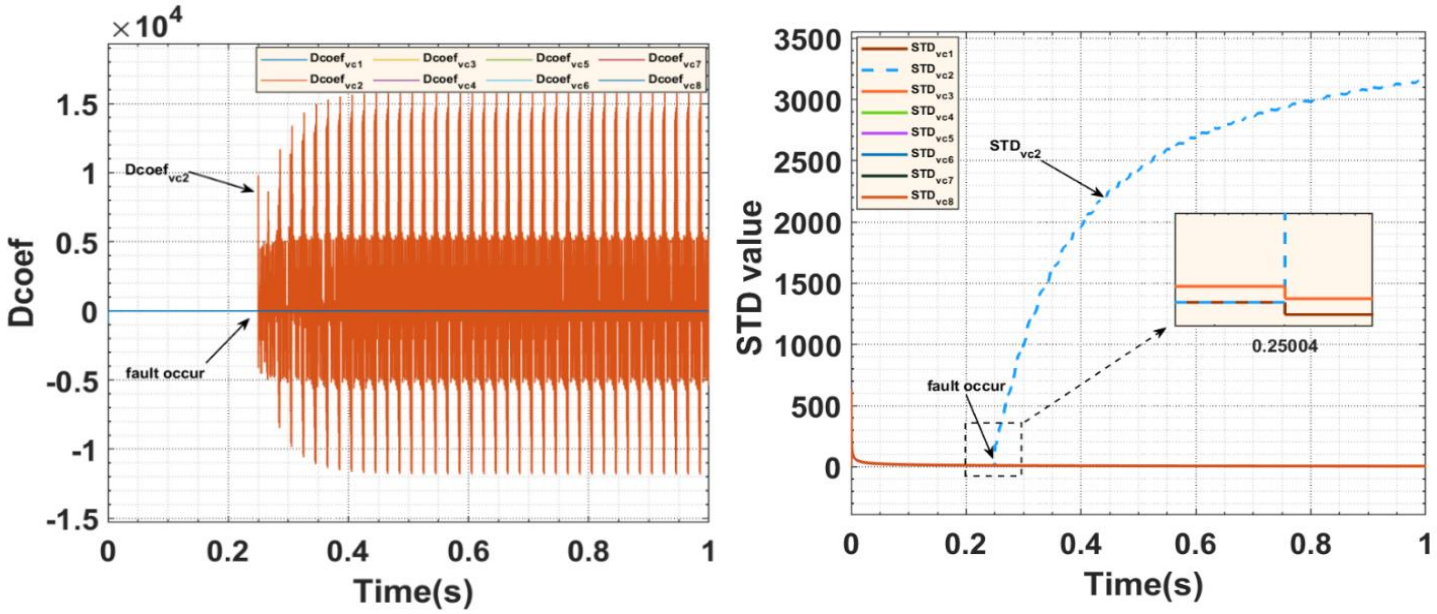


a) b)

Figure.IV. 8 features under healthy case: a) the detail coefficients of the capacitor voltage, b) the standard deviation values of the detail coefficients

To ensure the accuracy and precision of the ANN model, it must be trained with a well-structured and representative dataset. For this purpose, the standard deviation of the detail coefficients obtained from a one-level Discrete Wavelet Transform (DWT) was employed as the feature extraction technique, capturing the dynamic characteristics of the capacitor voltage in the MMC.

Figure.IV. 8.a presents the detail coefficients of the capacitor voltage during the healthy operation of the system. As can be observed, all eight signals converge within the range of approximately **±5**, following an identical pattern without noticeable deviation. Similarly, in Figure.IV.8.b, the standard deviation values of the detail coefficients show no abnormal behavior, with all plots evolving smoothly around a value of **7**, which further confirms the stable operation of the MMC under healthy conditions.



a) b)

Figure.IV. 9 features under fealty case: a) the detail coefficients of the capacitor voltage, b) the standard deviation values of the detail coefficients

An open-circuit fault was applied to the capacitor of Submodule 2 at t = 0.25 s. As illustrated in Figure.IV. 9.a, a sharp and significant deviation appears in the detail coefficients of VC2 immediately after the fault occurs, while the other healthy capacitor voltages remain within the

normal operating range. Furthermore, Figure.IV. 9.b shows that the standard deviation of the detail coefficients for Submodule 2 exhibits a pronounced increase, reaching a value close to 3000, whereas the standard deviation of the healthy submodules remains within the expected range of normal operation. This clear contrast confirms both the presence of a fault in capacitor 2 and the effectiveness of the proposed feature extraction technique in distinguishing faulty from healthy conditions.

Table.IV. 1 the structure of the dataset

CASES	Target
Healthy	00000000
Faulty capacitor 1	10000000
Faulty capacitor 2	01000000
Faulty capacitor 3	00100000
Faulty capacitor 4	00010000
Faulty capacitor 5	00001000
Faulty capacitor 6	00000100
Faulty capacitor 7	00000010
Faulty capacitor 8	00000001

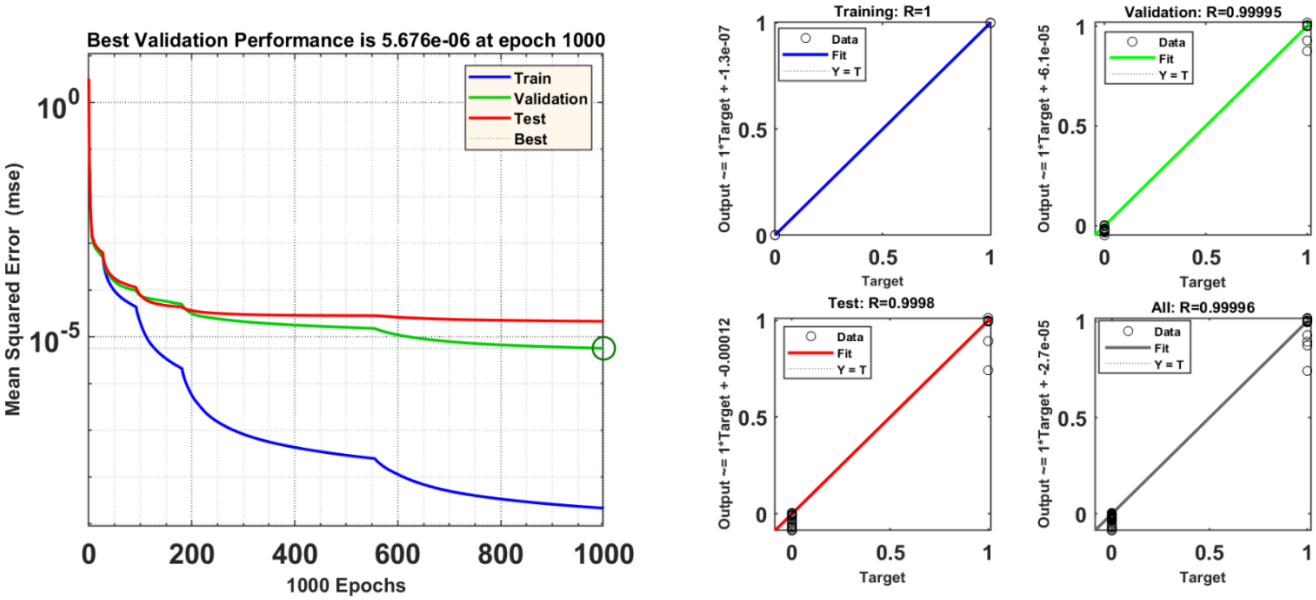
Table.IV. 1 presents the structure of the dataset employed in this study. It summarizes the organization of data collected under both healthy and faulty operating scenarios. Each entry in the dataset consists of the detail coefficients extracted from the capacitor voltage signals using the DWT, the corresponding normalized values obtained through standard deviation, and the classification label indicating the capacitor condition. In this labeling scheme, 1 denotes the presence of a fault, while 0 represents a healthy capacitor.

The constructed dataset is subsequently used to train the artificial neural network (ANN) model. The parameters and training configuration of the proposed ANN are summarized in Table.IV. 2

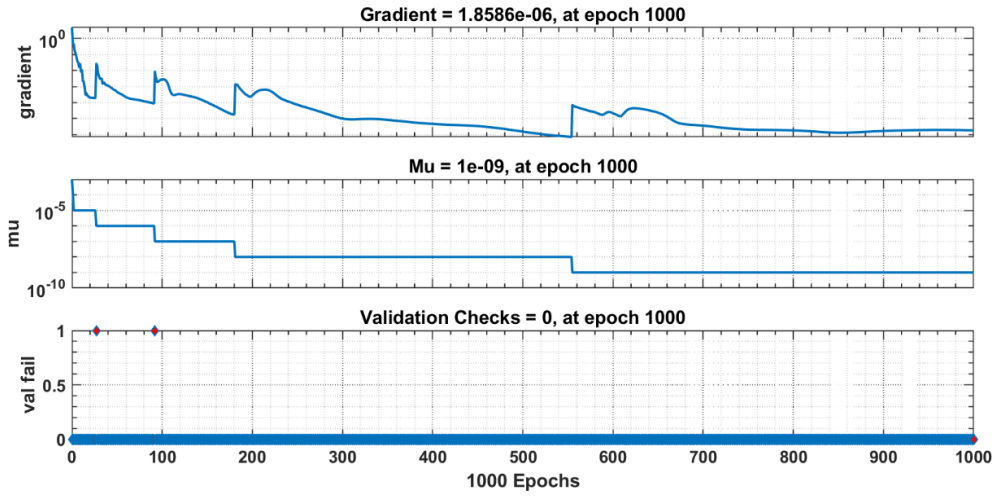
Table.IV. 2 The parameters and training configuration of ANN model

Parameter	Value/method
Input data	8X4509
Outpudata	8X4509
Number of layers	3
Number of neurons Input layer	8
Number of neurons Hidden layer	15
Number of neurons Output layer	8
Training function	Levenberg–Marquardt (TRAINLM)
Adaptation learning function	Gradient Descent with Momentum (learngdm)
Transfer function	Hyperbolic Tangent Sigmoid (TANSIG)
Performance function	MeanSquared Error (MSE)
Number of epochs	1000
Validation approach	Hold-Out Validation

The Levenberg–Marquardt (TRAINLM) algorithm was selected as the training function due to its fast convergence and robustness for medium-scale networks. The TANSIG transfer function was employed in the hidden layer as it effectively captures nonlinear relationships, which are inherent in the MMC fault dynamics. To ensure stable learning, gradient descent with momentum (learngdm) was adopted, which prevents oscillations and accelerates convergence. The performance of the ANN was evaluated using the mean squared error (MSE), providing a reliable measure of prediction accuracy. The network was trained for 1000 epochs with a hold-out validation strategy, where a portion of the dataset was reserved for validation to avoid overfitting and to assess the generalization capability of the model.



a) b)



c)

Figure.IV. 10 ANN evaluation: a) performance, b) regression, c) Training Progress

The training performance of the proposed ANN model is illustrated in Figure.IV. 10.a. The mean squared error (MSE) curve demonstrates a rapid decrease during the initial epochs, stabilizing after approximately 300 iterations and reaching its minimum value at epoch 1000. The best validation performance is recorded at 5.67×10^{-6}, which confirms the high accuracy and

effectiveness of the feature extraction and classification process. Importantly, the validation and testing error curves follow the training curve closely, without any significant divergence, which indicates that the network has successfully avoided overfitting and exhibits strong generalization capability.

The regression plots for training, validation, testing, and the overall dataset in Figure.IV. 10.b further confirm this performance. All correlation coefficients (R) are extremely close to unity, with values of R = 1.0 for training, R = 0.99995 for validation, R = 0.9998 for testing, and R = 0.99996 for the complete dataset. This near-perfect correlation demonstrates that the ANN outputs match the target labels with negligible deviation, ensuring reliable fault detection and classification of capacitor failures in MMC submodules.

The gradient evolution, shown in Figure.IV. 10.c, steadily decreases throughout the training process, reaching 1.85×10^{-6} at epoch 1000, which indicates that the optimization process has effectively converged to a minimum error solution. Similarly, the adaptive learning rate parameter ($\boldsymbol{\mu}$) decreases and stabilizes at $\mathbf{10^{-9}}$, further confirming stable convergence of the learning algorithm. The validation check counter remains at zero, signifying that no early stopping occurred and that the model consistently improved until the maximum epoch was reached.

IV.4.1.2. Fault Isolation

When an open-circuit fault occurs in a capacitor, the MMC loses its voltage balancing capability. This imbalance propagates through the system, leading to abnormal circulating currents, distorted output voltages, and possible overvoltage or overcurrent stresses on other components. To prevent further damage and maintain safe operation, it is essential to bypass the faulty submodule and exclude it from the converter operation.

In this work, a bypass mechanism is implemented in MATLAB/Simulink based on the output of the trained ANN. The ANN produces eight binary signals, each corresponding to the health state of one capacitor in the converter arm. Under normal operation, all signals remain at zero, indicating that all submodules are healthy. When a capacitor fault occurs, the ANN output corresponding to the faulty capacitor switches from 0 to 1

This transition triggers a bypass breaker associated with the affected submodule. The breaker model is configured such that:

- If the ANN output = 0 the breaker remains open, and the submodule continues normal operation.
- If the ANN output = 1 the breaker closes at the fault instant, thereby bypassing the faulty submodule.

The bypass signal (denoted as BP) ensures that the current can flow through the submodule branch without interruption while isolating the faulty capacitor. This strategy prevents the propagation of unbalanced capacitor voltages to the entire converter system and ensures the continuity of MMC operation until further reconfiguration or redundancy-based strategies are applied. (Figure.IV. 11).

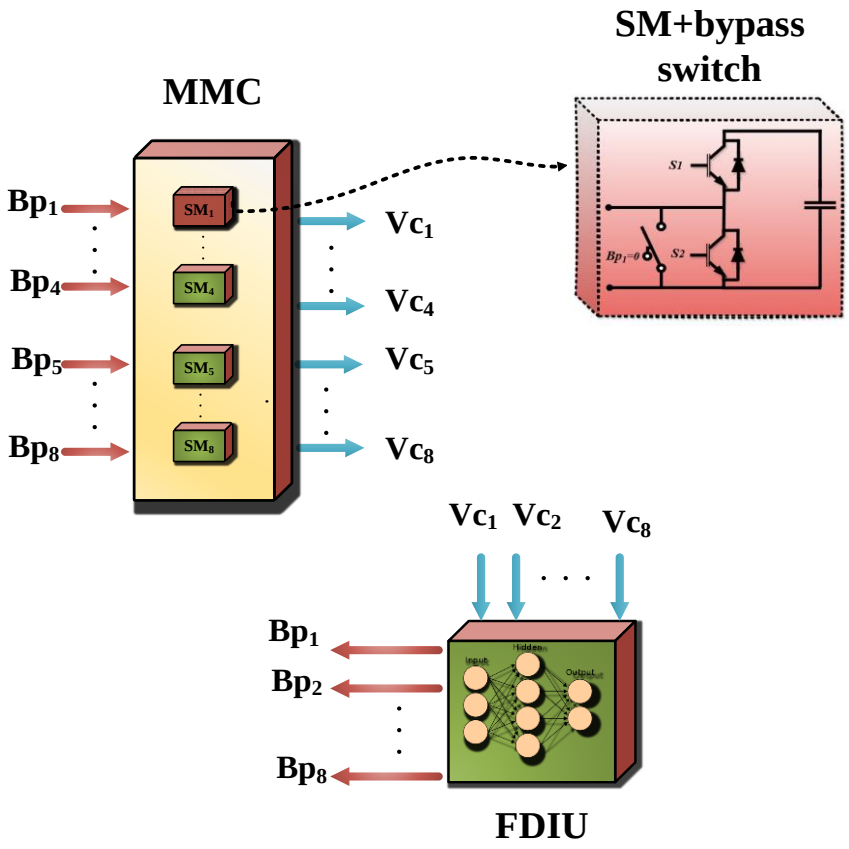


Figure.IV. 11 the bypass of the faulty SM mechanism

IV.4.1.3. System Reconfiguration

After bypassing a faulty submodule (SM), the Modular Multilevel Converter (MMC) loses one of its nominal cells. This reduction directly affects the available number of voltage levels, which leads to an imbalance in the arm voltages and a deterioration of the output waveform quality. To guarantee safe and reliable operation even under such conditions, a reconfiguration mechanism is introduced.

The reconfiguration strategy is based on the inclusion of cold redundant submodules. These redundant SMs remain inactive under normal operation and are only activated once a fault is detected and the corresponding faulty SM is bypassed. By switching in the redundant unit, the MMC restores its nominal number of active submodules, thus maintaining voltage balancing and minimizing distortion in the output voltage. The number of redundant SMs per arm is determined by the required reliability level, with practical implementations often including 10%–20% redundancy [37]. This tradeoff balances improved fault tolerance against increased cost and reduced utilization rates.

Mathematically, if the MMC has N_{SM} submodules per arm and N_r redundant submodules, the effective number of operational submodules is given as:

$$N_{eff} = N_{SM} + N_r - N_f \qquad \text{IV.3}$$

where:

N_{SM} = number of nominal submodules per arm,

N_r = number of redundant submodules per arm,

N_f = number of faulty submodules per arm.

In the studied case of a five-level MMC, each arm consists of N_{SM} =4 nominal submodules. To enhance fault tolerance, one redundant cold submodule is added per arm (both upper and lower)

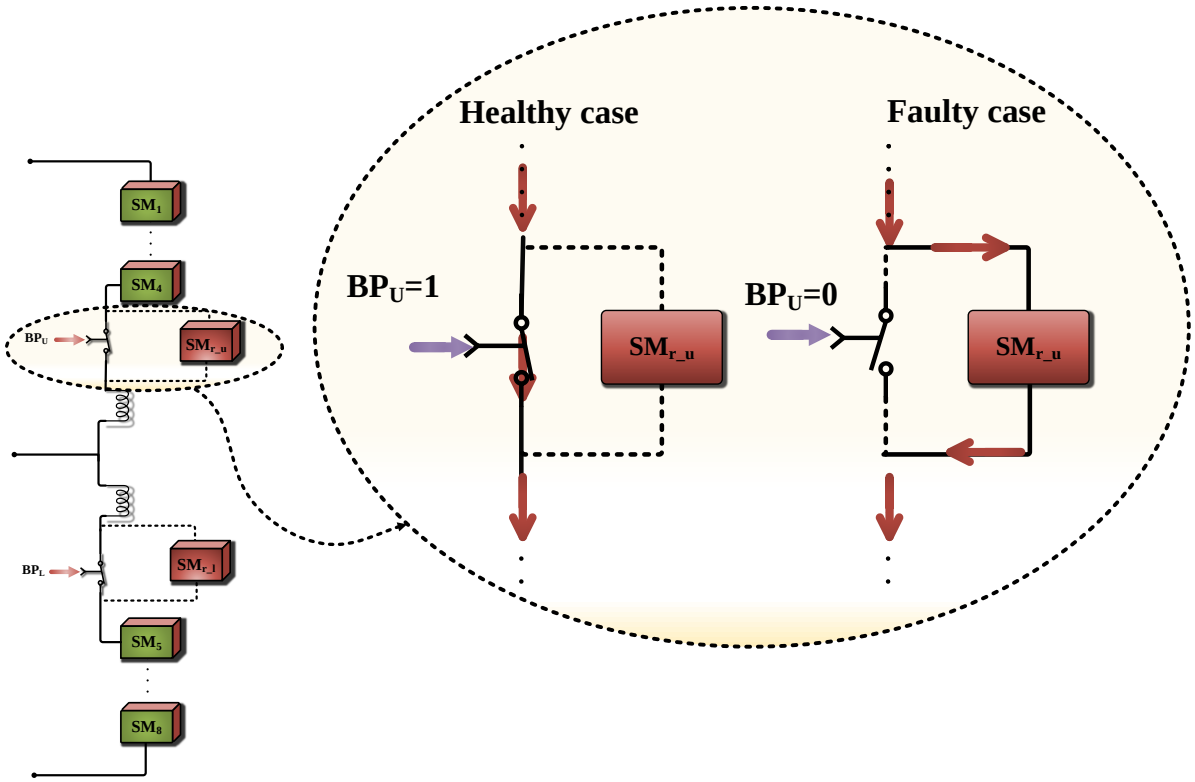


Figure.IV. 12 The integration of the redundant SM mechanism

The integration of the redundant submodule (SM) into the Modular Multilevel Converter (MMC) is governed by the output of the Fault Detection and Identification Unit (FDIU)**.** As explained in the previous section, the FDIU generates eight binary signals (BP1, BP2… BP8), where:

- BP1 to BP4 correspond to the health status of the submodules in the upper arm**,**
- BP5 to BP8 correspond to the submodules in the lower arm**.**

In the case of insertion each signal takes the value:

$$Bp_{u,L}\begin{cases}1, healthy\ case\\ 0, feauty\ case\end{cases}$$

Where the equation of the $Bp_{u,L}$ is:

$$Bp_u = \overline{Bp_1 + Bp_2 + Bp_3 + Bp_4} \quad \text{IV.4}$$

$$Bp_l = \overline{Bp_5 + Bp_6 + Bp_7 + Bp_8} \quad \text{IV.5}$$

Based on these fault flags, the insertion mechanism of the redundant SM operates dynamically. As illustrated in Figure.IV. 12, a controllable switch is placed in series with the arm of the MMC, while a cold redundant SM is connected in parallel to this switch.

- **Healthy case ($Bp_{u,L} = 1$)**

When the FDIU indicates that the submodule is healthy, the control signal $Bp_U=1$ keeps the series switch closed (ON)**.** In this condition, the arm current flows directly through the switch, while the redundant SM remains bypassed and inactive. This ensures that the redundant unit does not interfere with the operation of the MMC under normal conditions.

- **Faulty case ($Bp_{u,L} = 0$)**

Once a fault is detected, the FDIU generates a signal $Bp_U=0$, which forces the series switch to open (OFF)**.** With the main path interrupted, the arm current is redirected through the redundant SM. The redundant unit thus becomes fully inserted into the circuit, compensating for the faulty submodule and maintaining the nominal number of operating cells in the arm.

This mechanism ensures that the redundant submodules (SMs) are engaged only under fault conditions, thereby providing an on-demand fault-tolerant capability without interfering with the converter's normal operation. Since redundant SMs remain in a cold (inactive) state until they are required, their capacitor voltages must be incorporated into the sorting algorithm only upon activation. Consequently, a modification of the conventional capacitor sorting algorithm is necessary. As the system under study is originally designed to operate with only four active SMs, the baseline sorting process is limited to the corresponding four capacitor voltages

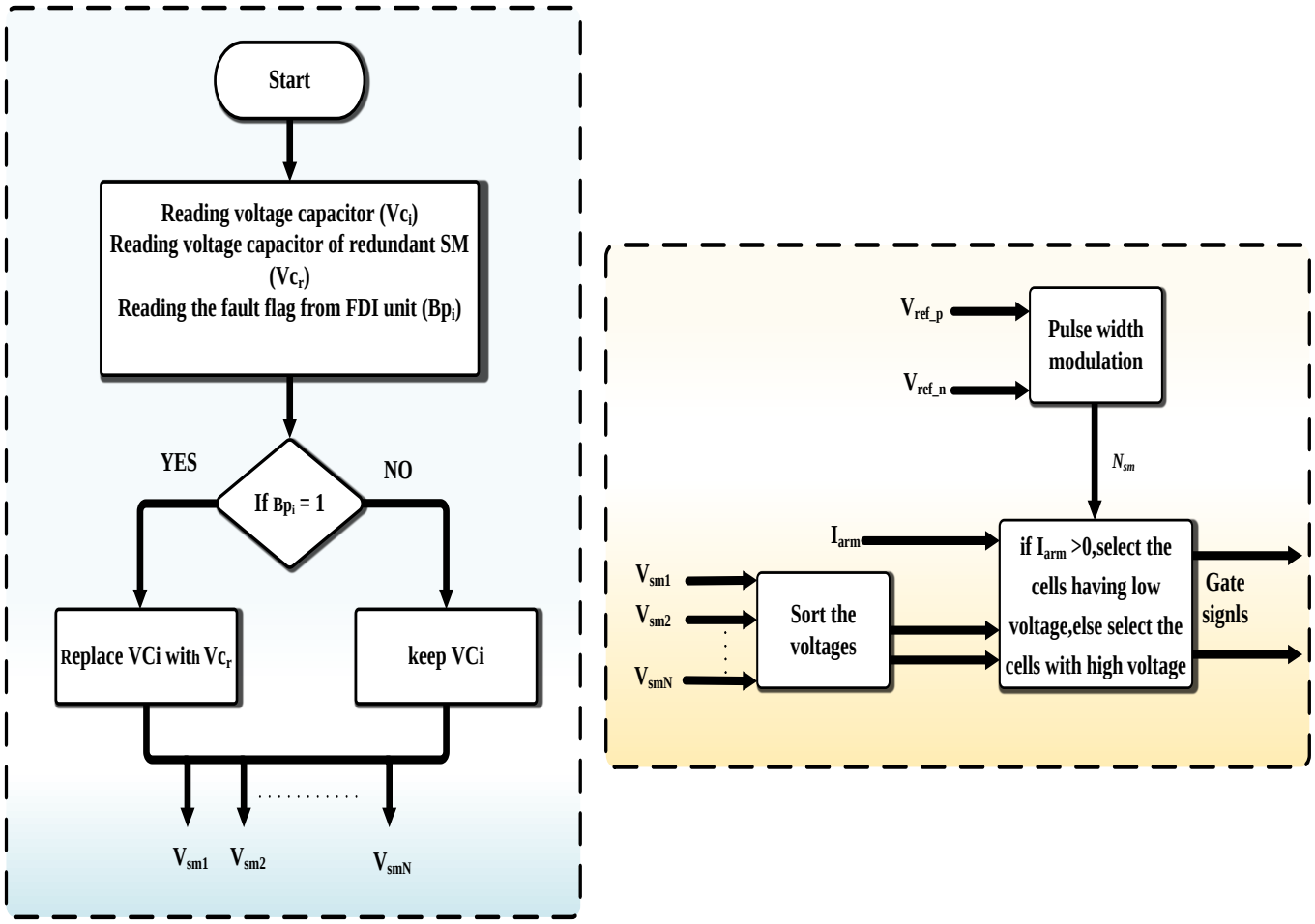


Figure.IV. 13 The flowchart of the modified sorting algorithm

The modified flowchart (Figure.IV..13) consists of two main stages. The fault-handling (blue part) reads the capacitor voltage of each active submodule (Vc_i), the voltage of the redundant submodule (Vc_r), and the fault flag (Bp_i) provided by the fault detection and identification (FDI) unit. If a fault is detected ($Bp_i = 1$), the faulty capacitor voltage Vc_i is replaced by the redundant voltage Vcr; otherwise, the original Vc_i is retained. The modified sorting algorithm (yellow part) then processes the updated capacitor voltages, sorts them, and based on the sign of the arm current (I_{arm}) selects either the lowest or highest voltage submodules for insertion.

Finally, a logic gate–based switching control strategy is proposed, which utilizes the fault flags generated from the Fault Detection and Unit Isolation (FDUI) module together with the gating signals provided by the modified control unit. Figure.IV. 14 illustrates the switching process,

where basic logic gates (NOT, AND, OR) are employed to determine the appropriate switching states.

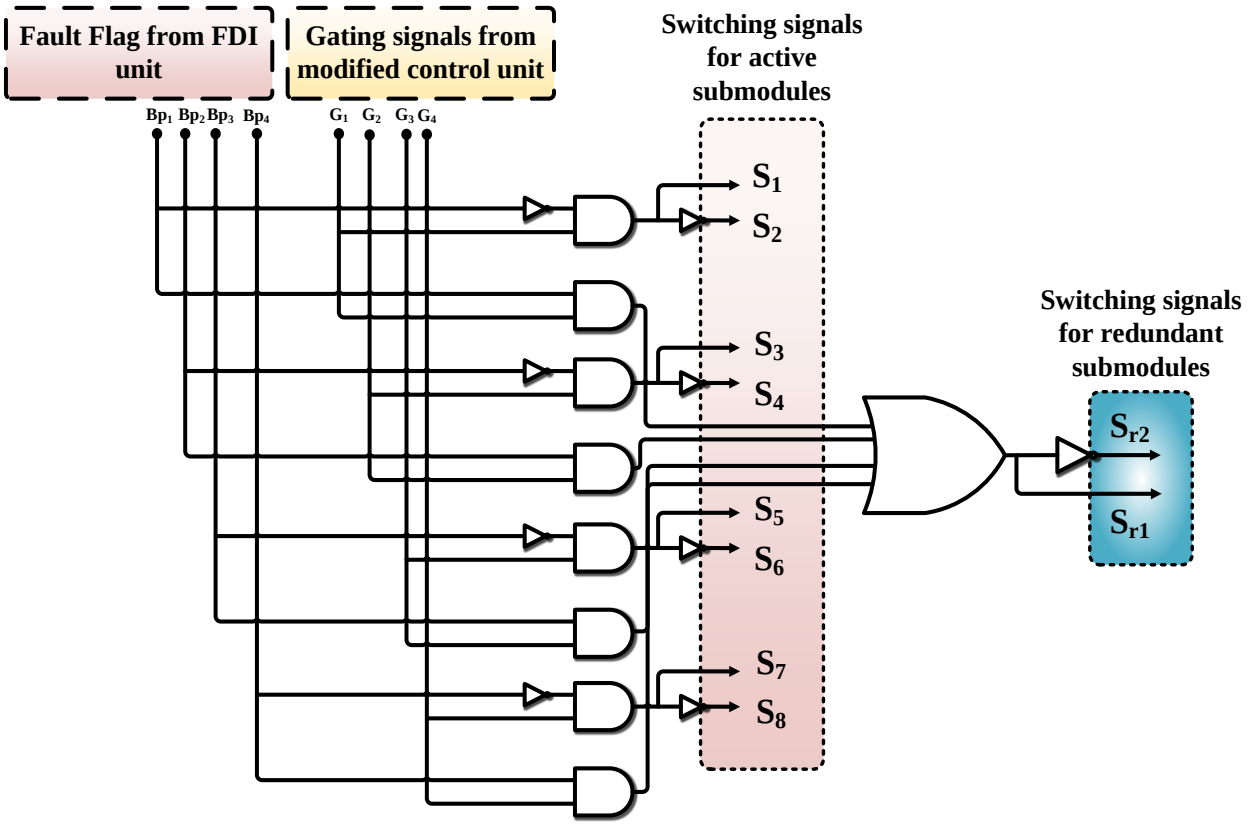


Figure.IV. 14. Logic circuit–based switching control strategy for active and redundant submodules

The mathematical representation of the switching signals for the active submodules is given as:

$$\text{Upper ARM switching signals} \begin{cases} S_1 = \overline{Bp_1}.G_1, S_2 = \overline{S_1} \\ S_3 = \overline{Bp_2}.G_2, S_4 = \overline{S_3} \\ S_5 = \overline{Bp_3}.G_3, S_6 = \overline{S_5} \\ S_7 = \overline{Bp_4}.G_4, S_8 = \overline{S_7} \end{cases} \quad \text{IV.6}$$

Lower ARM switching signals $\begin{cases} S_9 = \overline{Bp_5}.G_5, S_{10} = \overline{S_9} \\ S_{11} = \overline{Bp_6}.G_6, S_{12} = \overline{S_{11}} \\ S_{13} = \overline{Bp_7}.G_7, S_{14} = \overline{S_{13}} \\ S_{15} = \overline{Bp_8}.G_8, S_{16} = \overline{S_{15}} \end{cases}$ IV.7

Similarly, the switching signals for the redundant submodules can be expressed as:

Upper ARM redundant signals:

$$S_{ru_1} = \sum_{i=1}^{4} Bp_i.G_i, S_{ru_2} = \overline{S_{ru_1}} \quad \text{IV.8}$$

Lower ARM redundant signals:

$$S_{rl_1} = \sum_{i=5}^{8} Bp_i.G_i, S_{rl_2} = \overline{S_{rl_1}} \quad \text{IV.9}$$

Table.IV. 3 the modified switching states in bouth cases healthy and faulty

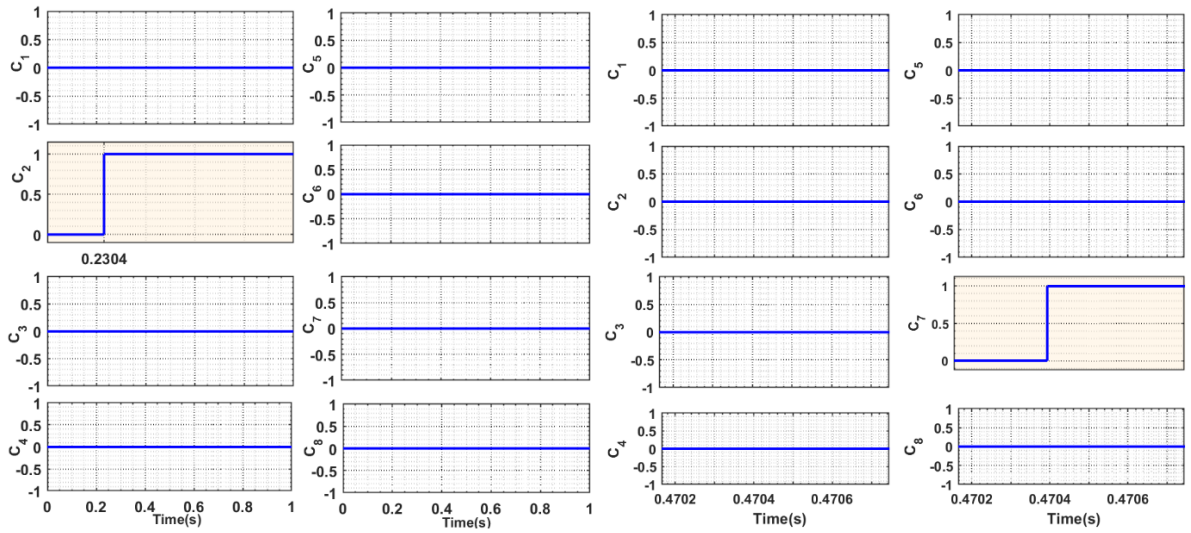
state	**Bp_i**	**S_i**	**S_r**
healthy	0	G_i	0
Faulty	1	0	G_i

Table.IV. 3 presents the modified switching states of the submodules under healthy and faulty conditions. The logic is based on the fault flag Bp_i, the original gating signal G_i , the actual switching signal S_i and the redundant switching signal S_r, In the healthy case, when no fault is detected (Bp_i =0), the submodule operates normally, and the switching signal follows the original gating signal ($S_i = G_i$) while the redundant signal remains inactive (S_r =0). Conversely, in the faulty condition (Bp_i =1), the original switching signal is blocked (S_i =0) and the redundant switching signal is activated to replace the faulty submodule ($S_r = G_i$).

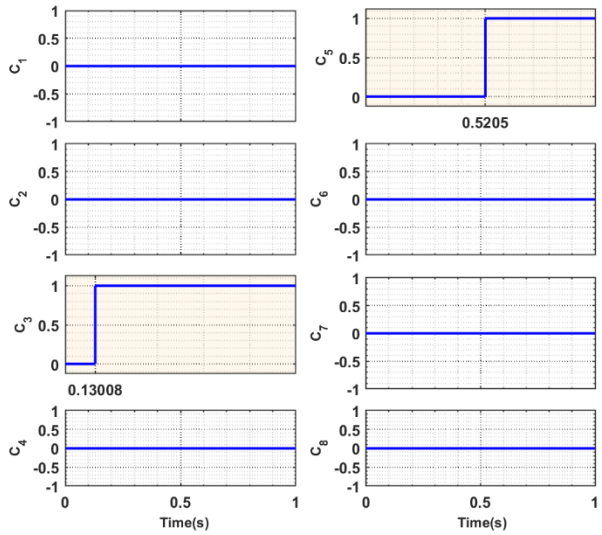
IV.5. Results and discussion

The proposed Fault-Tolerant Control (FTC) strategy was validated under different fault scenarios to evaluate its efficiency and robustness in handling various fault conditions. Three representative cases were considered. In **Scenario 1**, the capacitor of submodule 2 in the upper arm experienced an open-circuit fault at t=0.23s. In **Scenario 2**, the capacitor of submodule 7 in the lower arm was subjected to an open-circuit fault att=0.47s. Finally, in **Scenario 3**, multiple faults were introduced, where the capacitor of submodule 3 failed at t=0.13s, followed by a fault in the capacitor of submodule 5 at t=0.52s, affecting both the upper and lower arms. These scenarios were designed to demonstrate the capability of the proposed method to maintain reliable operation under single and multiple fault conditions.

IV.5.1. fault detection and identification



(a) (b)



c)

Figure.IV. 15 Fault detection and identification results: a) Scenario 1, b) Scenario 2, Scenario 3

Figure.IV. 15 illustrates the results of the proposed Fault Detection and Identification (FDI) method.

Figure.IV. 15(a): In Scenario 1, the method successfully detected the fault. As observed, all channels remained fixed at a value of 0, except for the channel corresponding to the capacitor of submodule 2. At t = 0.2304 s, this channel transitioned from 0 to 1, confirming the presence of a fault in submodule 2.

Figure.IV. 15(b): In Scenario 2, a similar behavior is observed. All channels remained stable at 0, except for the channel corresponding to the capacitor of submodule 7. At t = 0.4704 s, this channel transitioned from 0 to 1, clearly indicating a fault in submodule 7.

Figure.IV. 15(c): In Scenario 3, the channels corresponding to capacitors of submodules 3 and 5 exhibited transitions from 0 to 1 at t = 0.13008 s and t = 0.5205 s, respectively. This confirms the occurrence of multiple faults in submodules 3 and 5. Meanwhile, the remaining channels stayed stable. at 0, indicating that no false alarms were generated.

These results demonstrate that the proposed FDI method is highly accurate, free from false detections, and capable of identifying both single and multiple faults with fast response ranging

from 80 µs to 500 µs. Such reliability is crucial for ensuring the effectiveness of the overall Fault-Tolerant Control (FTC) strategy.

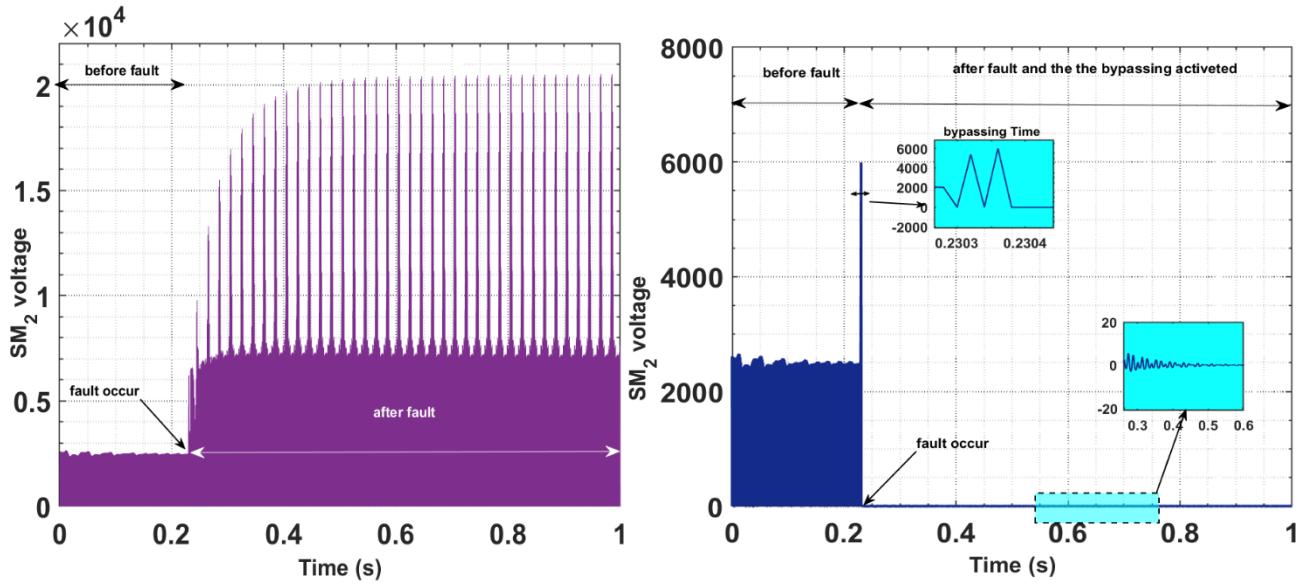
IV.5.2. Fault Isolation

Based on the results of the FDI method, the bypassing mechanism was applied as described in the previous section.

Figure.IV. 16(a): This Figure. represents the output voltage of submodule 2 without activating the bypassing mechanism. Under normal operation, the output voltage remained at its nominal value of 2500 V. However, when a fault occurred at t = 0.23 s, the voltage exhibited a sharp deviation, reaching 2.10^{4} V. Such an overvoltage is highly dangerous for the capacitor and can cause severe damage to the submodule.

Figure.IV. 16(b): This Figure.IV. shows the output voltage of submodule 2 when the bypassing mechanism was activated. After the fault occurred, the voltage rapidly decreased and stabilized approximately at 0 V within just 0.4 ms, confirming the prompt activation of the bypassing mechanism triggered by the FDI method (Figure.IV. 15(a)). This protective action successfully prevented the overvoltage condition that would otherwise threaten the system's reliability.

These results confirm that the bypassing mechanism, when coordinated with the proposed FDI method, effectively protects the system against fault-induced overvoltage. The same behavior was consistently observed across all tested scenarios.



a) b)

Figure.IV. 16 Fault isolation: a) without the bypassing mechanism, b) with the bypassing mechanism

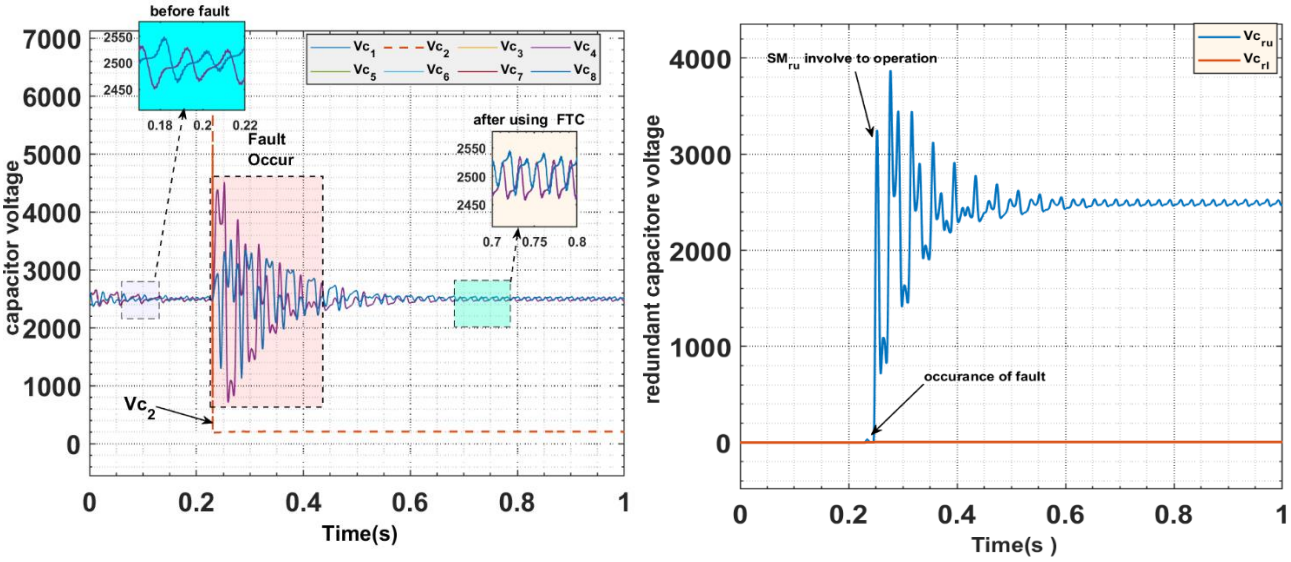
IV.5.3. system reconfiguration

Once the faulty submodule has been bypassed and the system is safeguarded against potential damage and the propagation of the fault, a reconfiguration process becomes essential. This reconfiguration is required not only to restore the converter to a safe operational state but also to maintain its power quality, voltage balancing, and overall system stability. Without such reconfiguration, the converter may experience degraded performance, increased stress on the remaining healthy submodules, and potential reliability issues. Therefore, reconfiguration plays a critical role in ensuring continuous operation, prolonging the system's lifetime, and achieving fault-tolerant performance in Modular Multilevel Converters

A) Scenario 1

In this section, the results of the reconfiguration method for Scenario 1 are presented. Figure.IV. 17(a) illustrates the capacitor voltages of the active submodules (SMs). As can be observed, prior to the fault occurrence, all capacitor voltages operate in a balanced manner around the nominal value of 2500 V. Once the fault occurs, the voltage of Vc_2 drops to approximately 0 V, which confirms the correct operation of the bypassing mechanism. On the other hand, the healthy capacitor voltages (Vc_1, Vc_3… Vc_8) exhibit noticeable oscillations. This behavior is

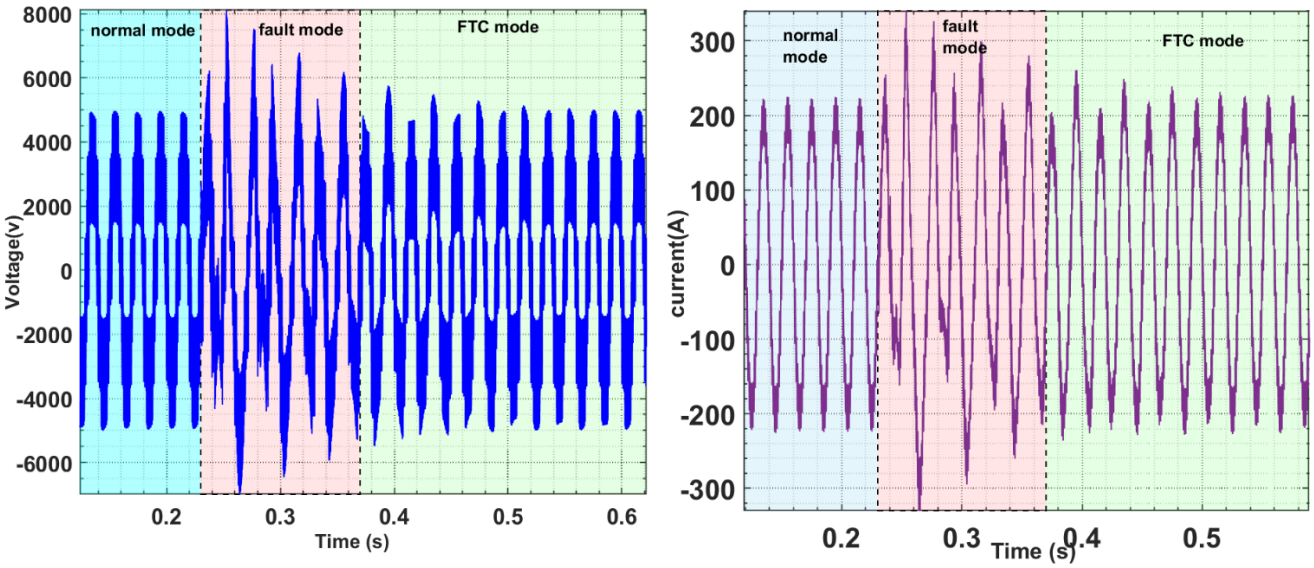
attributed to the insertion of the redundant submodule (SM_{ru}) and the charging process of its capacitor, as illustrated in Figure.IV. 17(b).



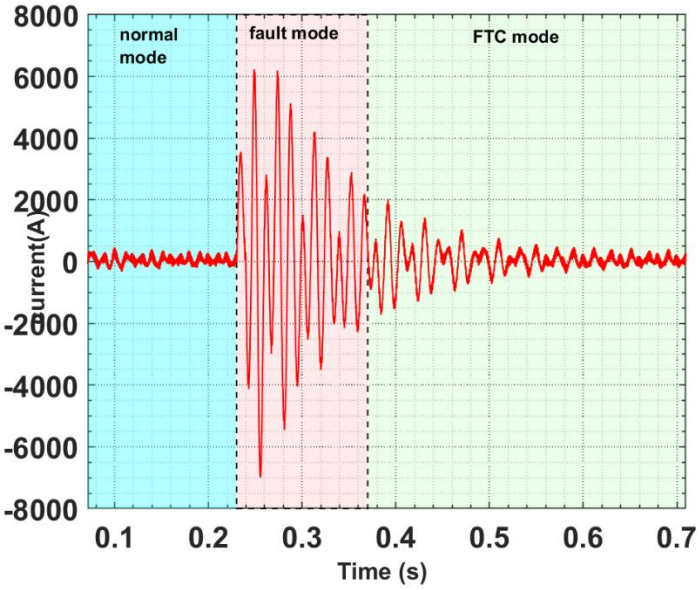
a) b)

Figure.IV. 17 capacitor voltage under fault c2: a) capacitor voltage of active SM, b) capacitor voltage of redundant SM

Figure.IV. 18 presents the performance of the MMC system under the proposed Fault-Tolerant Control (FTC) strategy. In Figure.IV. 18(a), the output voltage is shown. It can be observed that after the occurrence of the fault at t=0.23s, the voltage waveform exhibits a noticeable distortion. However, after approximately 0.14 s, the fault is cleared and the waveform is restored to its nominal shape, demonstrating a return to normal operation. Similarly, Figure.IV.s 18(b) and 18(c) illustrate the output current and the circulating current, respectively. In both cases, the fault is mitigated rapidly, confirming the effectiveness of the proposed strategy. These results highlight the capability of the method to achieve fast fault reconfiguration, ensuring system stability and preserving the overall performance of the MMC.



a) b)



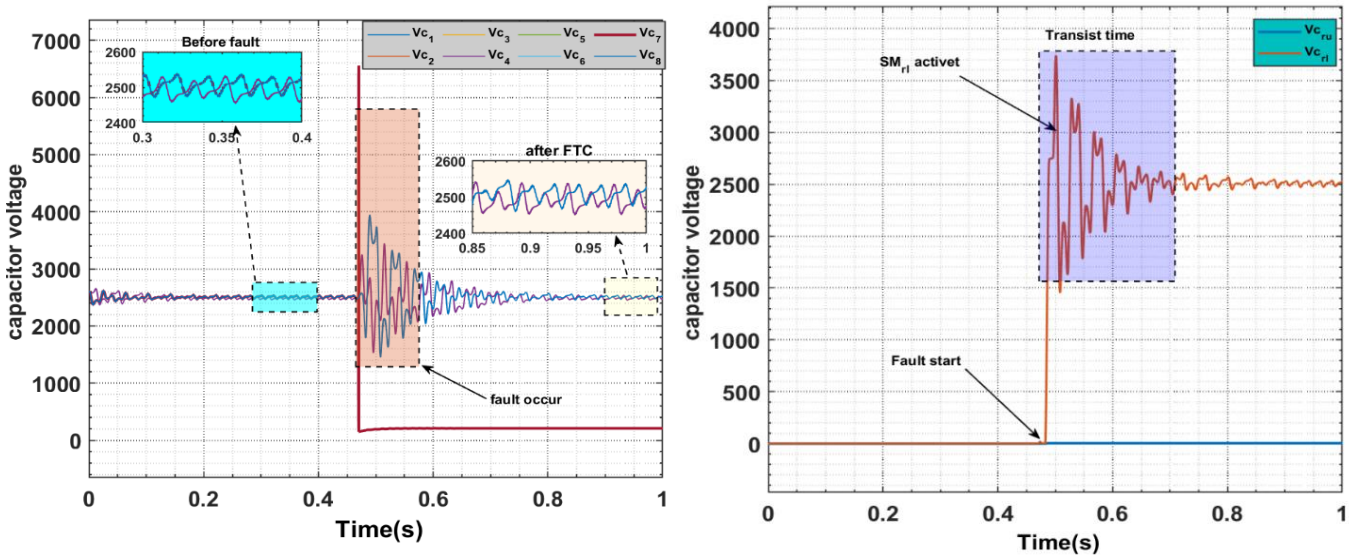
c)

Figure.IV. 18: AC output under c2 fault: a) output voltage, b) output current, c) circulation current

B) Scenario 2

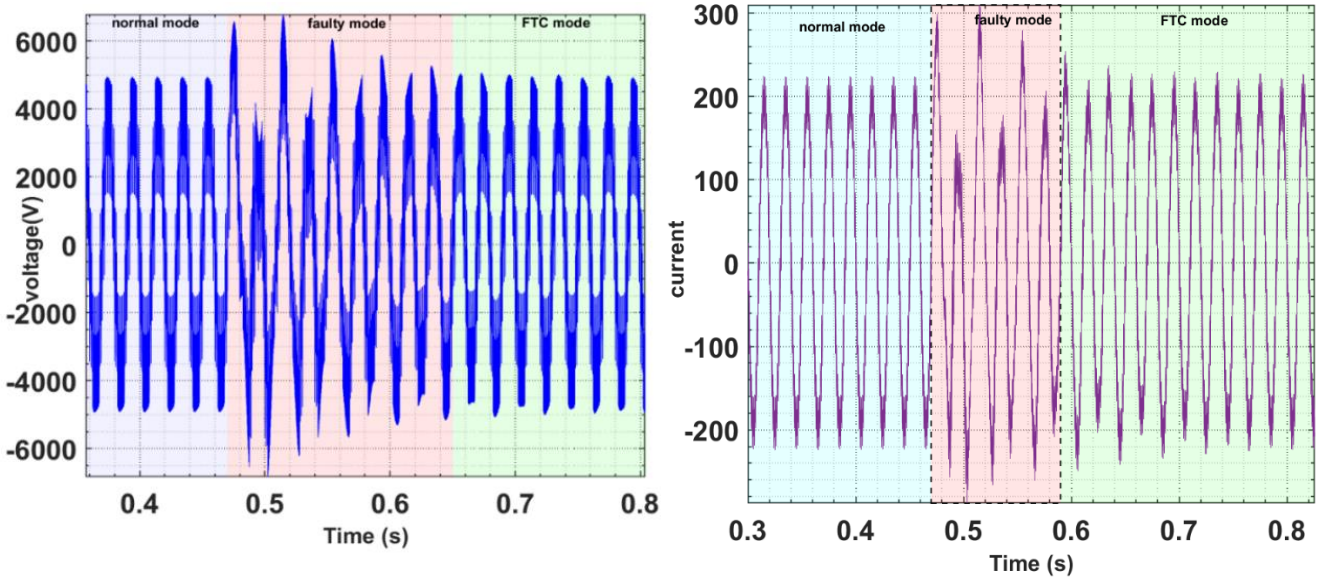
In this section, the proposed FTC strategy is evaluated under a different fault scenario, with the corresponding results shown in Figure.IV. 19 and 20. Figure.IV. 19(a) presents the capacitor voltages of the active submodules (SMs). Before the fault occurs, all capacitor voltages remain balanced around the nominal value of 2500 V similarly to the previous scenario. When the fault

takes place, the voltage of Vc_7 drops to nearly 0 V, confirming the disconnection of the faulty SM. Meanwhile, the voltages of the healthy SMs display oscillatory behavior, which is mainly due to the charging process of the redundant submodule capacitor (SM_{rl}), as illustrated in Figure.IV. 19(b).

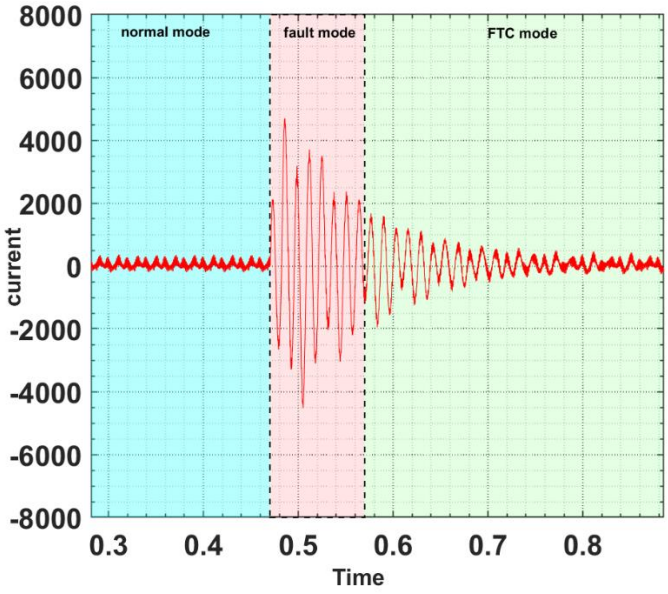


a) b)

Figure.IV. 19 capacitor voltage under fault c7: a) capacitor voltage of active SM, b) capacitor voltage of redundant SM



a) b)



c)

Figure.IV. 20 AC output under c7 fault: a) output voltage, b) output current, c) circulation current

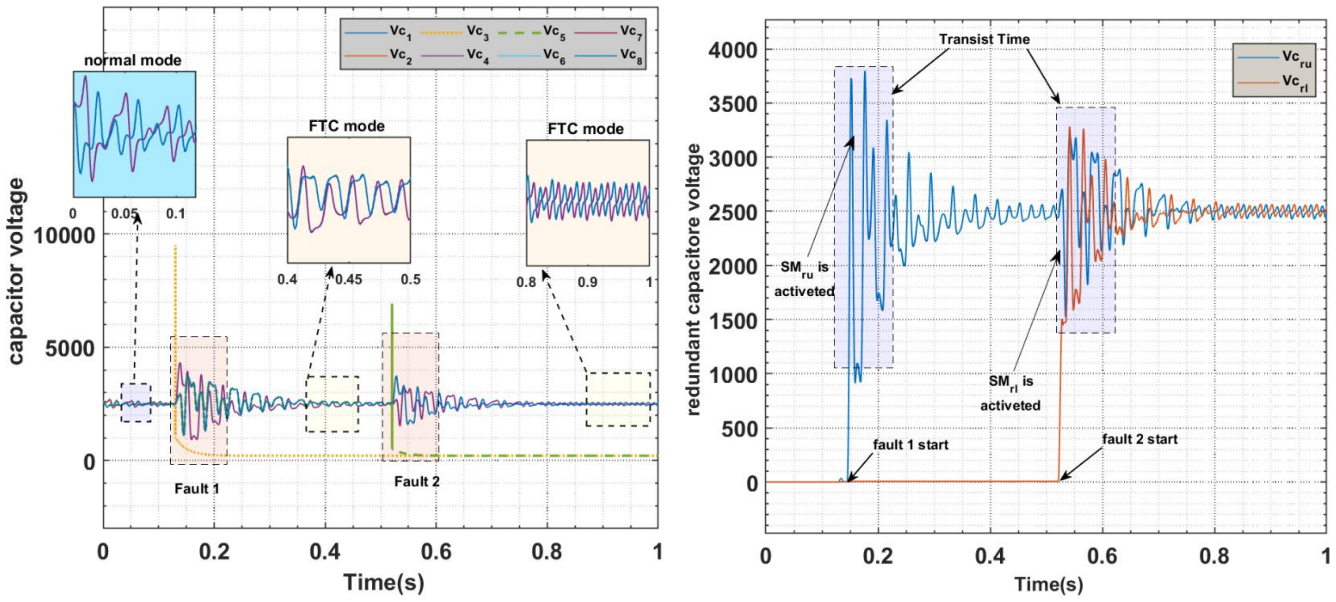
Similarly, to the previous case, the output voltage shown in Figure.IV. 20(a) exhibits a distortion at t=0.47s, corresponding to the instant of fault occurrence. Within a few milliseconds, the fault is cleared, and the voltage waveform recovers its nominal shape. Figure.IV.s 20(b) and 20(c) present the output current and the circulating current, respectively. In both cases, the disturbance is eliminated quickly, which demonstrates the capability of the proposed FTC strategy to mitigate faults effectively and restore normal operating conditions with a fast dynamic response. Overall, the results obtained from this scenario, together with those of Scenario 1, confirm the robustness and reliability of the proposed approach in maintaining stable. operation of the MMC under different fault conditions.

C) Scenario 3

In this section, the proposed FTC strategy is evaluated in the case of multiple faults, with the results shown in Figure.IV. 21. As illustrated in Figure.IV. 21(a), the capacitor voltages of the activated SMs indicate that Vc_3 and Vc_5 drop to approximately 0 V at t=0.19 sand t=0.52 s, respectively. This behavior confirms that the bypassing mechanism functions correctly under multi faults conditions. Furthermore, Figure.IV. 21(b) shows the involvement of the redundant submodules

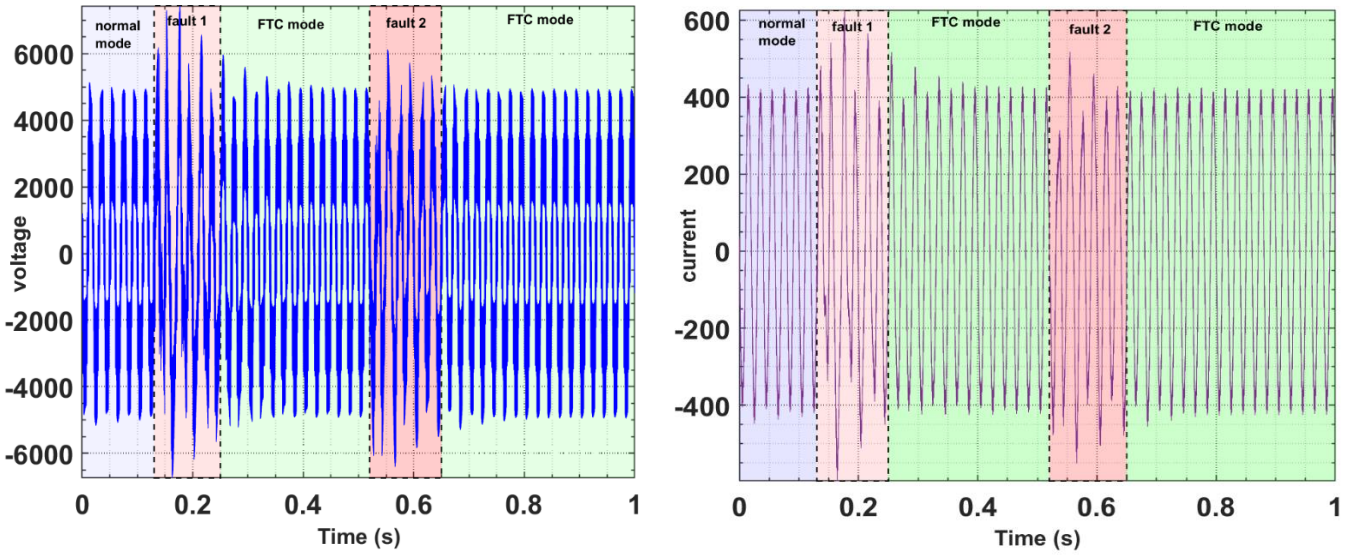
SM_{ru} and SM_{rl}, which validates their successful insertion into the upper and lower arms of the converter to compensate for the faulty SMs.

The overall performance of the MMC system under multi faults conditions is presented in Figure.IV. 22. As shown in Figure.IV. 22(a), the output voltage recovers its nominal value shortly after each fault occurrence, with a response time of approximately 0.13 s. A similar recovery is observed for the output current and the circulating current, as illustrated in Figure.IV.s 22(b) and 22(c). These results clearly demonstrate the effectiveness of the proposed FTC strategy in handling multiple simultaneous faults, ensuring fast reconfiguration, stable. Operation, and reliable fault-tolerant performance of the MMC.

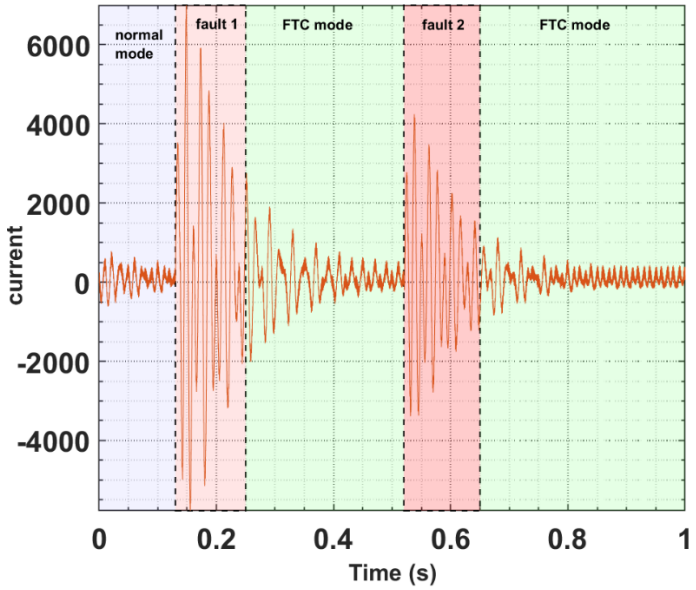


a) b)

Figure.IV. 21 capacitor voltage under fault in c3 & c5: a) capacitor voltage of active SM, b) capacitor voltage of redundant SM



a) b)

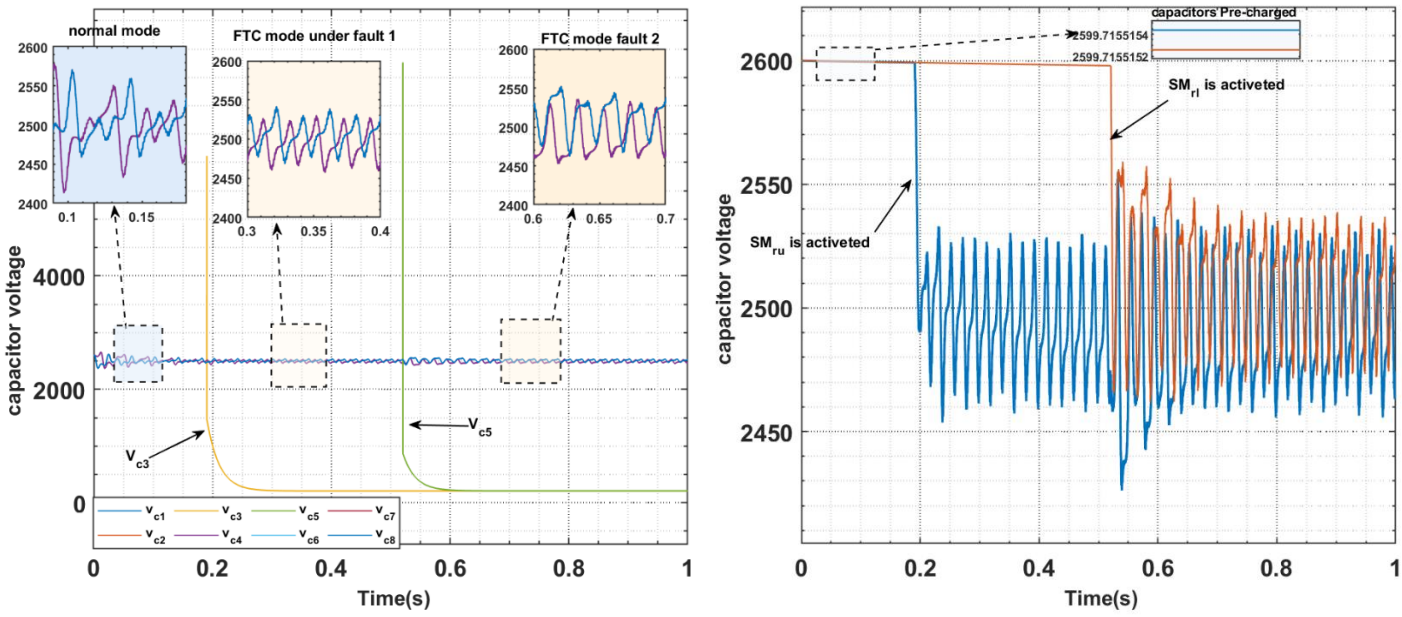


c)

Figure.IV. 22 AC output under fault in c3 & c5: a) output voltage, b) output current, c) circulation current

D) Evaluation of FTC Strategy Under Pre-Charged Redundant Capacitor Condition

For completeness, the performance of the proposed FTC strategy was also evaluated in the case where the redundant SM capacitor is initially charged. In this study, the capacitor was pre-charged manually in MATLAB/Simulink, without implementing a dedicated charging mechanism.

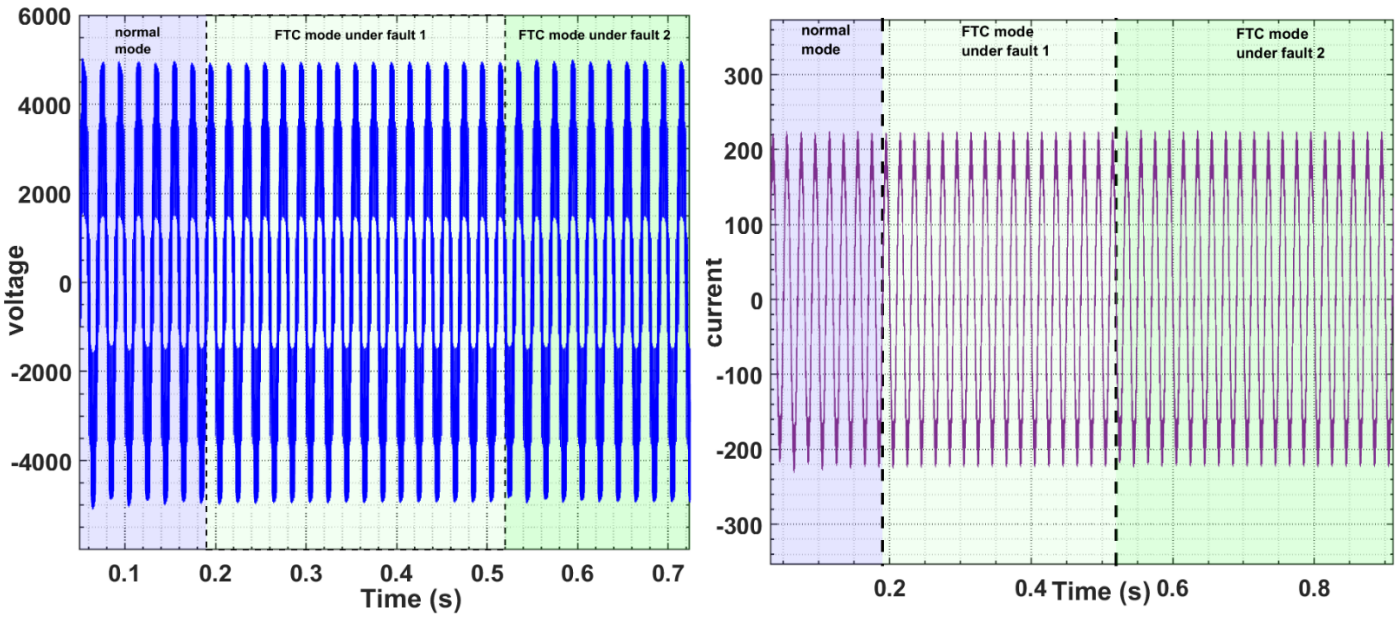


a) b)

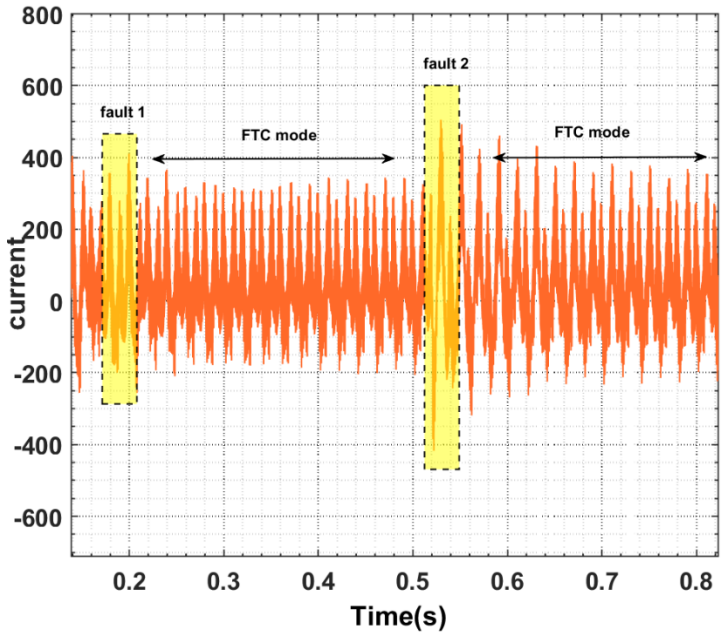
Figure.IV. 23 capacitor voltage under fault in c2: pre-charged capacitor: a) capacitor voltage of active SM, b) capacitor voltage of redundant SM

The multi-fault scenario was further tested under the condition where the redundant SM capacitor was pre-charged, as shown in Figure.IV. 23(a). In this case, Vc_3 and Vc_5 remain approximately at 0 V following the fault occurrence, confirming the proper operation of the bypassing mechanism. Compared to the uncharged case (Figure.IV. 21(a)), a clear improvement can be observed in the voltages of the healthy capacitors: the oscillations previously present are eliminated, and all capacitor voltages maintain smooth balancing, as illustrated in Figure.IV. 23(b).

Moreover, the overall performance of the MMC system benefits significantly from the pre-charging of the redundant capacitor. Figure.IV.s 24(a) ,24(b), and 24(c) present the output voltage, output current, and circulating current, respectively. In all cases, the waveforms recover rapidly and smoothly after the fault, confirming that capacitor pre-charging enhances the effectiveness of the proposed FTC strategy, leading to faster reconfiguration and improved system stability.



a) b)



c)

Figure.IV. 24 AC output under fault in c2 pre-charged capacitor: a) output voltage, b) output current, c) circulation current

Table.IV. 4 THD Analysis of Output Voltage and Current Under Different Fault Scenarios

Case	Output voltage THD	Output current THD
Healthy	17.74 %	11.28%
Single fault without FTC	26.53%	18.68%
Multi-faults without FTC	35.14%	29.51%
Single fault with FTC	20.13%	14.41%
Multi-faults with FTC	23.38%	18.23%
Single fault with FTC+ Pre-charge	17.74%	11.29%
Multi-faults with FTC+ Pre-charge	17.75%	11.30%

Table.IV. 4 summarizes the Total Harmonic Distortion (THD) values of the output voltage and current under different operating conditions. In the healthy case, the voltage and current THD are 17.74% and 11.28%, respectively. When a single fault occurs without applying any FTC strategy, the THD increases significantly to 26.53% for the voltage and 18.68% for the current. The degradation is even more pronounced under multi-fault conditions without FTC, where the THD rises to 35.14% and 29.51%, highlighting the severe impact of faults on power quality.

When the proposed FTC strategy is applied, a noticeable improvement is achieved. For a single fault, the voltage and current THD are reduced to 20.13% and 14.41%, respectively. Similarly, in the case of multi-faults, the THD values drop to 23.38% and 18.23%, confirming the effectiveness of the proposed method in mitigating fault effects and enhancing system performance.

The most significant improvement is observed when the FTC strategy is combined with pre-charged redundant capacitors. In this case, the THD values are nearly identical to those of the healthy condition. For a single fault, the voltage and current THD are 17.74% and 11.29%, while for multifaults, they are 17.75% and 11.30%. These results demonstrate that capacitor pre-charging allows the FTC to fully restore system performance, achieving harmonic levels comparable to fault-free operation

Table.IV. 5. Comparison between different fault tolerant strategies

Ref	Method	Type of fault	Recon time	i_{Cir} peaks	Complexity
[146]	Mixed hot & cold	diode	Fast (≈10 ms)	Medium	High
[147]	Cold	SM	Slow (≈1s)	Low	Medium
[145]	Cold	SM	Slow (≈1.2 s)	Medium	Medium
[141]	Hot	SM	Fast (≈20 ms)	Low	High
Proposed FTC	Cold	Capacitor	Medium (90 ms)	Medium	Medium

Table.IV. 5 compares different fault-tolerant control (FTC) strategies in terms of reconfiguration speed, current stress, and implementation complexity. Methods [146] and [141] achieve very fast reconfiguration (10–20 ms) by keeping redundant submodules active. However, this results in high complexity. In [146], complexity arises from a multi-stage control scheme coordinating hot and cold reserves, while [141] requires a modified sorting algorithm capable of continuously managing all submodules and instantly excluding the faulty one, leading to significant real-time computation. In contrast, methods [147] and [145] adopt a pure cold-reserve approach, which simplifies normal operation. Their complexity is considered medium, as they require a dedicated transition control algorithm to handle slow capacitor charging and ensure stability during a longer reconfiguration time (1–1.2 s), but they avoid complex control during steady-state operation.

The proposed FTC method provides a compromise, with a moderate reconfiguration time (≈90 ms) and medium complexity. It combines an artificial neural network with a simple logical circuit to manage gating signals, avoiding sophisticated control schemes and eliminating the need to keep redundant submodules active. Although it uses a cold redundant submodule—introducing a brief charging interval—it maintains simple normal-mode operation and avoids extra power losses. The method is currently focused on capacitor faults, enabling high detection accuracy and fast response, while remaining adaptable to other fault types in future work

IV.6. Conclusion

This chapter presented a fault-tolerant control (FTC) framework for Modular Multilevel Converters (MMCs) subject to capacitor failures. The proposed strategy demonstrated effective fault detection, isolation, and reconfiguration in both single and multiple fault scenarios, ensuring stable operation and reducing harmonic distortion. Simulation results confirmed that capacitor pre-

charging further improves performance by eliminating oscillations in healthy capacitors and restoring THD levels close to healthy conditions.

For future work, attention will be given to developing a simple and practical method for pre-charging redundant submodule capacitors, in order to fully exploit the benefits observed in simulation and enhance the applicability of the proposed FTC strategy in real MMC systems.

General Conclusion

This thesis addressed the problem of fault diagnosis and tolerance in MMCs. The main objective was to develop diagnostic and control strategies that can accurately detect, isolate, and mitigate different categories of faults in MMC submodules, thereby enhancing reliability. A range of signal-processing, intelligent, and hybrid methods were proposed and validated through simulations on a five-level MMC benchmark.

Summary of Contributions

- ✓ The first contribution is the development of intelligent diagnostic methods, based on fuzzy logic and artificial intelligence, for open-circuit faults in both IGBTs and their anti-parallel diodes. Unlike most previous works that considered only the IGBT, this study included diode faults, providing a more complete diagnosis framework. By combining time–frequency feature extraction with machine learning models, accurate detection and localization were achieved.
- ✓ The second contribution is a hybrid diagnostic approach for detecting and localizing multiple short-circuit faults within a single submodule. Traditional strategies often assume only one fault per submodule, a clear limitation. The proposed method combined discrete wavelet transform with radial basis function, improving accuracy and robustness against simultaneous failures.
- ✓ The third contribution is a fast signal-processing-based technique for IGBT short-circuit detection. Since short circuits escalate quickly to catastrophic failures, rapid detection is vital. The proposed method reduced detection latency while preserving precision, ensuring protective actions can be taken within safe time margins.
- ✓ The fourth contribution is a simple fault-tolerant control (FTC) strategy to manage capacitor failures. Using intelligent decision-making with logical gates, the FTC is easy to implement while providing effective fault ride-through capability. This allows the converter to remain in operation in a degraded but stable mode, avoiding unnecessary shutdowns.

Limitations

Despite these advances, several limitations remain. First, all validation was performed in MATLAB/Simulink; experimental validation on a real setup is still needed to confirm robustness under non-ideal conditions. Second, the intelligent methods rely on training datasets, making performance sensitive to data representativeness. Broader datasets would improve generalization. Third, the proposed FTC strategy is limited to capacitor faults, while more advanced schemes covering a wider range of device faults should be investigated.

Future Work

Based on these limitations, future work should focus on:

- Implementing the methods on a scaled-down or real MMC prototype.
- Combining model-based observers with AI-based methods to exploit their complementary strengths.
- Developing FTC schemes capable of handling both semiconductor and capacitor faults.
- Designing practical methods for precharging redundant submodule capacitors to enhance redundancy strategies.

In conclusion, this thesis has made significant contributions to improving MMC reliability through advanced diagnostic and control methods. The proposed approaches enhance both fault detection accuracy and fault tolerance. While bridging the gap between simulation and real-world deployment remains essential, the results provide a solid foundation for more intelligent, reliable, and resilient multilevel power conversion systems.

Appendix

Table 1 : simulation parameters

Parameter	Value
Number of SMs per arm	**4**
DC voltage (V)	$\mathbf{10\times10^{3}}$
SM capacitance (F)	$\mathbf{7.368\times10^{-3}}$
Arm inductance (H)	$\mathbf{9.549\times10^{-4}}$
Arm resistance (Ω)	**0**
Load resistance (Ω)	**10**
Load inductance (H)	$\mathbf{3.8\times10^{-3}}$
Load frequency (Hz)	**60**
K_δ	**3**
γ_1	**5**
γ_2	**3**

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