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Investigation on Active Power Filter based on Z-Source Inverter Topology

Supported, on 29 /05/ 2021, before the jury composed of:

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Nomenclature

List of abbreviations

ANFIS Adaptive network based fuzzy inference system

APFs Active power filters

CSC Current source converter

CSI Current source inverter

EMI Electromagnetic interference

FFT Fast Fourier transform

GTO Gate turn-off thyristor

HIL Hardware in the loop

HVDC High voltage direct current

IGBT Insulated-Gate Bipolar Transistor

InC Incremental conductance

IRPT Instantaneous reactive power theory

MBC Maximum boost control

MCBC Maximum constant boost control

MCBCT Maximum constant boost control with third harmonic injection

MPPT Maximum power point tracking

OCV Open circuit voltage

P&O Perturbation and observation

PCC Point of common coupling

PLL Phase Locked Loop

PV Photovoltaic

PWM Pulse with modulation

QZSI Quasi Z-source inverter

RMS Root mean square

SAPF shunt active power filters

SBC Simple boost control

SCC Short-circuit current

SCR Silicon controlled rectifier

SDM Synchronous detection method

SRF synchronous reference frame

STC standard test condition

THD Total harmonic distortion

UPQC Unified power quality conditioner

UPS Uninterruptible power supplies

VSC Voltage source converter

VSI Voltage source inverter

VUF Voltage unbalance factor

ZSI Z-source inverter

List of symbols

C_{dc} DC-link capacitor

d DC-DC boost duty ratio

D_0 shoot through duty ratio

f_s Switching frequency

I_{pv} PV current

$ic_{\alpha,\beta}$ Reference currents in $\alpha - \beta$ frame

ic_{abc} Reference currents

$if_{\alpha,\beta}$ Injected currents in $\alpha - \beta$ frame

if_{abc} Filter currents

$il_{\alpha,\beta}$ Load currents in $\alpha - \beta$ frame

il_{abc} Load currents

il_{dq} Load currents in $d - q$ frame

is_{abc} Source currents

P_{pv} PV power

R_L, L_L Load resistance and inductance

Rf_{abc}, Lf_{abc} Coupling filter resistance and inductance

Rs_{abc}, Ls_{abc} Source resistance and inductance

S_a, S_b, S_c Control signals

T_s Sampling time

V_{Cref} reference QZSI capacitor voltage

V_C QZSI capacitor voltage

v_{dcref} reference DC-link voltage

v_{dc} DC-link voltage

V_{in} Input voltage

V_{pv} PV voltage

$vf_{\alpha,\beta}$ filter voltages in $\alpha - \beta$ frame

vf_{abc} Filter voltages

$vs_{\alpha,\beta}$ Source voltages in $\alpha - \beta$ frame

vs_{abc} Source voltages

General introduction

As a result of the industrial development, the usage of nonlinear loads has increased significantly. This raised many concerns such as voltage and current harmonics in the industrial and domestic systems. Indeed, the intensive appearance of these harmonics is mainly caused by diode rectifiers, heating regulators, adjustable frequency drives, which consume non-sinusoidal currents. [1–4]. The resulting harmonics can cause very serious problems such as equipment overheating [5], devices malfunctions, mechanical vibrations, and interference with remote control systems used by energy distributors and transmission systems [6]. Which leads to an economic impact, degradation of energy efficiency, and components over-sizing [7].

Conventionally, to eliminate such problems, passive filters were used because of their low cost and easy implementation. However, they have several limitations such as their large size, inflexibility [8], in addition to the fact that they are highly vulnerable to resonance problem [5]. Therefore, due to the continuous evolution of power electronics and control strategies, active power filters have been widely investigated because of their effective harmonic mitigation and power factor improvement. Furthermore, APFs can be classified into series, shunt and hybrid topologies [2], [5].

Shunt active power filters (SAPFs) are broadly used because of their simple implementation and efficient operation, especially for current harmonics elimination [9]. Generally, they are based on a voltage source inverter (VSI) which interfaces a capacitor connected to the DC-link. The voltage across the DC-link capacitor needs to be regulated. Therefore, the power losses caused by the switching devices are absorbed from the main grid [10, 11].

Several researches have been proposed to improve SAPFs configuration by integrating renewable energy sources. These alternative sources have several advantages, such as they are non-polluting, limitless and environmentally sustainable. By connecting a renewable source in the DC side of the shunt power filter, the power loss of switching devices is covered and the remaining power is injected into the grid. However, in shunt active power filters connected to a PV source through a two-stage PV system, an extra DC–DC converter is

highly needed to interface PV sources. The extra DC–DC converter eventually complicates the system, increases its cost and decreases its efficiency [12, 13].

Therefore, the new solution so-called Z-source inverter (ZSI) have been proposed to overcome the shortcomings of the conventional two-stage PV systems. This new topology is able to perform the tasks of the conventional configuration using one single topology due to unique extra shoot-through zero state which provides the boosting feature that can be used to track the maximum power [13].

As part of this research issue, this thesis was conducted in order to improve the shunt active power filter configuration by interfacing a photovoltaic source through z-source inverter topologies. To achieve these research objectives, this dissertation is divided into five chapters:

The first chapter presents a description of various power quality problems, including current and voltage disturbances. Then the origin of current harmonics produced by so-called non linear load, their consequences, and their standards.

In the second chapter, we provide a detailed description and modelling of shunt active power topology. Then, two harmonics estimation techniques: instantaneous reactive power (PQ theory) and synchronous reference frame (SRF method) are evaluated under severe grid conditions. In addition, three current controllers: hysteresis, PWM, and backstepping controller are used and evaluated under transient and dynamic load conditions. Finally, we present the simulations of the mentioned scenarios.

In the third chapter, we present the PV systems based on two stage of configuration based on DC-DC boost converter and a single stage configuration based on Z-source inverter and Quasi Z-source inverter, including the mathematical modelling of each configuration. followed by Incremental MPP tracker and various shoot through control approaches.

The fourth chapter is more particularly dedicated to the shunt active power filter connected to a PV system through both two stage and single stage configurations. Both systems are tested and evaluated under dynamic load conditions, unsteady irradiance, and short-circuit fault. The simulation and hardware in the loop results are illustrated.

Chapter I

State of the art: Power quality problems and harmonic mitigation techniques.

I.1 Introduction

The increasing appearance of power quality problems and disturbances is mainly caused by the use of the devices based on power electronics converters in industrial and domestic equipment. These converters offer many advantages such as their flexibility, reliability, and high efficiency. However, they behave as a nonlinear loads and generate harmonic current which keep spreading in the entire power system at different levels [7].

This chapter deals firstly with different power quality problems which can influence the voltage, the current, or the frequency such as voltage sags, harmonics, and frequency deviation, then we present the main source of harmonics, their effects, and the standards related to their treatment . The second part presents the techniques of harmonic mitigation including the conventional techniques based on passive power filters and modern techniques based on active power filters.

I.2 Power Quality problems

I.2.1 Voltage sags

Voltage sag is an alternative name for the phenomenon of voltage dip illustrated in figure I.1. Voltage sag is defined as a brief reductions in root mean square (RMS) voltage magnitude between 0.1 pu and 0.9 pu for a duration of 0.5 to 30 cycles as mentioned in The IEEE Std 1159-2019 "IEEE Recommended Practice for Monitoring Electric Power Quality" [14].

The magnitude and the duration are the two most important sag characteristics. Voltage

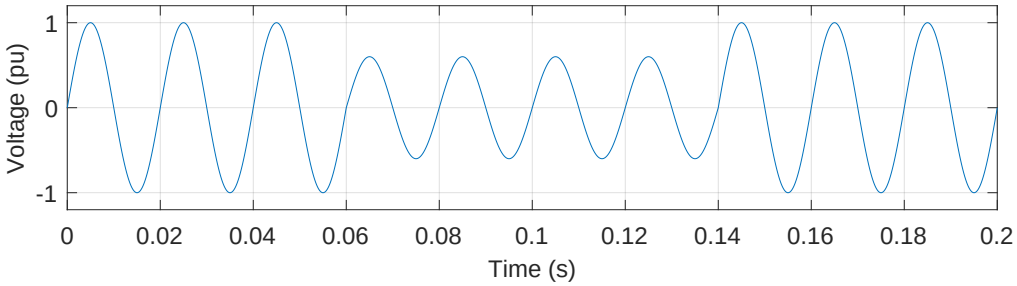


Figure I.1: Voltage sags

sags are typically caused by two main reasons:

- Starting devices that require a high current at startup like motors or transformer energizing
- Accidental short circuits on distribution networks, or local customer networks (insulation faults, cable damage... etc).

Indeed, this type of disturbance can cause operating degradation of electrical equipment which can lead to the total destruction of this equipment [15–18]. Moreover, voltage sags can be classified into instantaneous, momentary, and temporary as listed in Table (I.1).

Type of Sag	**Duration**	**Magnitude**
Instantaneous	0.5-30 cycles	0.10-0.90 pu
Momentary	30 cycles-3s	0.10-0.90 pu
Temporary	3s-1min	0.10-0.90 pu

Table I.1: Classification of voltage sags [14].

I.2.2 Voltage Swells

Voltage swell is phenomenon refers to a short duration (0.5 to 30 cycles) increase in the voltage beyond its tolerance levels (1.1 to 1.8 pu) as shown in Figure (I.2). Voltage swells can occur due to the start of heavy loads or energizing a large capacitor bank. Voltage swells can damage lighting systems, motors and shutdown equipment [15] [19, 20]. As with sags, swells are also associated with system fault conditions, but they are not as

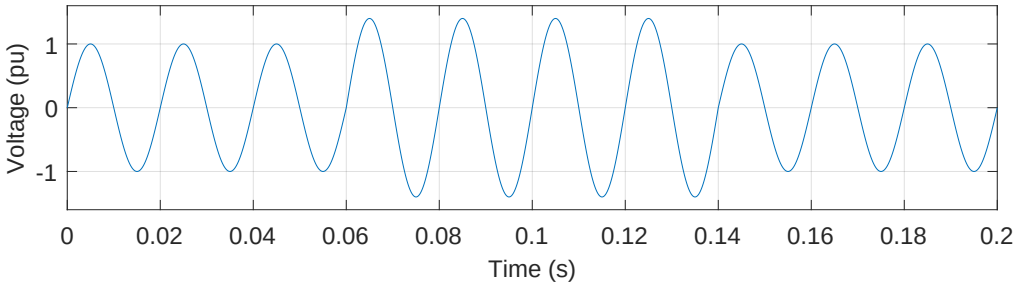


Figure I.2: Voltage swells

common as voltage sags [21]. Voltage swells can be classified according to their duration and magnitude as listed in Table (I.2).

Type of Swell	**Duration**	**Magnitude**
Instantaneous	0.5-30 cycles	0.10-1.80 pu
Momentary	30 cycles-3s	0.11-1.40 pu
Temporary	3s-1min	0.10-1.20 pu

Table I.2: Classification of voltage swells [14].

I.2.3 Harmonics

In the early 19th century, Jean Baptiste Fourier has proved that a periodic non-sinusoidal function of a fundamental frequency can be expressed as the sum of sinusoidal functions of frequencies which are integer multiples of the fundamental frequency [22].
A periodic function $f(t)$ of a period of T and defined in the interval $0 < t < T$ can be decomposed as:

$$\begin{aligned} f(t) &= \tfrac{a_0}{2} + a_1\cos(\omega t) + b_1\sin(\omega t) + \dots \\ &+ a_2\cos(2\omega t) + b_2\sin(2\omega t) + \dots \\ &+ a_n\cos(n\omega t) + b_n\sin(n\omega t) + \dots \end{aligned} \tag{I.1}$$

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n\cos(n\omega t) + \sum_{n=1}^{\infty} b_n\sin(n\omega t) \tag{I.2}$$

It can be also written as follows:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} c_n\sin\left(n\omega t + \phi_n\right) \tag{I.3}$$

Or:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} c_n \sin\left(\frac{2n\pi t}{T} + \phi_n\right) \tag{I.4}$$

Where:

$$a_0 = \frac{\omega}{\pi}\int_0^{2\pi/\omega} f(t)\mathrm{d}t \quad = \frac{2}{T}\int_0^{T} f(t)\mathrm{d}t \tag{I.5}$$

$$a_n = \frac{\omega}{\pi}\int_0^{2\pi/\omega} f(t)\cos(n\omega t)\mathrm{d}t = \frac{2}{T}\int_0^{T} f(t)\cos\left(\frac{2n\pi t}{T}\right)\mathrm{d}t \tag{I.6}$$

$$b_n = \frac{\omega}{\pi}\int_0^{2\pi/\omega} f(t)\sin(n\omega t)\mathrm{d}t = \frac{2}{T}\int_0^{T} f(t)\sin\left(\frac{2n\pi t}{T}\right)\mathrm{d}t \tag{I.7}$$

$$c_n = \sqrt{a_n^2 + b_n^2} \tag{I.8}$$

$$\phi_n = \mathrm{arctg}\,(a_n + jb_n) \tag{I.9}$$

$a_0/2$ is the dc component of the function,

a_n, b_n are the Fourier series coefficients,

n is an integer number from 1 to infinity,

c_n is the magnitude of the original function based on a_n and b_n,

ϕ_n is the initial phase of the original function.

According to [23], the word "Harmonic" refers to a sinusoidal component of a periodic wave with a frequency that is an integer multiple of the fundamental frequency. The fundamental frequency in the power systems could be either 50 Hz or 60 Hz. Therefore Harmonic components in 50 Hz systems are multiples of 50Hz (100Hz, 150Hz, 200Hz,... etc.). Voltage/current periodic waves which can be decomposed into a pure sinusoidal waves containing the fundamental component which has the fundamental frequency and harmonics with multiple frequencies. [23,24]. A sinusoidal voltage or current function that is dependent on time t is illustrated in Figure (I.3) and can be represented by equation (I.10) and equation (I.11) respectively.

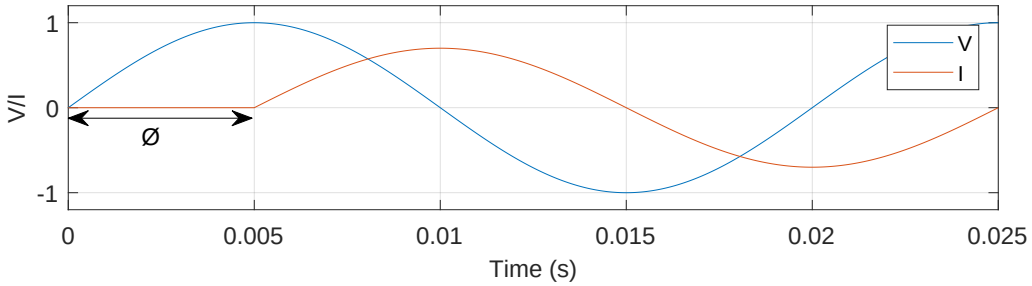


Figure I.3: Sinusoidal voltage and current wave-forms

$$v(t) = V\sin(\omega t) \tag{I.10}$$

$$i(t) = I\sin(\omega t - \phi) \tag{I.11}$$

The waveform illustrated in Figure (I.4) can be decomposed using Fourier representation [22] as follows:

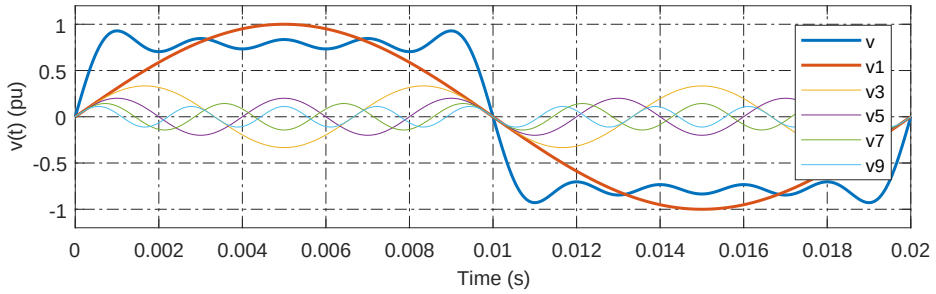


Figure I.4: Non-sinusoidal Waveform

$$\begin{aligned} v(t) = {} & V_1\sin(\omega t) + V_3\sin(3\omega t + \alpha_3) + V_5\sin(5\omega t + \alpha_5) + \\ & V_7\sin(7\omega t + \alpha_7) + V_9\sin(9\omega t + \alpha_3) \end{aligned} \tag{I.12}$$

Where, V_1 is the magnitude of the fundamental component and V_3, V_5, V_7, V_9 are magnitudes of harmonic components, and $\alpha_3, \alpha_5, \alpha_7, \alpha_9$ are shift phase angles.

I.2.3.1 Harmonic Sources

The development of technology over decades, especially the growth of the use of switched power semiconductor devices has resulted in rapid proliferation of harmonics within the power systems, such that the harmonics introduced by rotating machinery are nowadays considered negligible compared to those introduced by power electronic devices [25].

In modern power distribution networks single-phase and three-phase electronic power converters are perhaps the most important sources of harmonic distortion. Such as adjustable

speed drives, electronic power supplies, dc motor drives, battery chargers, electronic ballasts and many other types of rectifier /inverter applications [26].

Conventional nonlinear loads

This type of sources is not related to power electronics such as transformers, which causes a slight current peak due to the magnetization phenomena. The transformer current is rich in harmonics, especially the third harmonic component. On the same hand, machines also operates with peak flux densities. A three-phase synchronous generator generates a 30% third harmonic current. This harmonic components can be eliminated by using a delta transformer. Fluorescent lamps with magnetic ballasts extinguish and ignite each half-cycle. However, the caused flicker is difficult to be observed at frequencies of 50 or 60 Hz. Their current is slightly skewed, peaked, and have a second peak characteristic with third harmonic domination with up to 20% of fundamental. Arc Furnaces are difficult to be treated by Fourier series and harmonics since they are not strictly periodic. They are considered as transient loads for which flicker is a greater problem than harmonics [27].

Power Electronic Loads

a- Line Commutated Converters: Also known as six-pulse converters because they produce six ripple peaks On Vdc per cycle. The power flows often to the DC load. In order to control power flow, each silicon controlled rectifier (SCR) is fired after its natural forward-bias turn-on point, which leads to a poor displacement power factor at medium and low power levels. Line commutated converters have the advantage of simplicity and their SCRs are turned off by the load instead of forced-commutated circuits. Moreover, line commutated converters have the advantage of simplicity [27]. The circuit of line commutated converter is shown in Figure (I.5).

b- Voltage-Source Converters: The term "voltage source" comes from the stiff V_{dc} source for for the pulse with modulation (PWM) drive provided by the diode bridge and the capacitor. The displacement power factor in these converters is nearly 1 because they don't use phase control. However, the power system side in these converters suffer from higher current distortions compared to line commutated converters. Even though lower load levels have higher current distortions, the harmonic components do not vary greatly

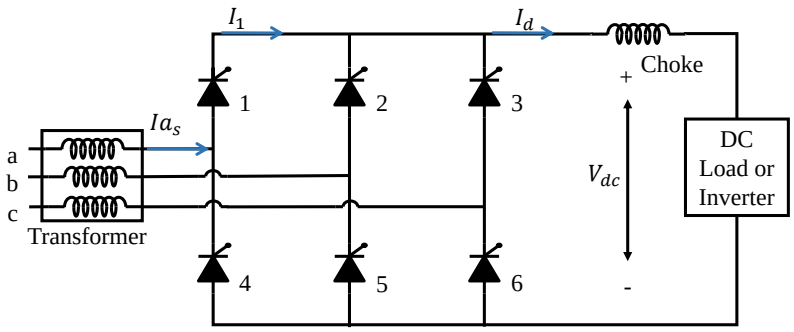


Figure I.5: Three-Phase, Six-Pulse Line Commutated Converter

with load level because fundamental current is proportional to load level. Voltage source converter are not often used in higher power applications (above 500HP) because of their higher current distortions [27]. The main circuit of typical voltage source converter is illustrated in Figure (I.6).

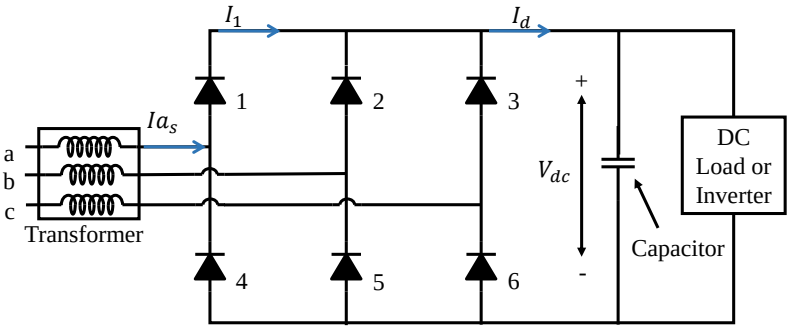


Figure I.6: Three-Phase, voltage source Converter

c- Switched-Mode Power Supplies: These power supplies are generally connected to the front-end of single phase domestic loads. They uses a full wave diode rectifier between the AC side and the capacitor. The capacitor acts as low ripple battery for the DC side. Hence, it is charged for only a fraction of half cycle which causes an extremely peaked AC waveform [27]. The main circuit of switched-mode power supplies is shown in Figure (I.7).

d- Other Nonlinear Loads: There are many other harmonic sources. Among these are cycloconverters, which directly convert 50 Hz to another frequency, static VAR compensators, which provide a variable supply of reactive power, and almost any type of "energy saving" or wave-shaping device, such as motor power factor controllers.

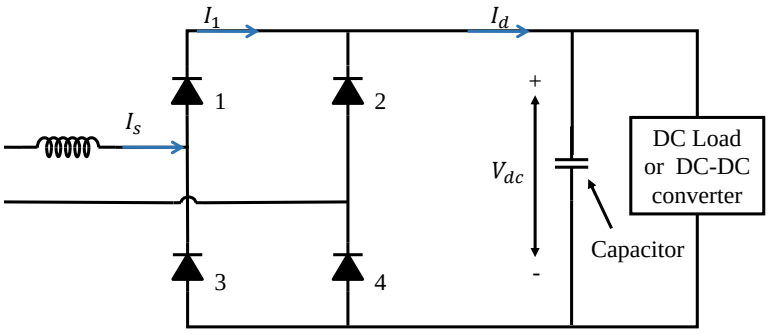


Figure I.7: Single-phase Switched-Mode Power Supply

I.2.3.2 Effects of harmonics

Harmonics cause several undesirable effects such as equipment malfunctions, dielectric breakdowns, heating and therefore losses, mechanical vibrations. This leads to a significant economic impact, degradation of energy efficiency, components over-sizing [7]. These effects can be classified into two types:

a- Instant effects:

- Interference with regulation devices.
- Shifting the voltage zero crossing, which influences the thyristors switching conditions.
- Poor precision in measuring devices (energy meter, instrumentation, etc.)
- Interference with remote control systems used by energy distributors.
- Harmonic currents generate vibrations and acoustic noises, especially in electromagnetic devices (transformers, inductors).
- Disturbances in low current lines (telecommunications, local networks, etc.).
- Unexpected switching off of protection circuits [28].

b- Long-term effects:

- Cables overheating and extra losses leading to equipment degradation and over-sizing.

- Capacitors breakdown due to the extra heating.
- Additional losses in transformers and inductors.
- Mechanical deterioration of equipment due to vibrations and pulsating torques [7].

I.2.3.3 Common Terms used in Analysing Harmonics

Several terms are used to quantify these disturbances, among them:

a- Harmonic distortion of h order:

Is defined by the distortion of harmonic of 'h' order with respect to the fundamental component [17], as expressed in equation (I.13).

$$S_h = \frac{C_h}{C_f} \tag{I.13}$$

b- Total Harmonic Distortion:

Total harmonic distortion (THD) is one of the most commonly used terms to indicate the harmonic content of the waveform [29]. This term can be expressed by:

$$THD_I = \frac{\sqrt{\sum_{h=2}^{\infty}\left(\frac{I_h}{\sqrt{2}}\right)^2}}{\frac{I_1}{\sqrt{2}}} = \frac{\sqrt{\sum_{h=2}^{\infty}\left(I_h\right)^2}}{I_1} \tag{I.14}$$

Line losses always increase when harmonics are present because these losses are proportional to the square of the RMS current [25, 29].

c- Power factor:

Apparent power in balanced three-phase systems can be defined by:

$$S = V_{rms} \cdot \mathrm{I_{rms}} = \mathrm{V_{rms}} \cdot \sqrt{\frac{1}{T}\int_0^T i_l^2 dt} \tag{I.15}$$

Where i_l is the current required by the load and can be expressed by:

$$i_l = i_f + i_h \tag{I.16}$$

i_f: the fundamental component of i_l.

i_h: the harmonic component of i_l.

The power factor can be expressed by:

$$Fp = \frac{P}{S} = \frac{P}{\sqrt{P^2 + Q^2}} \tag{I.17}$$

Where P and Q are the active and reactive power respectively:

$$P = VI \cdot \cos(\phi) \tag{I.18}$$

$$Q = VI \cdot \sin(\phi) \tag{I.19}$$

Where ϕ is the phase angle. In case of harmonics, the harmonic current increases and additional distorted power D appears as shown in Figure (I.8). This power can be defined as:

$$D = V_{rms}\sqrt{\sum_{h=2}^{\infty} i_h^2} \tag{I.20}$$

The new apparent power can be expressed by:

$$S = \sqrt{P^2 + Q^2 + D^2} \tag{I.21}$$

Therefore, the power factor is expressed by the following expression:

$$Fp = \frac{P}{\sqrt{P^2 + Q^2 + D^2}} \tag{I.22}$$

Hence, it can be noticed that the power factor decreases by the presence of harmonics and reactive power consumption [30].

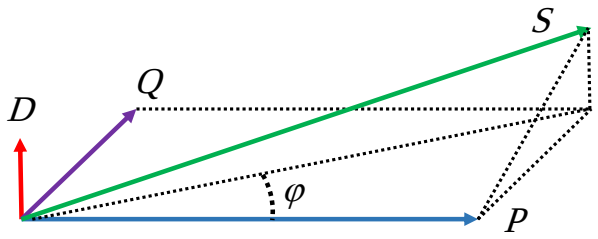


Figure I.8: Fresnel diagram

c- Crest factor

Crest factor can be defined by the ratio of the peak value of a signal to its RMS value [31], as follows:

$$\text{Crest Factor(CF)} = \frac{\text{Peak value}}{\text{RMS value}} \tag{I.23}$$

I.2.3.4 Power quality standards related to harmonic distortion

The IEEE-519 "IEEE recommended practice and requirement for harmonic control in electric power systems" [32], is the mostly used standard for power quality limits [22]. Harmonic limits of voltage and current in this standard are listed in Table (I.3) and Table (I.4) respectively.

Bus voltage V at PCC	Individual harmonic (%)	Total harmonic distortion THD (%)
$V \leq 1.0\ kV$	5.0	8.0
$1\ kV < V \leq 69\ kV$	3.0	5.0
$69\ kV < V \leq 161\ kV$	1.5	2.5
$161\ kV < V$	1.0	1.5^a

Table I.3: Voltage Distortion Limits [32].

[a]High-voltage systems can have up to 2.0% THD where the cause is a high voltage direct current (HVDC) terminal whose effects will have attenuated at points in the network where future users may be connected.

Maximum harmonic current distortion in presence of I_L						
Individual harmonic order (odd harmonics)[a,b]						
I_{sc}/I_L	$3 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h \leq 50$	TDD
$< 20^c$	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$0 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

Table I.4: Current Distortion Limit for Systems rated 120V through 69kV [32].

[a]Even harmonics are limited to 25% of the odd harmonic limit above.

[b]Current distortion that result in a dc offset, e.g., half-wave converters, are not allowed.

[c]All power generation equipment is limited to these values of current distortion, regardless of actual I_{SC}/I_L .
where:

I_{sc}= maximum short-circuit current at PCC.

I_L= maximum demand load current (fundamental frequency component) at the PCC under normal load operating conditions.

h = Individual harmonic order.

TDD=Total Harmonic distortion (or) the total root-sum-square harmonic current distortion expressed in percent of maximum demand load current [32].

I.2.4 Voltage unbalance

In balanced three-phase systems, the three phase signals have the same magnitude with a phase shift of $\frac{2\pi}{3}$. However, any variation of their magnitude and phase as shown in Figure (I.9) will eventually cause a zero phase sequence component and a negative phase sequence component. The voltage unbalance factor (VUF) can be defined by the ratio of the negative sequence voltage Vs^- to the positive sequence voltage Vs^- [33, 34]:

$$(\text{VUF}\%) = \frac{Vs^-}{Vs^+}.100\% \tag{I.24}$$

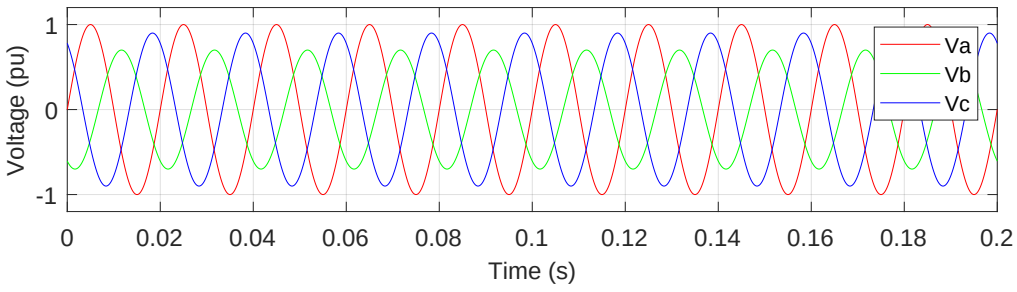


Figure I.9: Voltage unbalance

I.2.5 Voltage spikes

Voltage spikes is a quick voltage variation for a short duration from microsecond to millisecond as illustrated in Figure (I.10). This phenomenon occurs due to lightning, connecting and disconnecting heavy loads and power system faults. Voltage spikes could cause equipment malfunctions and data loss [23] [15].

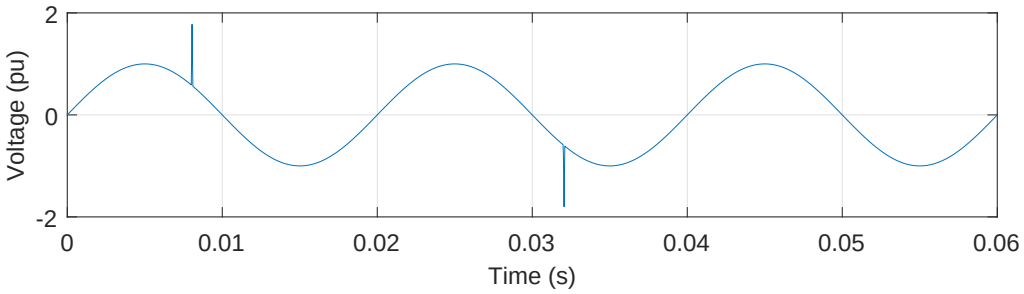


Figure I.10: Voltage spikes

I.2.6 Voltage flicker

Voltage flicker caused by the periodical operation of large loads in weak power distribution system. This resulting fluctuations cause a visible lighting flicker on incandescent or fluorescent lamps. In addition, voltage flicker can also cause electrical equipment efficiency drop, torque and power oscillations, and interference in protection systems [35]. This phenomenon is presented in Figure (I.11)

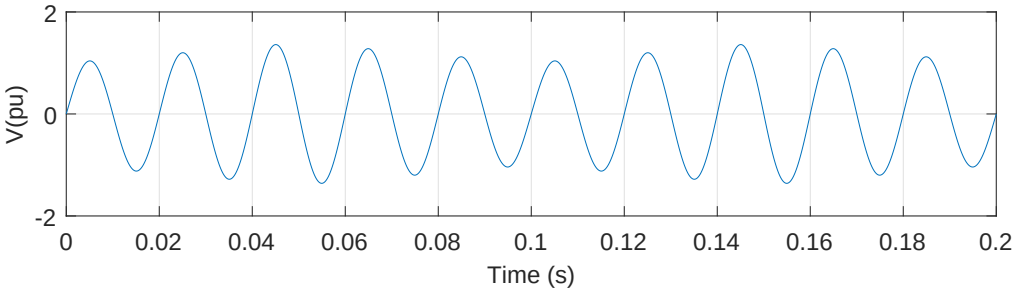


Figure I.11: Voltage flickers

I.3 Harmonics mitigation

Commonly, there are two mitigation techniques to eliminate current harmonics, namely, passive and filters. These two techniques can be classified into series and parallel (shunt) configurations [36].

I.3.1 Passive filters

Passive power filters are single frequency filters which absorb individual harmonics. Passive filters are used to eliminate an individual harmonic by tuning their band-pass characteristics. Generally, passive power filters are composed of a series-resonant inductor-capacitor (LC) circuit tuned to reduce the harmonics of a single frequency. The performance of passive filters is related to the value of the impedance of the system [24, 31]. There are several configurations of passive filters as illustrated in Figure (I.12).

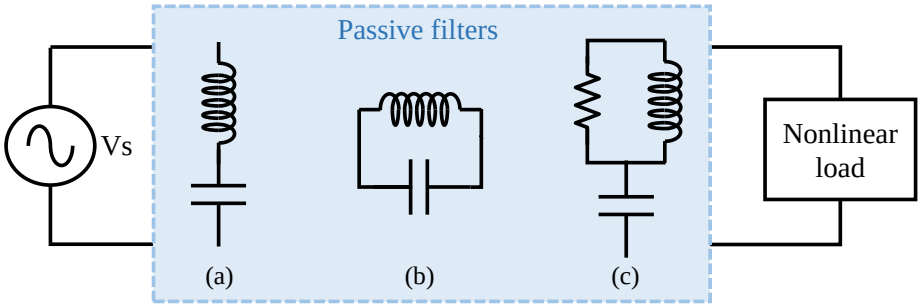


Figure I.12: a- Single tuned filter, b- series filter, and c- 2^{nd} order high-pass filter

I.3.2 Active power filters

Due to the drawbacks of the passive filters such as resonance problem and limited performance, active power filters (APFs) were developed to reduce the power quality problems. Active power filters are based on power electronics to produce a compensating current to reduce the harmonic currents and voltages [37].

I.3.2.1 The state of the-art of shunt active power filters

Even though there were previous references discussing the basic idea of active power filter [38, 39], the first shunt active power filter configuration were initially designed using PWM inverters based on power transistors in the early 70s [40]. These filters were mainly developed to suppress harmonics caused by the converters used on HVDC transmission systems [41]. However, at that time, it was still difficult to extend the use of these systems to industry. In fact, the transistors available at that time were not able to satisfy the requirement of the industrial applications in terms of switching frequency and power rating [42].

In 1977, the mentioned limitations were overcome by the means of the first active filter prototype based on naturally commutated thyristors for harmonic current elimination [43]. However, the use of the active power filter based on thyristors was precluded because they introduced the problem of injecting unwanted components into the grid.

Over the following years, remarkable progress of fast switching devices has spurred interest in the study of active power filters for reactive power and harmonic compensation. In addition to sophisticated PWM inverter technology, the development of the so-called "PQ theory" has made it possible to put them into a practical testing stage [44].

In 1982, a shunt active conditioner of 800 kVA, which consisted of a current-source PWM inverters using GTO thyristors, was put into practical use for harmonic compensation for the first time in the world. Moreover, attention was paid to the combined system of an active power line conditioner and a shunt passive filter to reduce initial costs and to improve efficiency [44].

A few years later, several shunt active power filters were designed using PWM power inverters based on GTO and IGBT transistors to meet the industrial requirements [45–47].

In 1986, a combined system of a shunt active conditioner of rating 900kVA and a shunt passive filter of rating 6600kVA was practically installed to suppress the harmonics produced by a large capacity cycloconverter for steel mill drives [44].

Since 1990, shunt active power filters began to be commercialized and installed across the world especially in Japan. Where more than 500 shunt active power filters were installed in a range of 50kVA to 2MVA by 1996 [48].

Until that time, limiting current distortion caused by power electronic equipment was done by individual low-power end-users and high- power consumers. Whereas, electric utilities were responsible for limiting voltage distortion at the point of common coupling in distribution systems [49].

I.3.2.2 Classification of active power filters

Active power filters can be categorized into several categories in terms of the used converter, system conditions, power rating, and connection type.

According to the converter structure : According to the used converter, active power filters can be classified into voltage source converter (VSC) based filters and current source converter (CSC) based filters.

- **VSI-based active filters:** active filters based on voltage source inverter use a capacitor at the DC-link of the converter as an energy storage element. Moreover, they are connected to the point of the common coupling through a coupling filter, which helps to eliminate the high frequency voltage ripples produced by the power converter. Figure (I.13) shows the circuit diagram of an active power filter based on three phase two level VSI [50].

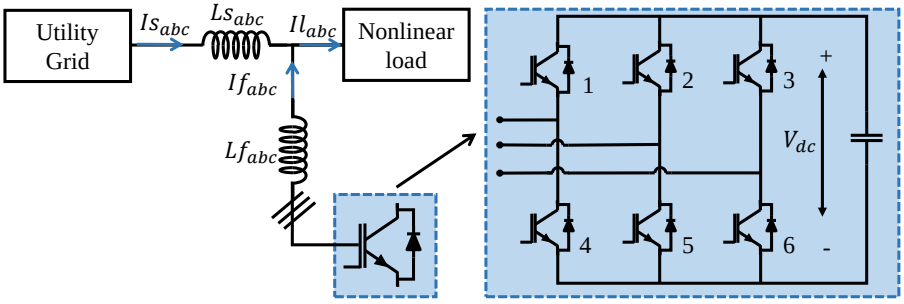


Figure I.13: Circuit diagram of shunt active power filter based on VSI

- **CSI-based active filters:** On the other hand, current source Inverter based active power filters use an inductor as an energy storage element. In these filters a filtering capacitor is highly needed in the converter terminals to filter the high frequency current ripple generated by the current source Inverter. Alike in the VSI based filter, a coupling inductor is used as in interface between the filter and the grid [50]. A three phase three wire current source inverter (CSI) based active filter is shown in Figure (I.14).

Despite robust current controllability, high reliability and fast response of CSIs, their switches must be connected to a series diode which eventually increases the cost and the size of the inverter. In addition to losses introduced by the inductor connected to the DC-link. For such reason VSIs are preferable because of the small size, lower cost and higher efficiency [50].

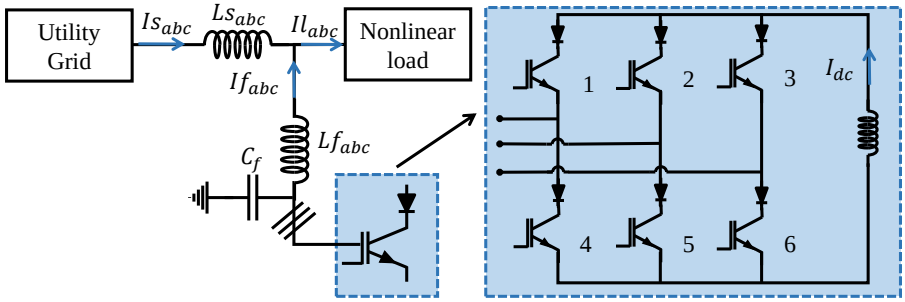


Figure I.14: Circuit diagram of shunt active power filter based on CSI

According to the topology

APFs can also be classified into four categories according to their topologies, as follows: series active power filters, shunt active power filters, hybrid active power filters and unified power quality conditioner [50].

- **Series active power filters:** These configuration of active power filters was introduced in the early 80s. They are used as voltage regulators and harmonic isolators between the nonlinear load and utility system. They operate by modifying the impedance of the grid. They can eliminate the voltage disturbances of the grid or the ones caused by harmonic currents circulation from the one hand, and protect the end user form poor supply voltage quality, voltage sag, and voltage unbalance from the other hand. Series active power filters are considered as a low-cost alternative to Uninterruptible Power Supplies (UPS). The rated power of series APFs is small (around 5% of load rating), which is an advantage of this configuration [51]. Generally, these filters use CSI as illustrated in Figure (I.15).

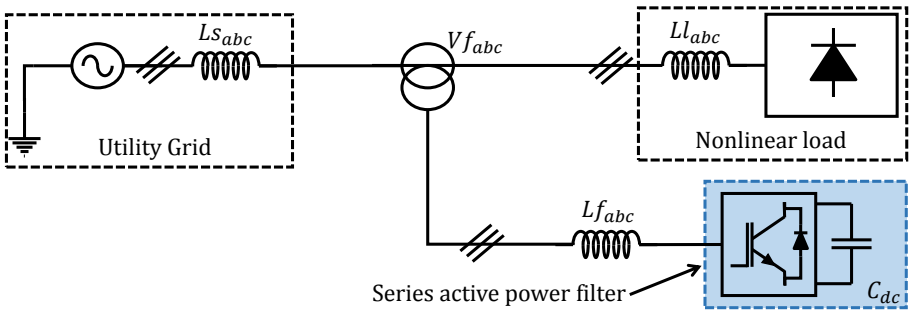


Figure I.15: Series active power filter

- **Shunt active power filters:** In this configuration, SAPFs are connected in parallel to the nonlinear load as shown in Figure (I.16). They are controlled to cancel out the harmonic current by injecting compensating currents. They are often used because they are able to suppress multiple harmonic orders, improve the power factor and acts as reactive power generator [52], [31].

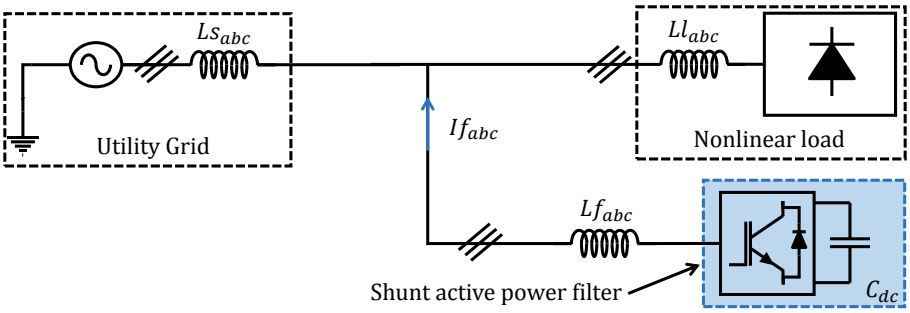


Figure I.16: Shunt active power filter

- **Unified power quality conditioner:** The unified Power Quality Conditioner (UPQC) is a combination of both shunt and series active power filters. Therefore, UPQC is able to compensate current and voltage harmonics at the same time and provide the advantages of the both configurations [31], [17]. The scheme of UPQC is illustrated in Figure (I.17).

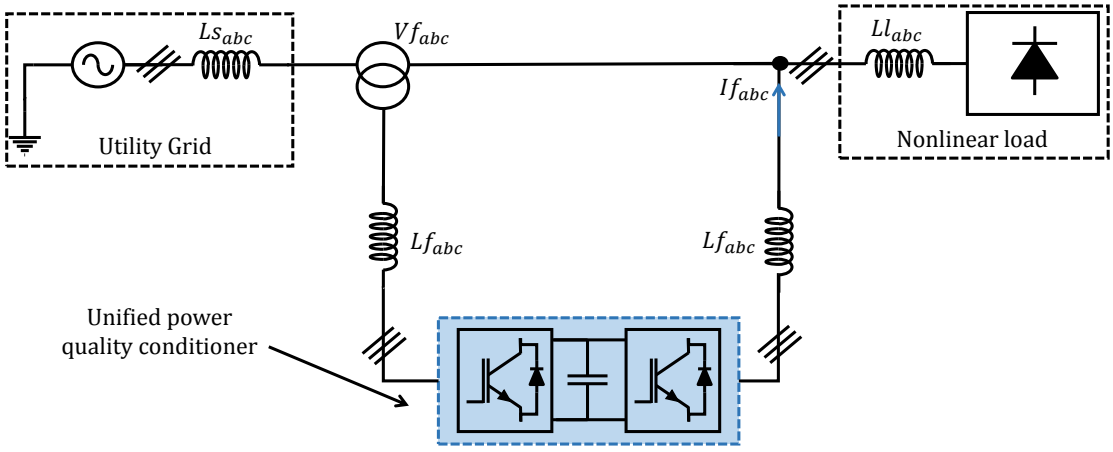


Figure I.17: Unified power quality conditioner

I.3.3 Passive filters and active filters comparison

An overall performance evaluation of active power filter and passive power filters is provided in Table (I.5).

Comparison criteria	Passive filter	Active filter
Influence on harmonic currents	Requires a filter for each harmonic	Acts simultaneously on several frequencies
Interaction between neighboring filters	Destruction risk of filters tuned to neighboring frequencies (resonances)	No risk
Influence of frequency variation	Reduced efficiency (the filter is tuned for an exact frequency)	No risk
Grid impedance variation	Risk of harmonic amplification	No consequences
Aging	Risk of performance degradation	No influence on performance
Connection	Case by case study	No preliminary study
Operating monitoring	No monitoring	Ensured by control system
Influence of current increase	Risk of overload and deterioration	No risk of overload, but reduced efficiency
Adding extra equipment	Requires modifications to the filter, in some cases	No problem (within the limit of filter rating)
Size	Large	Small
Weight	High	Low
Cost	Lower components cost, sizing study is required	Higher components cost, no cost of sizing study

Table I.5: Passive filters and active filters comparison

I.4 Conclusion

This chapter has been devoted to the study of different power quality problems especially harmonic currents which may cause equipment overheating, mechanical vibrations, and disturbances in communications lines. Then, common terms used in analyzing harmonics have been presented followed by power quality standards related to harmonic distortion. Next, to reduce these effects, conventional passive mitigation techniques and modern active mitigation techniques were exhibited. The conventional solutions suffer from several drawbacks such as their large size, inflexibility and susceptibility to resonance phenomena. Therefore, Modern solutions based on active power filtering have been gaining interest because of their flexibility, tiny size, and efficiency.

Chapter II

Shunt active power filter: Structure, modelling, and control techniques

II.1 Introduction

This chapter is devoted to providing the detailed mathematical modelling and simulation of shunt active power filter. Firstly, for harmonic currents identification, the instantaneous reactive power and synchronous reference frame methods are discussed and evaluated in accordance with their performance under severe grid conditions .
Then, for the control of the injected current, the performance of three current controllers (hysteresis, PWM, and backstepping controller) are evaluated under static and dynamic nonlinear load conditions. Finally, the simulation results and the overall evaluation of the mentioned control approaches are presented.

II.2 Shunt active power filter

In the SAPF structure the VSI is connected in parallel with the nonlinear load. The DC-link capacitor is considered as DC voltage source. Hence, maintaining constant and reducing the fluctuation of the voltage across its terminals is a crucial factor to ensure that the DC-link voltage lies within the allowable voltage range of the power switches on the one hand, and prevent performance degradation of the filter on the other hand. The filter in connected to the grid through a first order filter which is an inductor. It intervene in the controllability of the injected currents. The voltage source inverter is composed of six bidirectional power switches with an anti-parallel diodes. These switches are controlled in such a way that only one switch per leg is gated on to prevent short-circuit problem and at least one switch in the upper and the lower level are gated on to prevent load isolating [7].

II.2.1 Voltage source inverter modelling

The scheme of VSI is illustrated in Figure (II.1). The output voltage varies between two levels $-v_{dc}$ and $+v_{dc}$. The upper and the lower switch of each leg are controlled in a complementary manner. The state of the power switches are selected according to the

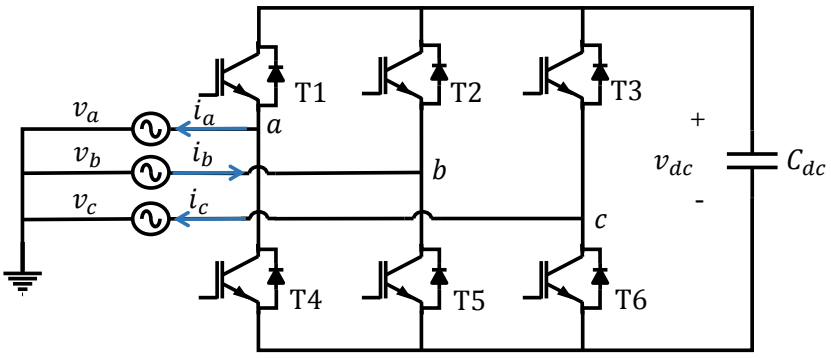


Figure II.1: VSI circuit diagram

control signals (S_a, S_b, and S_c) as follows:

$$S_a = \begin{cases} 1 & T1 \text{ ON and } T4 \text{ OFF} \\ 0 & T1 \text{ OFF and } T4 \text{ ON} \end{cases} \tag{II.1}$$

$$S_b = \begin{cases} 1 & T2 \text{ ON and } T5 \text{ OFF} \\ 0 & T2 \text{ OFF and } T5 \text{ ON} \end{cases} \tag{II.2}$$

$$S_c = \begin{cases} 1 & T3 \text{ ON and } T6 \text{ OFF} \\ 0 & T3 \text{ OFF and } T6 \text{ ON} \end{cases} \tag{II.3}$$

The output phase to phase voltages of the inverter can be obtained by the following equations:

$$\begin{cases} v_{ab} = \mathrm{v_{dc}}\,(S_a - S_b) \\ v_{bc} = \mathrm{v_{dc}}\,(S_b - S_c) \\ v_{ca} = \mathrm{v_{dc}}\,(S_c - S_a) \end{cases} \tag{II.4}$$

Whereas the output simple voltages can be obtained by:

$$\begin{aligned} v_a &= v_{dc}\tfrac{2S_a - S_b - S_c}{3} \\ v_b &= v_{dc}\tfrac{2S_b - S_a - S_c}{3} \\ v_c &= v_{dc}\tfrac{2S_c - S_a - S_b}{3} \end{aligned} \tag{II.5}$$

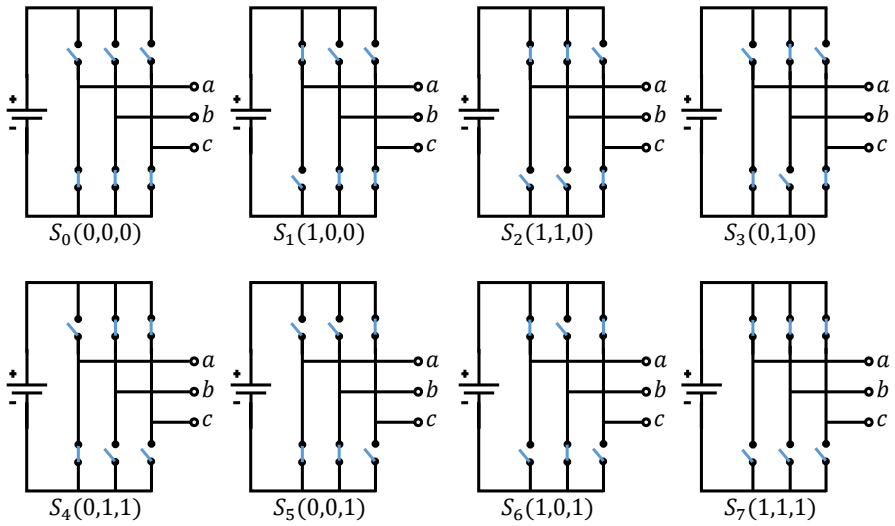


Figure II.2: The eight switching configurations of VSI

The configurations and the output voltages of the possible cases are summarized in Figure (II.2) and Table (II.1) respectively.

State	S_a	S_b	S_c	v_a	v_b	v_c
0	0	0	0	0	0	0
1	1	0	0	$2v_{dc}/3$	$-v_{dc}/3$	$-v_{dc}/3$
2	1	1	0	$v_{dc}/3$	$v_{dc}/3$	$-2v_{dc}/3$
3	0	1	0	$-v_{dc}/3$	$2v_{dc}/3$	$-v_{dc}/3$
4	0	1	1	$-2v_{dc}/3$	$v_{dc}/3$	$v_{dc}/3$
5	0	0	1	$-v_{dc}/3$	$-v_{dc}/3$	$2v_{dc}/3$
6	1	0	1	$v_{dc}/3$	$-2v_{dc}/3$	$v_{dc}/3$
7	1	1	1	0	0	0

Table II.1: Switch states for three-phase two level VSI

II.2.2 SAPF modelling

The scheme of SAPF is illustrated in Figure (II.3), wherein the capacitor C_{dc} is the energy storage element, $Rf - Lf$ is the coupling filter which is used to connect the filter at the point of common coupling (PCC).

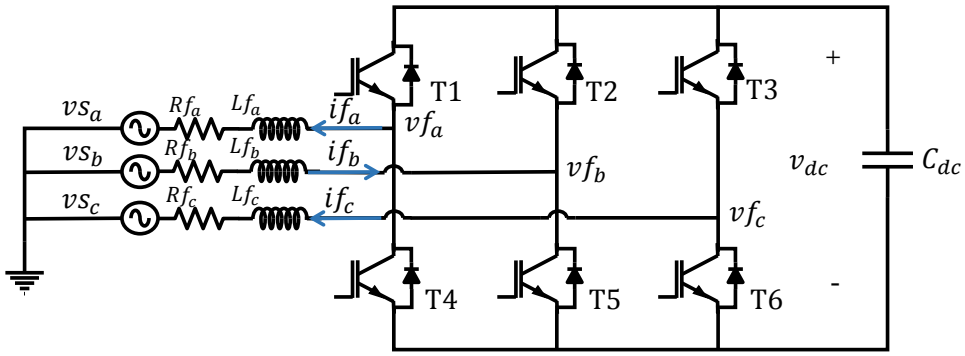


Figure II.3: SAPF circuit diagram

II.2.2.1 Model of SAPF in three-phase system (a-b-c)

In balanced systems, the source voltage can be expressed as follows:

$$\begin{aligned} vs_a(t) &= V_m \cos(\omega t) \\ vs_b(t) &= V_m \cos(\omega t - 2\pi/3) \\ vs_c(t) &= V_m \cos(\omega t + 2\pi/3) \end{aligned} \tag{II.6}$$

According the equivalent circuit illustrated in Figure (II.3), the three phase voltages can be written as:

$$\begin{aligned} vs_a &= vf_a - v_{Lf_a} - v_{Rf_a} = vf_a - Lf_a \tfrac{dif_a}{dt} - Rf_a if_a \\ vs_b &= vf_b - v_{Lf_b} - v_{Rf_b} = vf_b - Lf_b \tfrac{dif_b}{dt} - Rf_b if_b \\ vs_c &= vf_c - v_{Lf_c} - v_{Rf_c} = vf_c - Lf_c \tfrac{dif_c}{dt} - Rf_c if_c \end{aligned} \tag{II.7}$$

The three-phase equations are then given by :

$$Lf \frac{d}{dt} \begin{bmatrix} if_a \\ if_b \\ if_c \end{bmatrix} = -Rf \begin{bmatrix} if_a \\ if_b \\ if_c \end{bmatrix} + \begin{bmatrix} vf_a \\ vf_b \\ vf_c \end{bmatrix} - \begin{bmatrix} vs_a \\ vs_b \\ vs_c \end{bmatrix} \tag{II.8}$$

For the DC bus:

$$C_{dc} \frac{dv_{dc}}{dt} = S_a if_a + S_b if_b + S_c if_c \tag{II.9}$$

Therefore, the SAPF can be defined in the three-phase frame by the following equations:

$$\begin{cases} Lf_a \frac{dif_a}{dt} = -Rfif_a + vf_a - vs_a \\ Lf_b \frac{dif_b}{dt} = -Rfif_b + vf_b - vs_b \\ Lf_c \frac{dif_a}{dt} = -Rfif_c + vf_c - vs_c \\ C_{dc} \frac{dv_{dc}}{dt} = S_a if_a + S_b if_b + S_c if_c \end{cases} \tag{II.10}$$

II.2.2.2 Model of SAPF in stationary reference frame $(\alpha - \beta)$

By applying Concordia Transform on the the three-phase model given in equation (II.10), the model in the stationary reference frame can be defined by:

$$\begin{cases} Lf\frac{dif_\alpha}{dt} = -Rfif_\alpha + vf_\alpha - vs_\alpha \\ Lf\frac{dif_\beta}{dt} = -Rfif_\beta + vf_\beta - vs_\beta \\ C_{dc}\frac{dv_{dc}}{dt} = S_\alpha if_\alpha + S_\beta if_\beta \end{cases} \tag{II.11}$$

Where:

$$\begin{bmatrix} if_\alpha \\ if_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} if_a \\ if_b \\ if_c \end{bmatrix} \tag{II.12}$$

$$\begin{bmatrix} vs_\alpha \\ vs_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} vs_a \\ vs_b \\ vs_c \end{bmatrix} \tag{II.13}$$

$$\begin{bmatrix} vf_\alpha \\ vf_\beta \end{bmatrix} = \begin{bmatrix} S_\alpha \\ S_\beta \end{bmatrix} v_{dc} \tag{II.14}$$

$$\begin{aligned} S_\alpha &= \tfrac{1}{\sqrt{6}}(2S_a - S_b - S_c) \\ S_\beta &= \tfrac{1}{\sqrt{2}}(S_b - S_c) \end{aligned} \tag{II.15}$$

II.2.2.3 Model of SAPF in synchronous reference frame $(d - q)$

The equations of SAPF in the synchronous frame can be obtained by applying the Park transform as follows:

$$\begin{cases} Lf\frac{dif_d}{dt} = -Rfif_d + Lf\omega if_q + vf_d - vs_d \\ Lf\frac{dif_q}{dt} = -Rfif_q - Lf\omega if_d + vf_q - vs_q \\ C_{dc}\frac{dv_{dc}}{dt} = S_d if_d + S_q if_q \end{cases} \tag{II.16}$$

Where:

$$\begin{bmatrix} if_d \\ if_q \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} if_\alpha \\ if_\beta \end{bmatrix} \tag{II.17}$$

$$\begin{bmatrix} vs_d \\ vs_q \end{bmatrix} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \begin{bmatrix} vs_\alpha \\ vs_\beta \end{bmatrix} \tag{II.18}$$

$$\begin{bmatrix} vf_d \\ vf_q \end{bmatrix} = \begin{bmatrix} S_d \\ S_q \end{bmatrix} v_{dc} \tag{II.19}$$

$$\begin{aligned} S_d &= S_\alpha \cos\omega t + S_\beta \sin\omega t \\ S_q &= -S_\alpha \sin\omega t + S_\beta \cos\omega t \end{aligned} \tag{II.20}$$

II.3 SAPF control techniques

The main objective of the active power filter is to diminish the harmonic propagation and compensate reactive power by injecting a compensation current. Unity power factor can be achieved by ensuring a suitable control system for the APF. The whole control unite must ensure three tasks, which are producing reference currents, ensuring the control of the DC-link voltage to be equal to the reference DC-link voltage, and generating control signals which will be delivered to the VSI power switches. APFs can be evaluated in terms of their performance in both steady and dynamic periods, THD reduction, reactive power compensation, and their behaviour under fast load change. Furthermore, the harmonic identification techniques can be classified into direct and indirect techniques. In the direct techniques, the injected current is measured, while in the indirect techniques the source current is measured. [37].

II.3.1 Harmonic current identification

Harmonic identification is a crucial factor that highly influences the whole performance of the APF. For such reason, several control techniques have been widely investigated. These techniques can be classified into frequency domain and time domain. The techniques of the first category are based on Fast Fourier Transform (FFT) [53]. However, this type of techniques introduces bad performances while transients and requires heavy calculations and large computational resources [54–60]. The techniques in the second family are operating on the time domain, such as instantaneous reactive power theory

(IRPT) [61, 62], synchronous reference frame method (SRF) [63], synchronous detection method (SDM) [64], Kalman-filter based methods [65–67] , and notch filters-based techniques [68–70]. The time domain techniques have an easier implementation compared to the techniques of the frequency domain. Recently, artificial intelligence techniques such as neural networks and adaptive network based fuzzy inference system (ANFIS) are used in harmonic current identification field [37], [41].

II.3.1.1 Instantaneous reactive power theory

This method of the instantaneous reactive power theory proposed in [61] is widely used because of its advantages such as easy implementation, precision, and the ability to choose which disturbance to be compensated [42].

In the presence of harmonics the apparent power can be expressed as:

$$S = \sqrt{P^2 + Q^2 + D^2} \tag{II.21}$$

Where, P is the active power, Q is the reactive power, and D is the distorted power.

In this method, the three-phase source voltages and load currents are transformed from the *abc* system to $\alpha - \beta$ frame to estimate the real and imaginary powers. The source voltages and load currents in the $\alpha - \beta$ frame can be obtained using the following equations:

$$\begin{bmatrix} vs_\alpha \\ vs_\beta \\ vs_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} vs_a \\ vs_b \\ vs_c \end{bmatrix} \tag{II.22}$$

$$\begin{bmatrix} il_\alpha \\ il_\beta \\ il_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} il_a \\ il_b \\ il_c \end{bmatrix} \tag{II.23}$$

The instantaneous active power theory denoted by $p(t)$ can be obtained by:

$$p(t) = vs_a is_b + vs_b is_b + vs_c is_c \tag{II.24}$$

While, in the $\alpha - \beta$ frame $p(t)$ can be given by:

$$p(t) = v_\alpha i_\alpha + v_\beta i_\beta \tag{II.25}$$

Whereas, the homo-polar sequence power is :

$$p_0(t) = vs_0 il_0 \tag{II.26}$$

The instantaneous reactive power can be expressed by:

$$q(t) = -\frac{1}{\sqrt{3}}\left[(vs_a - vs_b)\, il_c + (vs_b - vs_c)\, il_a + (vs_c - vs_a)\, il_b\right] = vs_\beta i_\alpha - vs_\alpha il_\beta \tag{II.27}$$

The equations (II.25) and (II.27) can be given in matrix as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} vs_\alpha & vs_\beta \\ vs_\beta & -vs_\alpha \end{bmatrix} \begin{bmatrix} il_\alpha \\ il_\beta \end{bmatrix} \tag{II.28}$$

Generally, the instantaneous active and reactive power are composed of continuous components related to the fundamental voltage and current and oscillatory components related to the harmonics of voltage and current as given in the following equation:

$$\begin{cases} p = \bar{p} + \tilde{p} \\ q = \bar{q} + \tilde{q} \end{cases} \tag{II.29}$$

A law-pass filter can be used to ensure the decomposition of the active and reactive power into average and oscillatory components [71].

High order low-pass filters require longer calculation time [42]. Therefore, a second order low-pass filter is used in our study. The transfer function of second order low-pas filter is given by:

$$G_{lp}(s) = \frac{\omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} \tag{II.30}$$

Where $\omega_c = 2\pi.f_c$ and f_c is the cutoff frequency which allows only the flowing of the continuous component and blocks the oscillatory components [42].

The instantaneous reactive power theory provides the flexibility to choose the compensation or reference components [71]. The reference active and reactive powers are denoted by p_{ref} and q_{ref} respectively. The compensating currents in the $\alpha - \beta$ frame can be given by the following equation:

$$\begin{bmatrix} ic_\alpha \\ ic_\beta \end{bmatrix} = \frac{1}{vs_\alpha^2 + vs_\beta^2} \begin{bmatrix} vs_\alpha & vs_\beta \\ vs_\beta & -vs_\alpha \end{bmatrix} \begin{bmatrix} p_{ref} \\ q_{ref} \end{bmatrix} \tag{II.31}$$

Where;

$$\begin{bmatrix} p_{ref} \\ q_{ref} \end{bmatrix} = \begin{bmatrix} \tilde{p} - P_{dc} \\ q \end{bmatrix} \tag{II.32}$$

The reference currents in the three-phase frame can be obtained using inverse Concordia transformation as follows:

$$\begin{bmatrix} ic_a \\ ic_b \\ ic_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} ic_\alpha \\ ic_\beta \end{bmatrix} \tag{II.33}$$

The PQ theory can be used to compensate the harmonic currents, reactive power and line current unbalances according to the selected references powers [71]. The block diagram of PQ theory is illustrated in Figure (II.4).

II.3.1.1.1 DC-link voltage regulation using P_{dc}

If we assume that the inverter and coupling filter losses are neglected, the relation between the power absorbed by the capacitor and the voltage at its terminals can be written as:

$$P_{dc} = \frac{dE_{dc}}{dt} = \frac{d}{dt}\left(\frac{1}{2}C_{dc}v_{dc}^2\right) \tag{II.34}$$

By applying the Laplace transformation to this relation:

$$P_{dc}(s) = \frac{1}{2}.s.C_{dc}v_{dc}^2(s) \tag{II.35}$$

The square of the voltage across the capacitor is given by:

$$v_{dc}^2(s) = \frac{2P_{dc}(s)}{C_{dc}s} \tag{II.36}$$

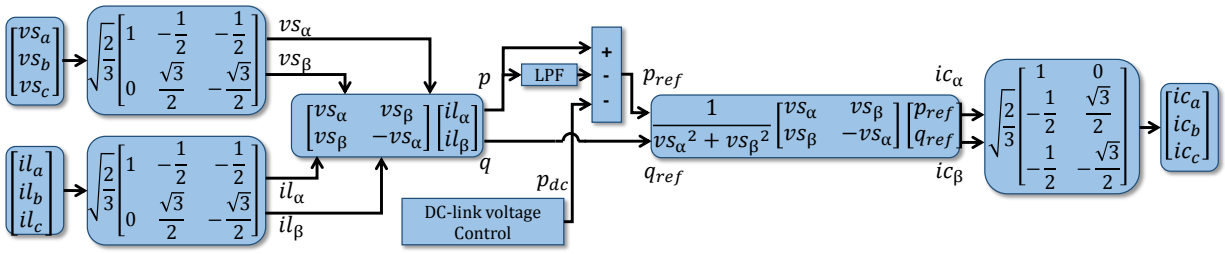


Figure II.4: PQ theory block diagram

The DC-link control scheme is illustrated is Figure (II.5), wherein PI coefficients are tuned to obtain a minimum response time so as not to affect the dynamics of the active filter [72]. From Figure (II.5), the transfer function of the DC voltage control loop is given by :

$$G_{vdc} = \frac{1 + \frac{K_{pdc}}{K_{idc}} s}{s^2 + 2\frac{K_{pdc}}{C_{dc}} s + 2\frac{K_{idc}}{C_{dc}}} \tag{II.37}$$

Using the second order transfer function expressed in equation (II.37), we find:

$$K_{idc} = \frac{1}{2} C_{dc} \omega_c^2 \tag{II.38}$$

$$K_{pdc} = \xi \sqrt{2 C_{dc} K_{idc}} \tag{II.39}$$

Where, $\omega_c = 2\pi f_c$ with f_c is the cutoff frequency [17].

II.3.1.2 Synchronous reference frame theory

In this method the three-phase load currents are transformed to $\alpha - \beta$ system as follows:

$$\begin{bmatrix} il_\alpha \\ il_\beta \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} il_a \\ il_b \\ il_c \end{bmatrix} \tag{II.40}$$

The rotating frame aligned by $\pi/2$ behind the a-axis, that is, at t=0, the q-axis is aligned with the a-axis. Thus, $d-q$ components of load current can be obtained by:

$$\begin{bmatrix} il_d \\ il_q \end{bmatrix} = \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \cdot \begin{bmatrix} il_\alpha \\ il_\beta \end{bmatrix} \tag{II.41}$$

Where θ is the phase angle obtained using Phase locked loop (PLL) controller, The active component of load current can be decomposed into average and oscillatory quantities using second order low pass filter as follows:

$$\begin{bmatrix} il_d \\ il_q \end{bmatrix} = \begin{bmatrix} \overline{il}_d + \tilde{il}_d \\ \overline{il}_q + \tilde{il}_q \end{bmatrix} \tag{II.42}$$

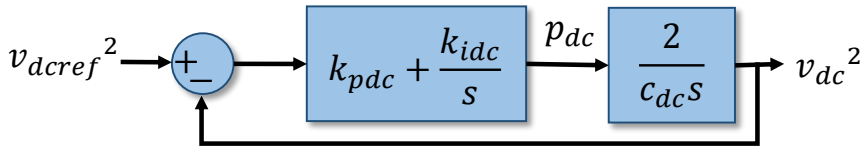


Figure II.5: DC-link voltage control loop

The compensating current in $\alpha - \beta$ system can be expressed in the following Equation:

$$\begin{bmatrix} ic_\alpha \\ ic_\beta \end{bmatrix} = \begin{bmatrix} \sin(\theta) & \cos(\theta) \\ -\cos(\theta) & \sin(\theta) \end{bmatrix} \cdot \begin{bmatrix} \tilde{il}_d - i_{dc} \\ \bar{il}_q + \tilde{il}_q \end{bmatrix} \tag{II.43}$$

Where idc is the component of the DC-link regulation. Finally, $\alpha - \beta$ coordinates of the compensating current are transformed back into abc system using inverse Clarke transformation in equation (II.44). The block diagram of SRF method is illustrated in Figure (II.6)

$$\begin{bmatrix} ic_a \\ ic_b \\ ic_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} ic_\alpha \\ ic_\beta \end{bmatrix} \tag{II.44}$$

II.3.1.2.1 Phase-Locked Loops (PLL)

Generally, the PLL unit consists of (PD) a phase detector, (LF) a loop filter and (VCO) a voltage controller oscillator as shown in Figure (II.7). The PD extracts the error $e(t)$ between the input $i(t)$ and the output signals $o(t)$.

The error is delivered to the LF to be treated. The frequency of the generated signal is regulated by the VCO [73]. The grid voltages are expressed as:

$$\begin{cases} vs_a = V_m cos(\theta) \\ vs_b = V_m cos(\theta - 2\pi/3) \\ vs_c = V_m cos(\theta + 2\pi/3) \end{cases} \tag{II.45}$$

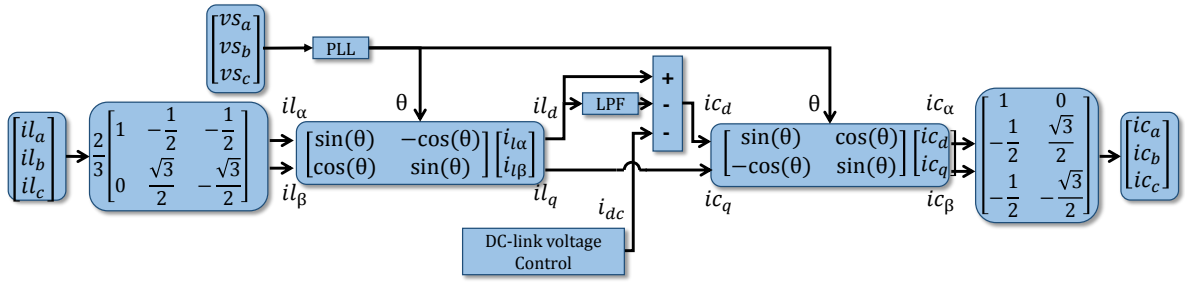


Figure II.6: SRF method block diagram

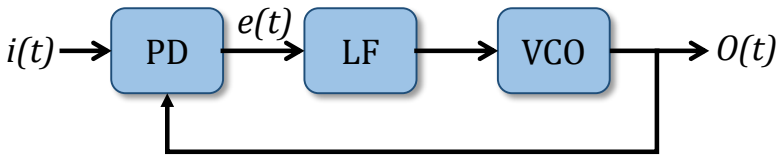


Figure II.7: Schematic diagram of PLL

Where $V_m$is the amplitude and θ is the phase angle. The three-phase grid voltages are transformed into stationary $\alpha\beta$ frame using Clarke transformation as follows:

$$\begin{bmatrix} vs_\alpha \\ vs_\beta \end{bmatrix} = \frac{2}{3}. \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} . \begin{bmatrix} vs_a \\ vs_b \\ vs_c \end{bmatrix} \tag{II.46}$$

The synchronous $d-q$ frame of the grid voltages can be obtained by:

$$\begin{bmatrix} vs_d \\ vs_q \end{bmatrix} = \begin{bmatrix} sin(\theta') & -cos(\theta') \\ cos(\theta') & sin(\theta') \end{bmatrix} . \begin{bmatrix} vs_\alpha \\ vs_\beta \end{bmatrix} \tag{II.47}$$

Where θ' is the estimated phase angle.

Therefore,

$$\begin{cases} vs_d = V_m.cos(\theta - \theta') \\ vs_q = V_m.sin(\theta - \theta') \end{cases} \tag{II.48}$$

When the estimated phase angle approaches the real phase angle of the grid voltages, the grid voltages in the $d-q$ synchronous frame become:

$$\begin{cases} vs_d = V_m \\ vs_q = 0 \end{cases} \tag{II.49}$$

To achieve a good phase angle estimation, the error between the estimated and the real phase angle is fed to a PI regulator to be minimized [73]. The diagram of the used PLL is illustrated in Figure (II.8).

II.3.1.2.2 DC-link voltage regulation using I_{dc}

The voltage across the DC-link can be expressed by:

$$v_{dc} = \frac{1}{C_{dc}} \int I_{dc} dt \tag{II.50}$$

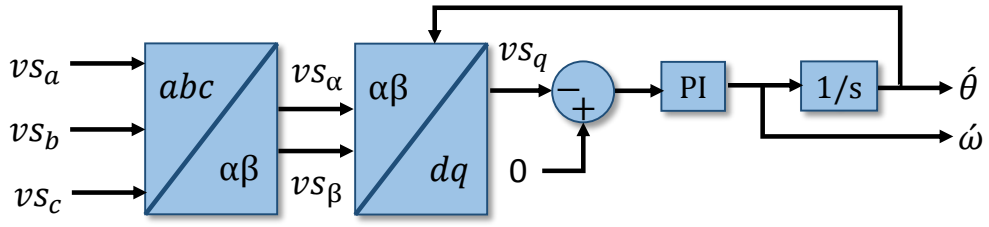


Figure II.8: Block diagram of dq-PLL

By applying the Laplace transform we find:

$$v_{dc} = \frac{1}{s.C_{dc}} I_{dc} \tag{II.51}$$

From Figure (II.9), the closed loop transfer function is written as:

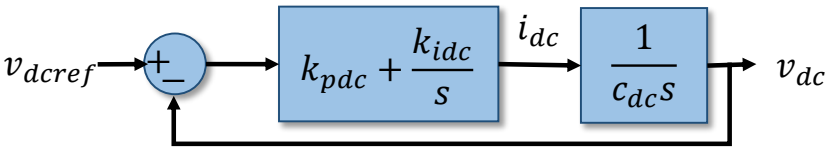


Figure II.9: DC-link voltage control loop

$$G_{vdc} = \frac{\left(1 + \frac{K_p}{K_i} s\right) \omega_c^2}{s^2 + 2\xi\omega_c s + \omega_c^2} \tag{II.52}$$

The PI controller parameters can be estimated as follows [72]:

$$K_{idc} = \omega_c^2 C_{dc} \tag{II.53}$$

$$K_{pdc} = 2\xi\sqrt{K_{idc} C_{dc}} \tag{II.54}$$

II.3.1.3 Simulation results

To choose the most suitable current identification technique for our filter, extensive simulations under several scenarios have been carried out. Firstly, the shunt active power filter is connected to the PCC with nonlinear load to observe its behaviour. Secondly, a sudden load demand increase is applied to test the PQ and SRF estimators under dynamic load conditions. Finally, the shunt active power filter is tested under normal and severe grid conditions. The simulation parameters are listed in Table (A.1).

II.3.1.3.1 SAPF based on PQ theory

The overall circuit diagram of the shunt active power filter based on instantaneous reactive power theory is illustrated in Figure (II.10).

Nonlinear load:

Figure (II.11-a) shows that the source current and load current of phase A are distorted due to the harmonic components generated by the nonlinear load and the injected current is null as illustrated in Figure (II.11-b). After the activation of the active power filter at 0.06 it starts injecting the compensating currents which eliminates the harmonics. Therefore, the source current becomes quasi-sinusoidal with THD of 3.46% as shown in Table (II.2). Moreover, the source current is in phase with the grid voltage as shown in Figure (II.11-c). The voltage across the DC-link starts tracking the reference voltage after the activation of the filter after a transient period of 0.01s as shown in Figure (II.12-a). Figure (II.12-b) and Figure (II.12-c) show that the instantaneous active power of the main source has less oscillations after initiating the filter and the reactive power is well compensated.

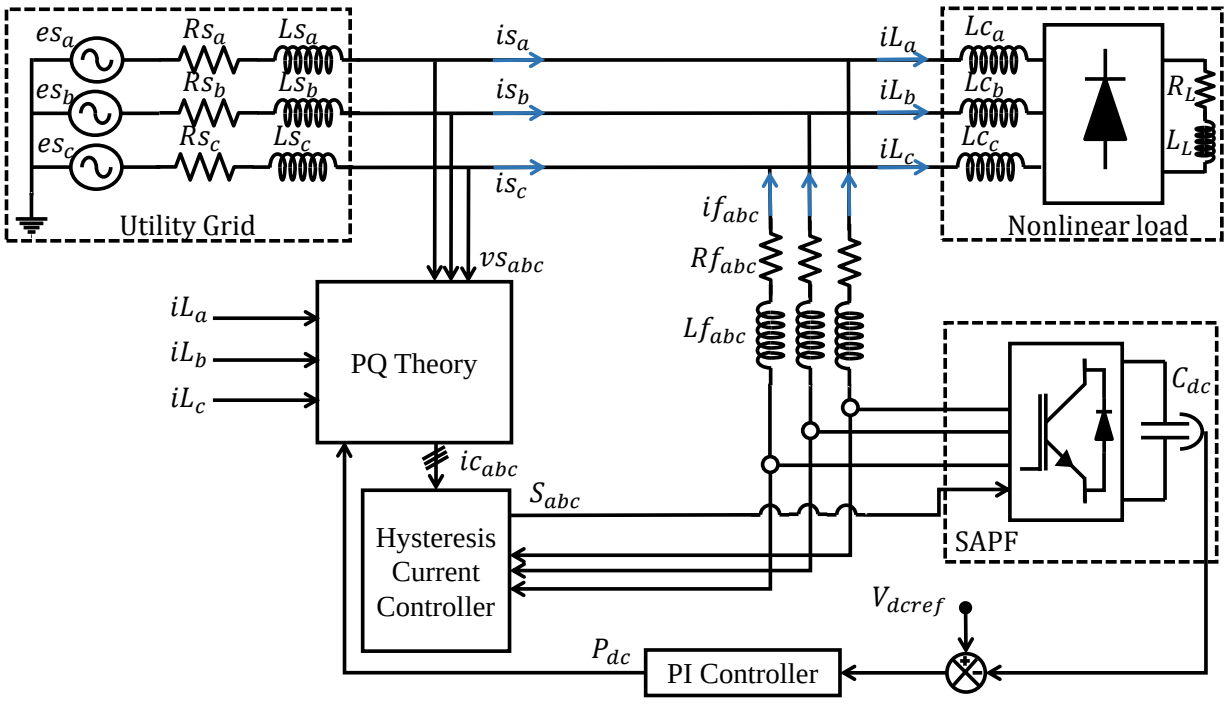


Figure II.10: Circuit diagram of SAPF based on PQ theory

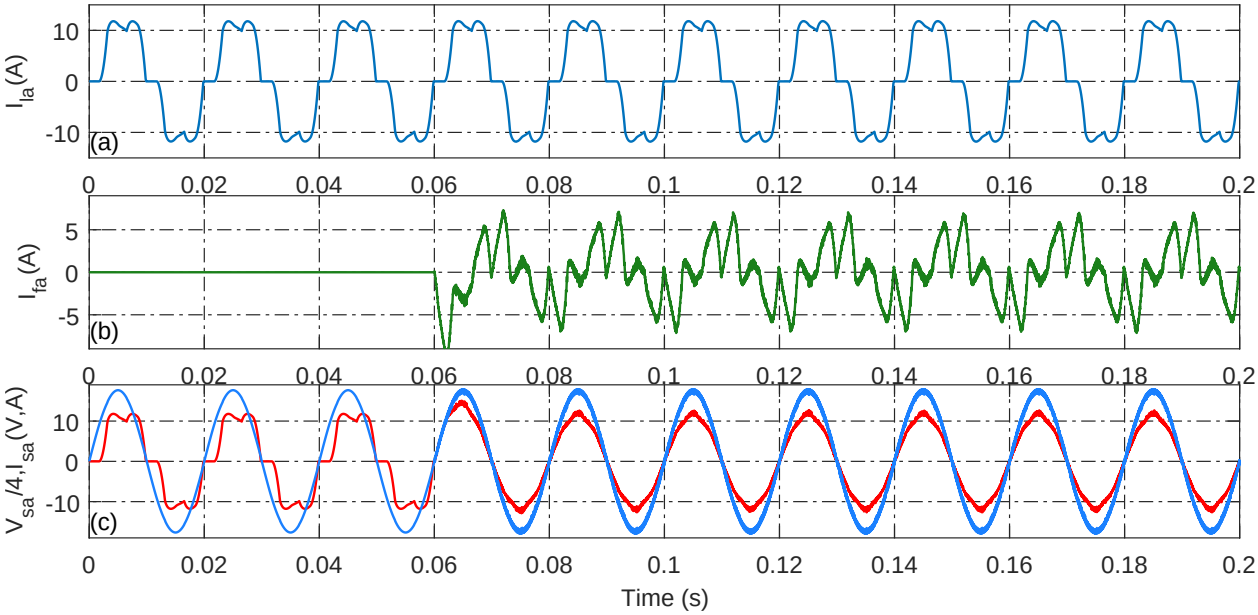


Figure II.11: Nonlinear load: a- load current, b- filter current, c- source current and voltage

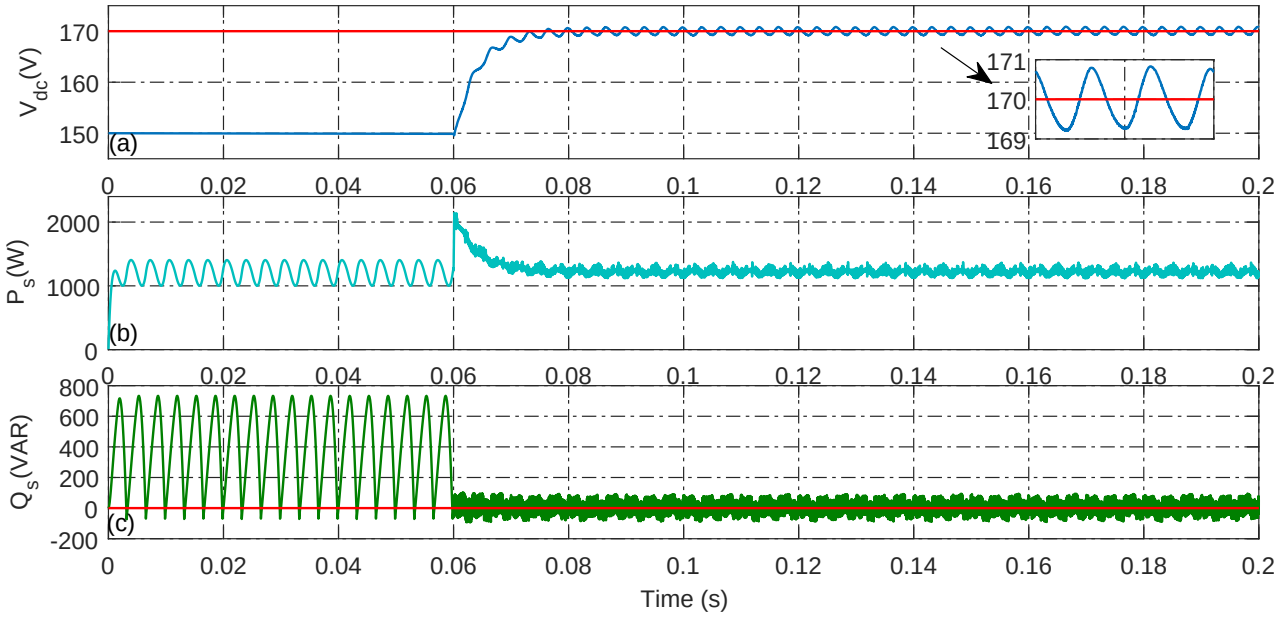


Figure II.12: Nonlinear load: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

Harmonic	Mag %	Ang- Deg	Harmonic	Mag %	Ang- Deg
(DC) 0 Hz	0.01	90	(h11) 550 Hz	0.19	-55.6
(Fnd) 50 Hz	100	-0.4	(h12) 600 Hz	0.15	-14.4
(h2) 100 Hz	0.04	-6.4	(h13) 650 Hz	0.58	252.9
(h3) 150 Hz	0.18	-54.7	(h14) 700 Hz	0.05	192.7
(h4) 200 Hz	0.07	-146.7	(h15) 750 Hz	0.12	204.7
(h5) 250 Hz	1.36	13.3	(h16) 800 Hz	0.13	140.1
(h6) 300 Hz	0.04	54.8	(h17) 850 Hz	0.46	200
(h7) 350 Hz	2.25	179.8	(h18) 900 Hz	0.09	-67.3
(h8) 400 Hz	0.02	66.6	(h19) 950 Hz	0.11	192.6
(h9) 450 Hz	0.25	21.5	(h20) 1000 Hz	0.12	-31.1
(h10) 500 Hz	0.04	105.5	THD of Is_a:		3.64%

Table II.2: THD of source current using PQ theory

Different grid conditions

a- Balanced undistorted Source voltage: Figure (II.13-a) shows that the applied grid voltage is balanced and undistorted. At 0.06s the filter start injecting the compensating currents as illustrated in Figure (II.13-b).Eventually, the harmonic components of the the three-phase source currents are suppressed and the source currents become sinusoidal with THDs between 3.28% and 3.64% as shown in Figure (II.13-c). In Figure (II.14-a), it can be seen that the voltage across the DC-link is regulated after a transient period of 0.01s, the oscillations of the instantaneous active power produced by the utility grid are minimized, and the reactive power is compensated as illustrated in Figure (II.14-b) and Figure (II.14-c) respectively.

b- Unbalanced undistorted Source voltage: In this case the magnitudes of the first phase and the third phase of the utility grid voltages are increased by 20% and decreased by 20% respectively as follows: ($\hat{Vs_a} = 84.71V$, $\hat{Vs_b} = 70.6V$, and $\hat{Vs_c} = 56.46V$) as shown in Figure (II.15-a). After the activation of the filter at 0.06 it start injecting the compensating

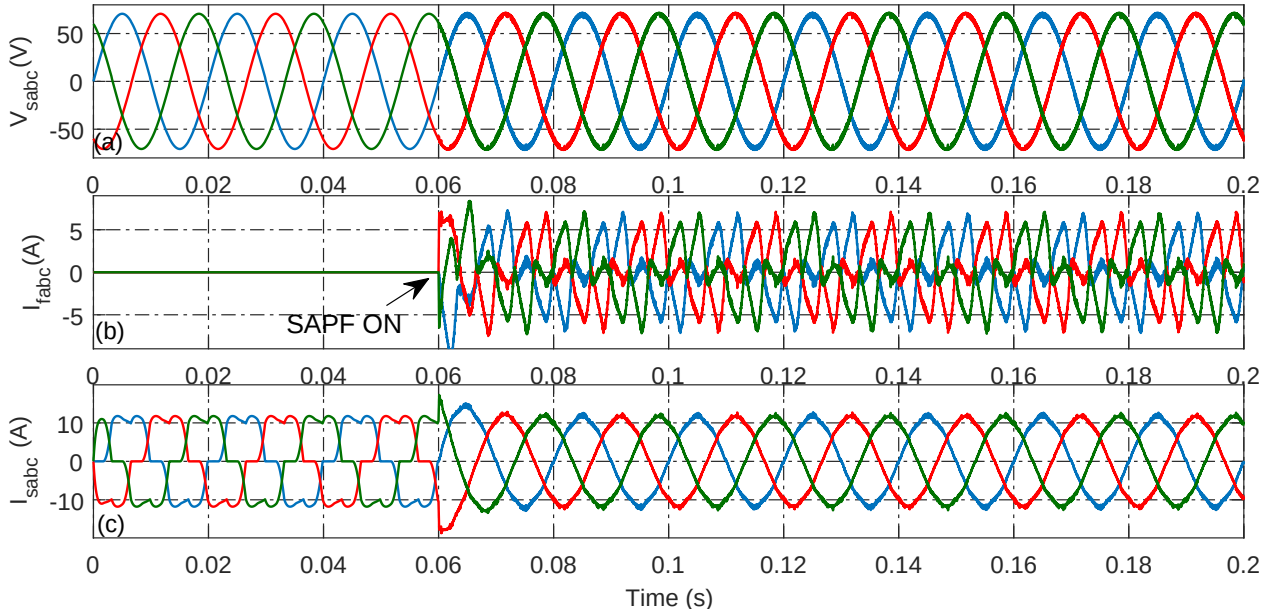


Figure II.13: Case a: a- Grid voltages, b- injected currents, and c- source currents

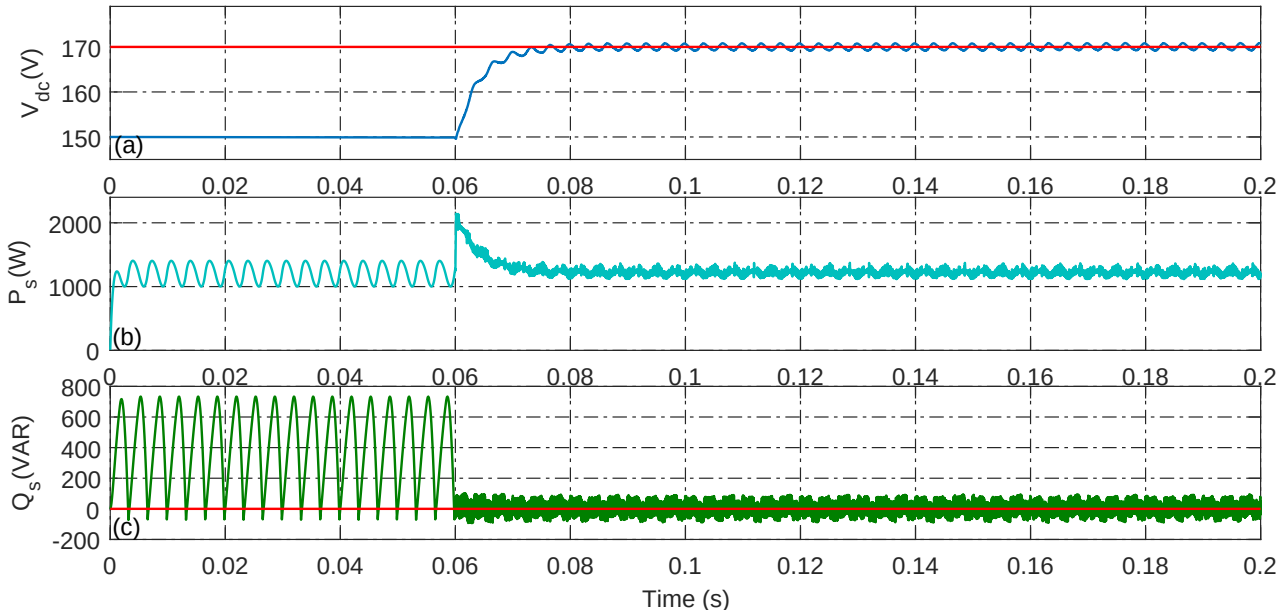


Figure II.14: Case a: DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

current as illustrated in Figure (II.15-b). The harmonic estimation accuracy is affected by the unbalances applied on the voltages of the utility grid. Thus, the harmonics of the source current are not well-compensated which can be seen in the resulted waveform illustrated in Figure (II.15-c) with THDs between 12.88% and 15.96%. The DC-link voltage and the

instantaneous active power have encountered higher oscillations because of the unbalanced grid voltages as shown in Figure (II.16-a) and Figure (II.16-b) respectively. In Figure (II.16-c) the reactive power is compensated but not as good as in the first scenario of balanced undistorted grid voltages.

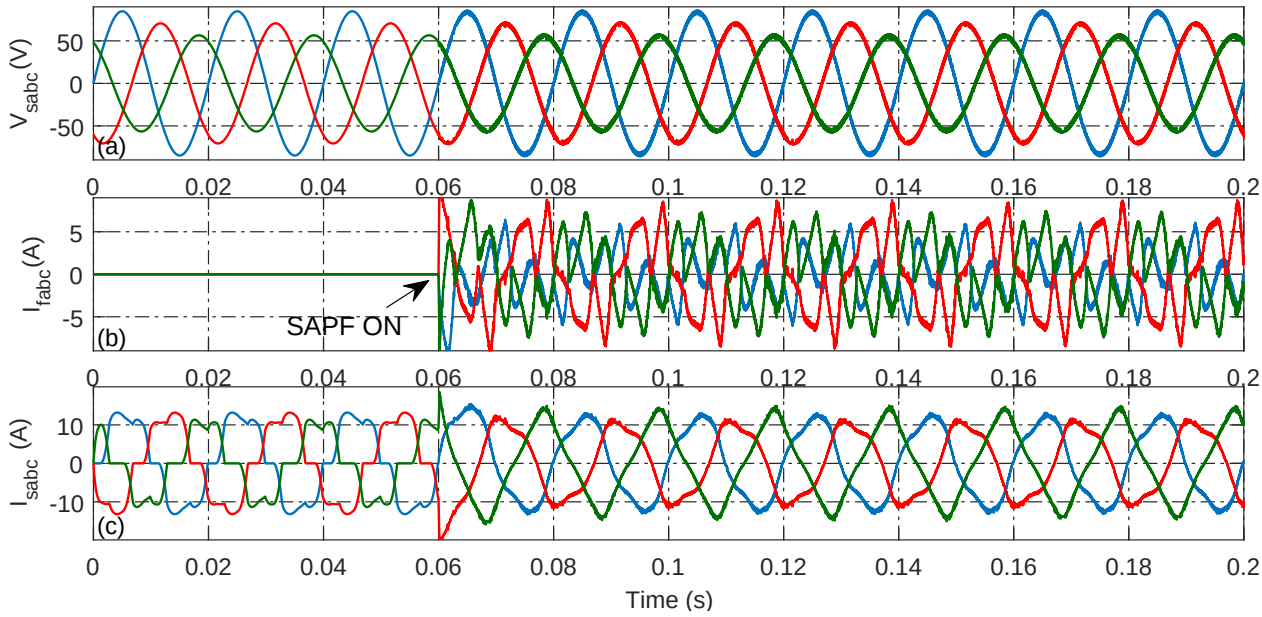


Figure II.15: Case b: a- Grid voltages, b- injected currents, and c- source currents

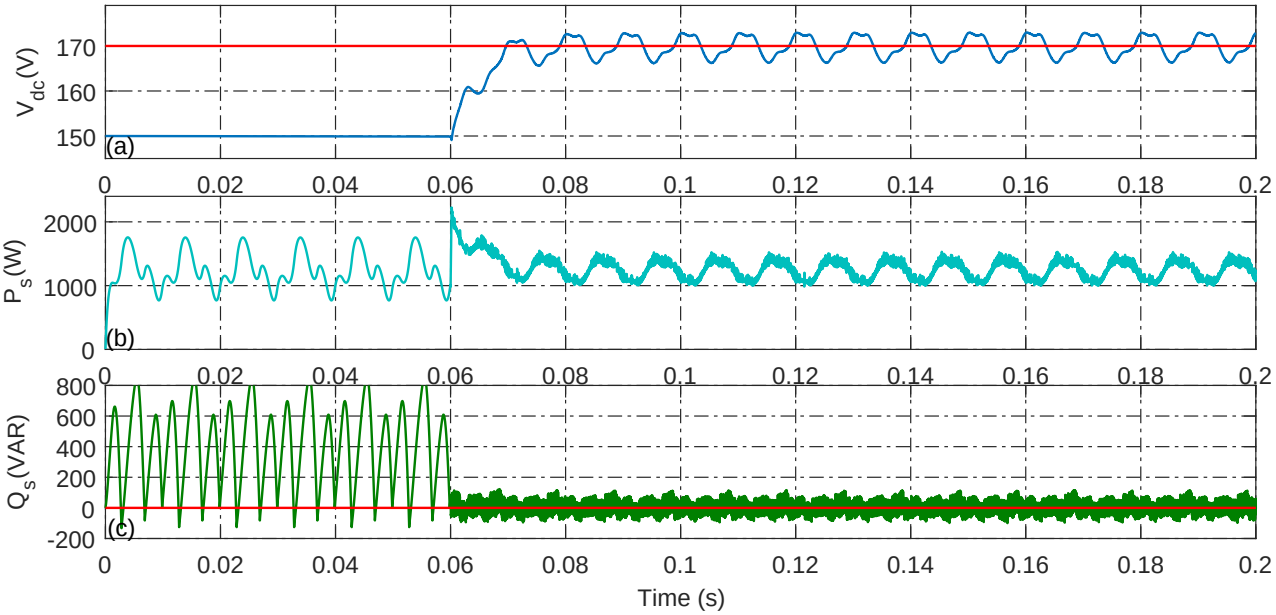


Figure II.16: Case b: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

c- Balanced distorted Source voltage: In this case the grid voltages have been contaminated by harmonic components as shown in Figure (II.17-a) . Therefore, their THD have been increased as follows (THD: $Vs_a = 7.34\%$, $Vs_b = 7.16\%$, and $Vs_c = 7.54\%$). Despite the applied distortion, the source currents are maintained sinusoidal with THD between 4.64% and 5.03% as illustrated in Figure (II.17-c). On the other hand, in Figure (II.18-a) the voltage across the DC-link is regulated after a transient period of 0.02s. the instantaneous active and reactive power have encountered higher oscillations compared to normal grid conditions as shown in Figure (II.18-b) and Figure (II.18-c) respectively.

d- Unbalanced distorted Source voltage: This case is the worst for the grid condition since both an unbalance and a distortion are applied on the grid voltages as shown in Figure (II.19-a). At 0.06 the filter is activated and started injecting the compensating current as in Figure (II.19-b). However, the unit of harmonic current identification have been highly effected by the severe condition of the utility grid.

the performance of the filter have been deteriorated as can be seen in the resulted source currents shown in Figure (II.19-c) which are unbalanced and have a THDs of ($is_a = 14.55\%$, $is_b = 18.4\%$, and $is_c = 15.45\%$).

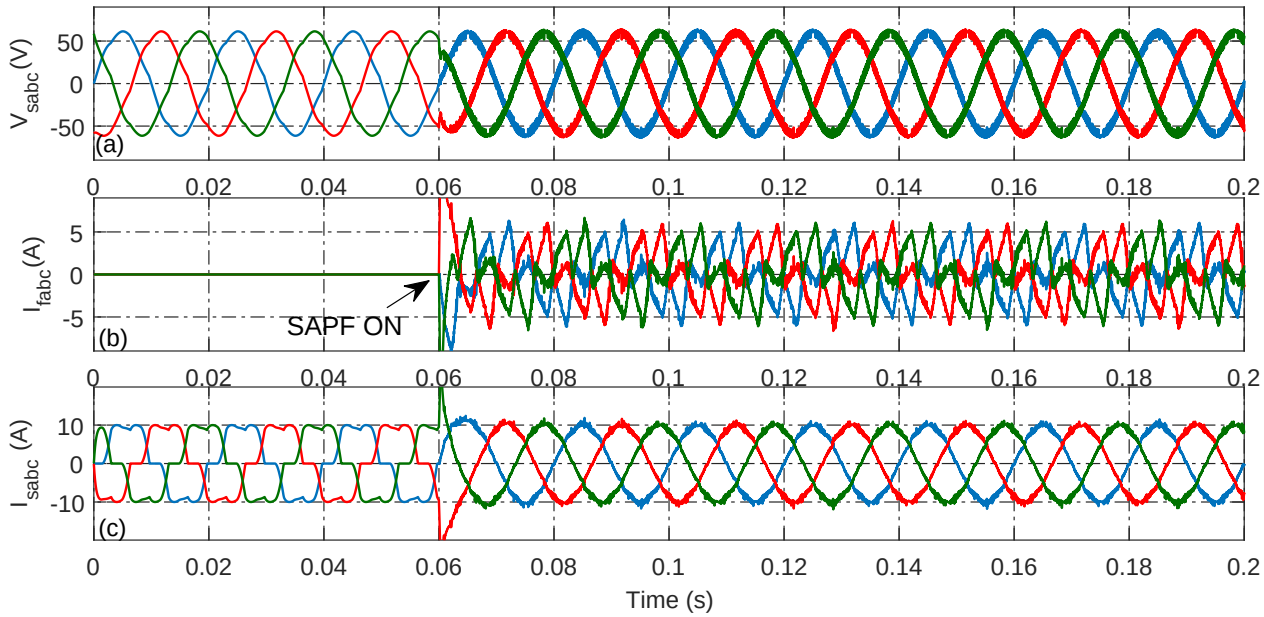


Figure II.17: Case c: a- Grid voltages, b- injected currents, and c- source currents

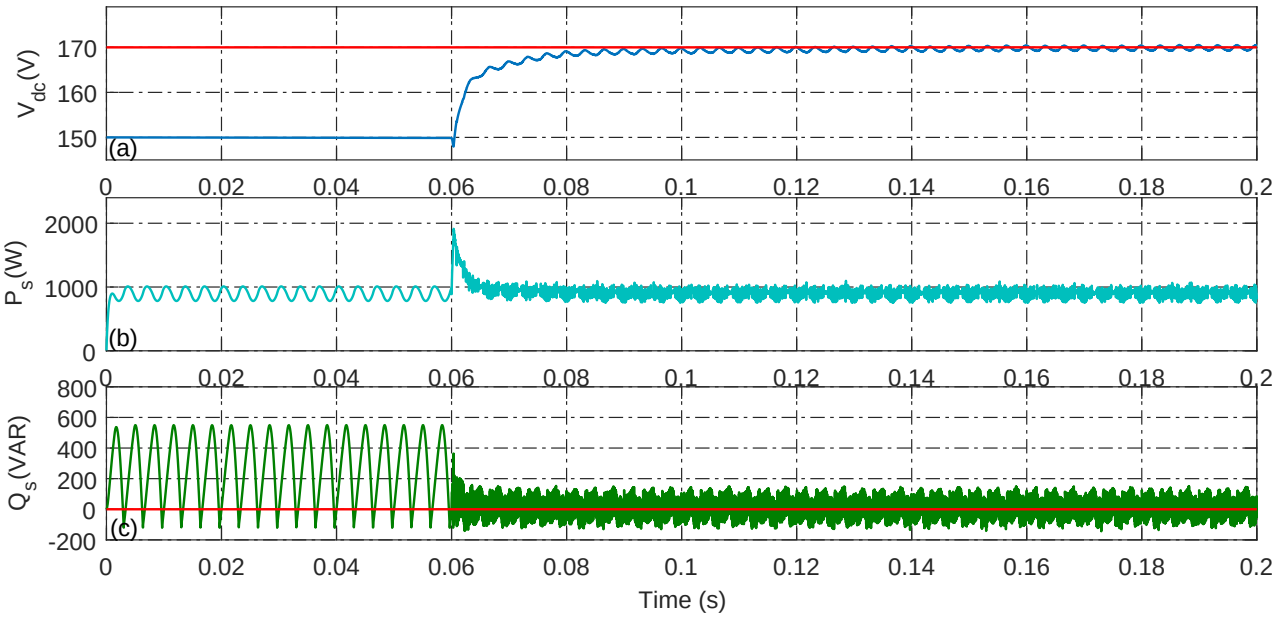


Figure II.18: Case c: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

In The DC-link voltage which encountered a high drop after the activation of the filter as shown in Figure (II.20-a), and in the instantaneous active and reactive power which have confronted higher oscillations as illustrated in Figure (II.20-b) and Figure (II.20-c) respectively.

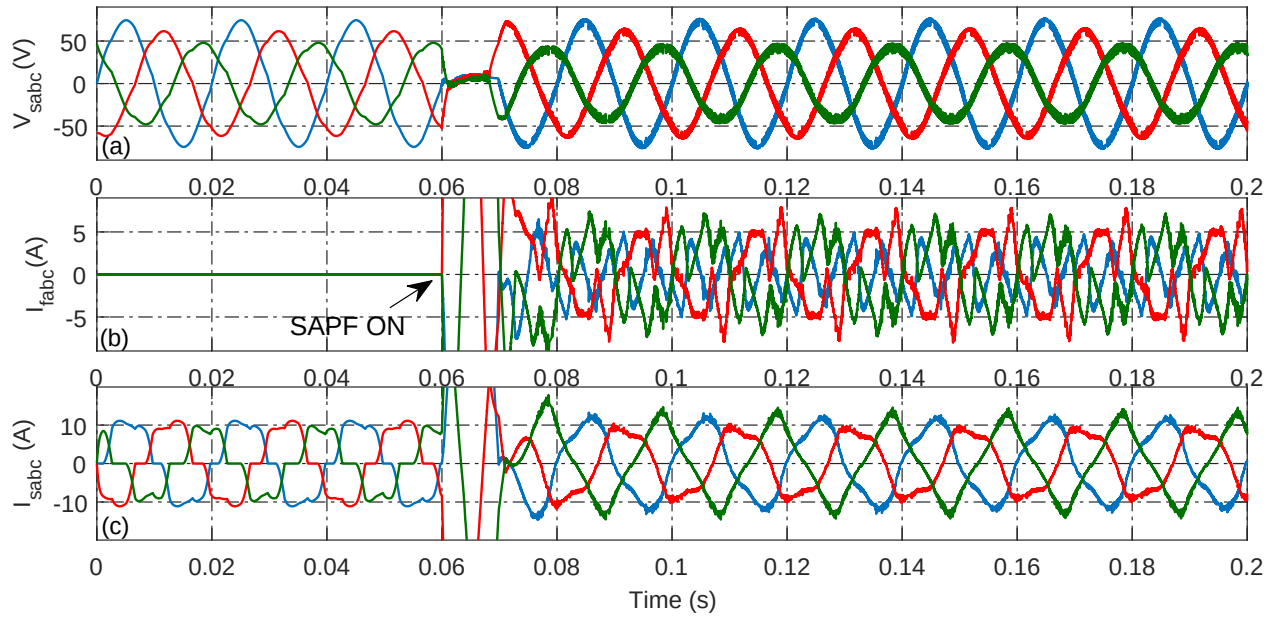


Figure II.19: Case d: a- grid voltages, b- injected currents, and c- source currents

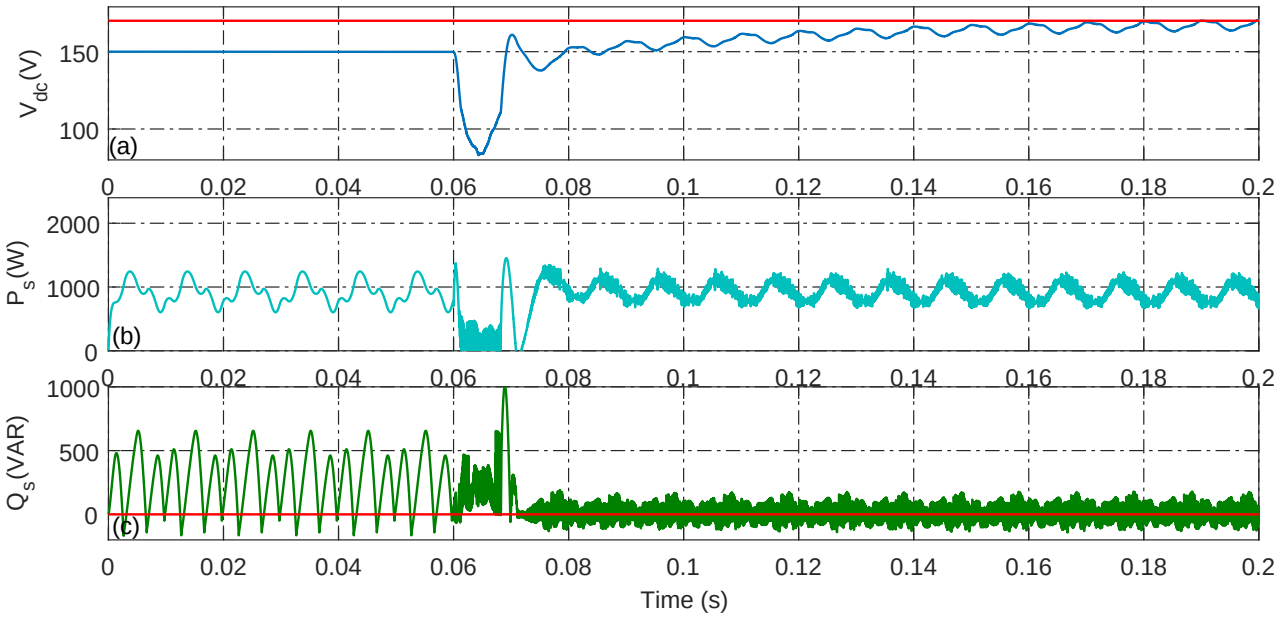


Figure II.20: Case d: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

II.3.1.3.2 SAPF based on SRF method

The circuit of shunt active power filter based on synchronous reference frame method for the harmonic currents estimation is illustrated in Figure (II.21)

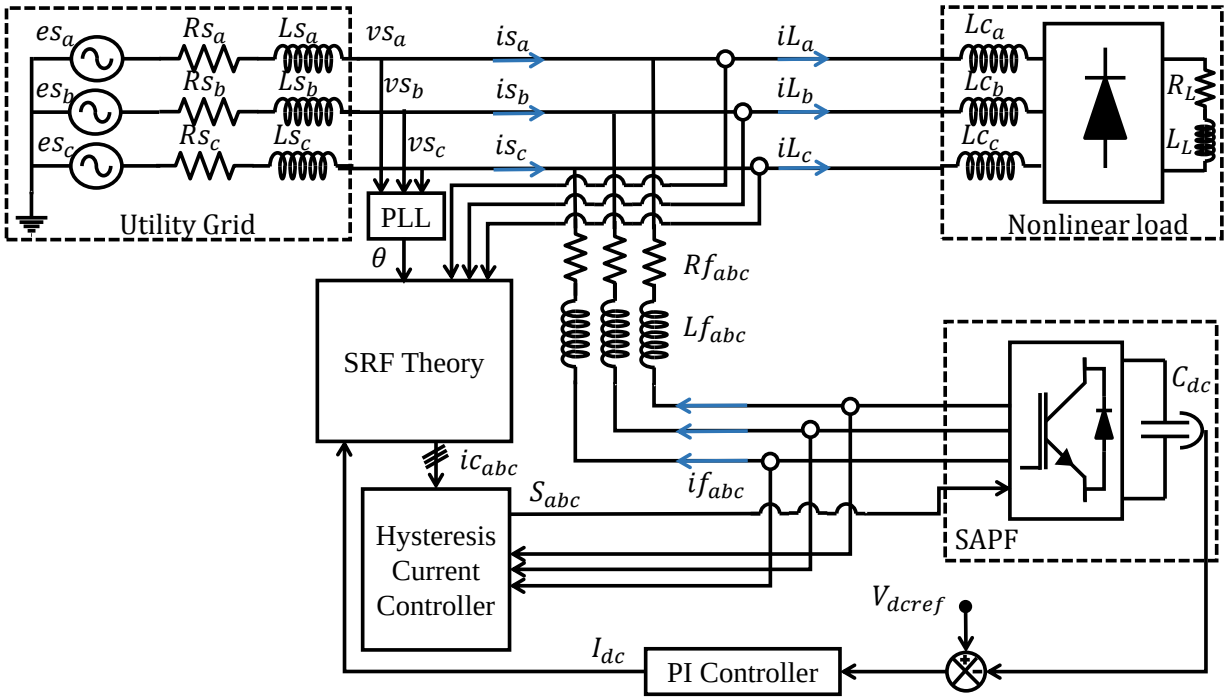


Figure II.21: Circuit diagram of SAPF based on SRF method

Nonlinear load:

Figure (II.22-a) shows the first phase current consumed by the nonlinear load which is rich in harmonics with THD of 22.5%. The injected current is null before the activation of the filter. At 0.06s the filter starts injecting the filtering currents as shown in Figure (II.22-b). Therefore, the harmonic components are suppressed and the source current becomes sinusoidal as shown in Figure (II.22-c) with THD of 1.85% as shown in Table (II.3). On the hand, the DC-link voltage is well regulated after a transient period of 0.01s, the oscillations of the instantaneous active power are minimized, and the reactive power is well compensated as shown in Figure (II.23).

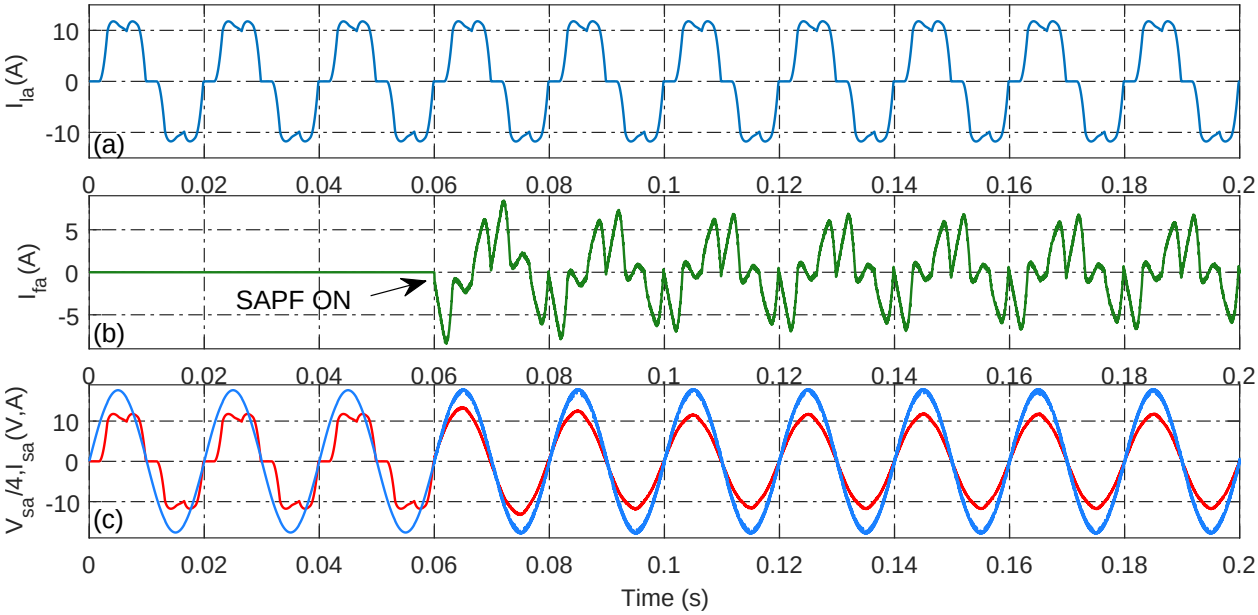


Figure II.22: Nonlinear load: a- load current, b- filter current, c- source current and voltage

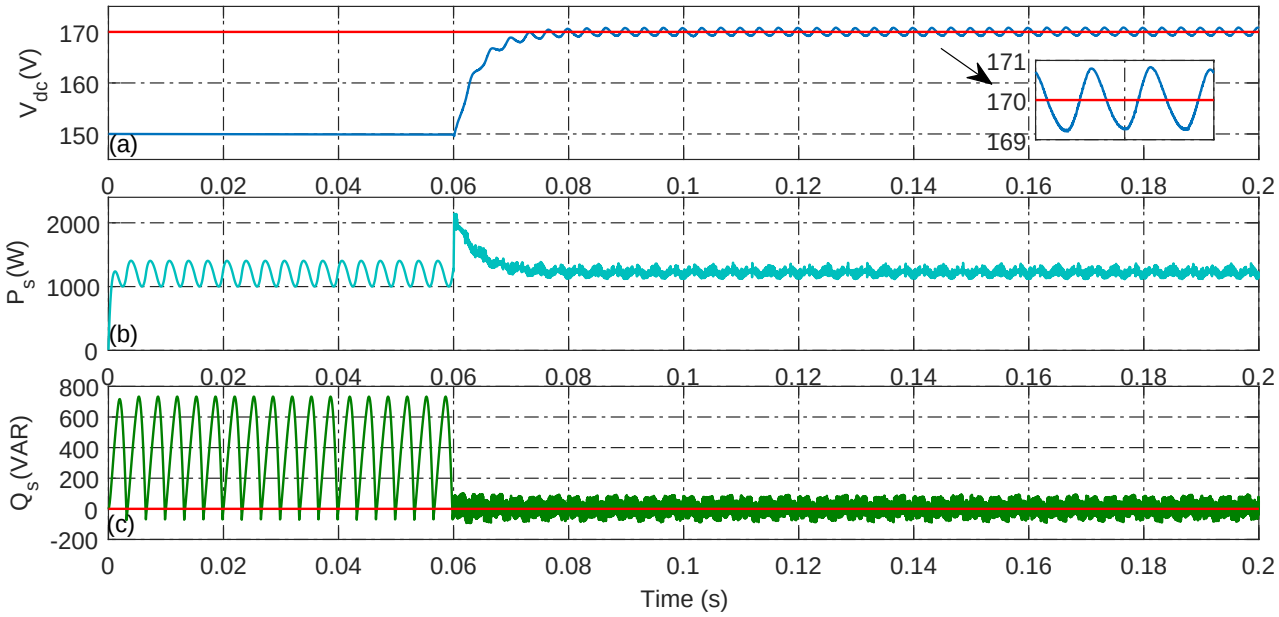


Figure II.23: Nonlinear load: a- DC-link voltage, b- instantaneous active power and c- instantaneous reactive power

Different grid conditions:

a- Balanced undistorted Source Voltage: In this case we apply a balanced undistorted utility grid voltages as shown in Figure (II.24-a). At 0.06 the filter is initialized which started injecting the filtering currents as presented in Figure (II.24-b).

The source current of the the first phase becomes quasi-sinusoidal and its THD has been reduced from 22.5% to 1.85% as demonstrated in Figure (II.24-c). On the other hand and same as in the previous estimation method the voltage across the DC-link follows the reference voltage after starting the filter at 0.06 as shown in Figure (II.25-a).

The oscillations of the instantaneous active power delivered by the utility grid are minimized in the steady state, and the reactive power is compensated as well as shown in Figure (II.25-b) and Figure (II.24-c) respectively.

b- Unbalanced undistorted Source voltage: As it can be seen in Figure (II.26-a), the three-phase voltages of the utility grid are unbalanced by +20% and -20% in the magnitude of the first phase and the third phase respectively. The filter injected the required currents with unequal magnitude to ensure both harmonics and current unbalances elimination of the source current as presented in Figure (II.26-b). Unlike the previous method, the SRF theory ensures higher source current THD reduction (between 2.44% and 3.46%) and unbalance suppression as demonstrated in Figure (II.26-c).

Harmonic	Mag %	Ang- Deg	Harmonic	Mag %	Ang- Deg
(DC) 0 Hz	0.01	90	(h11) 550 Hz	0.04	109.4
(Fnd) 50 Hz	100	0.0	(h12) 600 Hz	0.05	-72.5
(h2) 100 Hz	0.02	79.1	(h13) 650 Hz	0.12	240.2
(h3) 150 Hz	0.07	-21.9	(h14) 700 Hz	0.01	89.8
(h4) 200 Hz	0.3	-84.9	(h15) 750 Hz	0.04	-72.1
(h5) 250 Hz	0.8	-9.7	(h16) 800 Hz	0.04	176.1
(h6) 300 Hz	0.04	29.7	(h17) 850 Hz	0.07	227.9
(h7) 350 Hz	0.85	164.4	(h18) 900 Hz	0.03	44.6
(h8) 400 Hz	0.02	-22.3	(h19) 950 Hz	0.07	-62.9
(h9) 450 Hz	0.05	-60.3	(h20) 1000 Hz	0.02	-24.7
(h10) 500 Hz	0.02	169.7	THD of Is_a:		1.85%

Table II.3: THD of source current using SRF method

The DC-link voltage is regulated after a longer transient period compared to PQ theory but SRF theory ensures lower steady state oscillations as shown in Figure (II.27-a). Moreover, SRF theory ensures lower active power oscillations but the compensation of reactive power is deteriorated compared to PQ theory as shown in Figure (II.27-b) and (II.27-c).

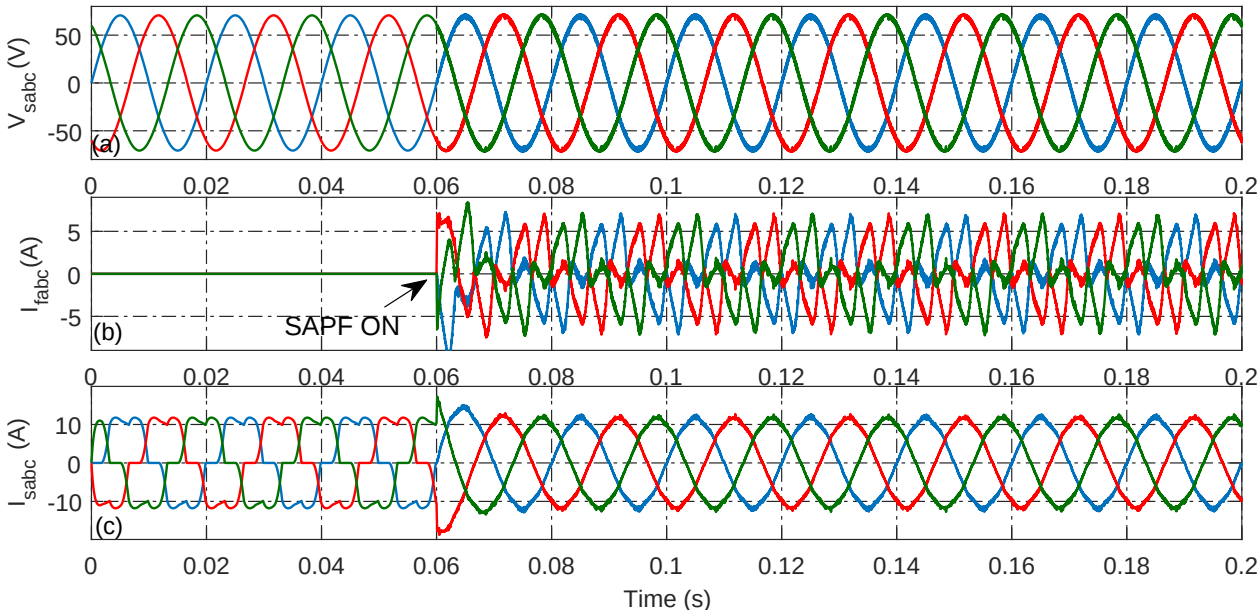


Figure II.24: Case a: a- Grid voltages, b- injected currents, and c- source currents

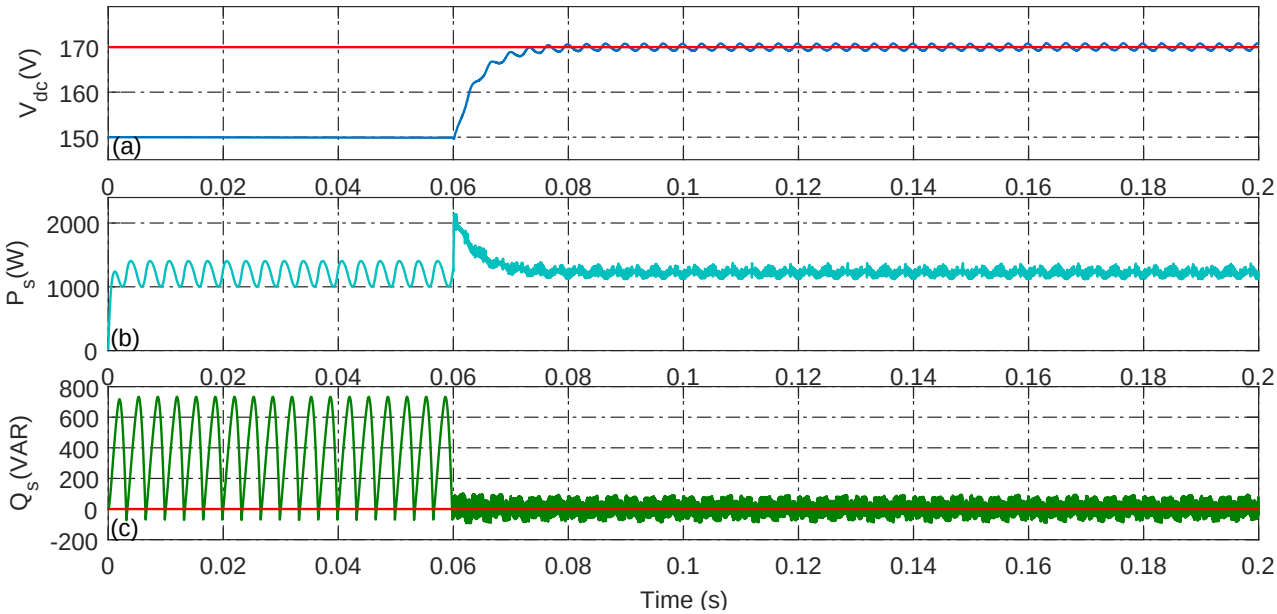


Figure II.25: Case a: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

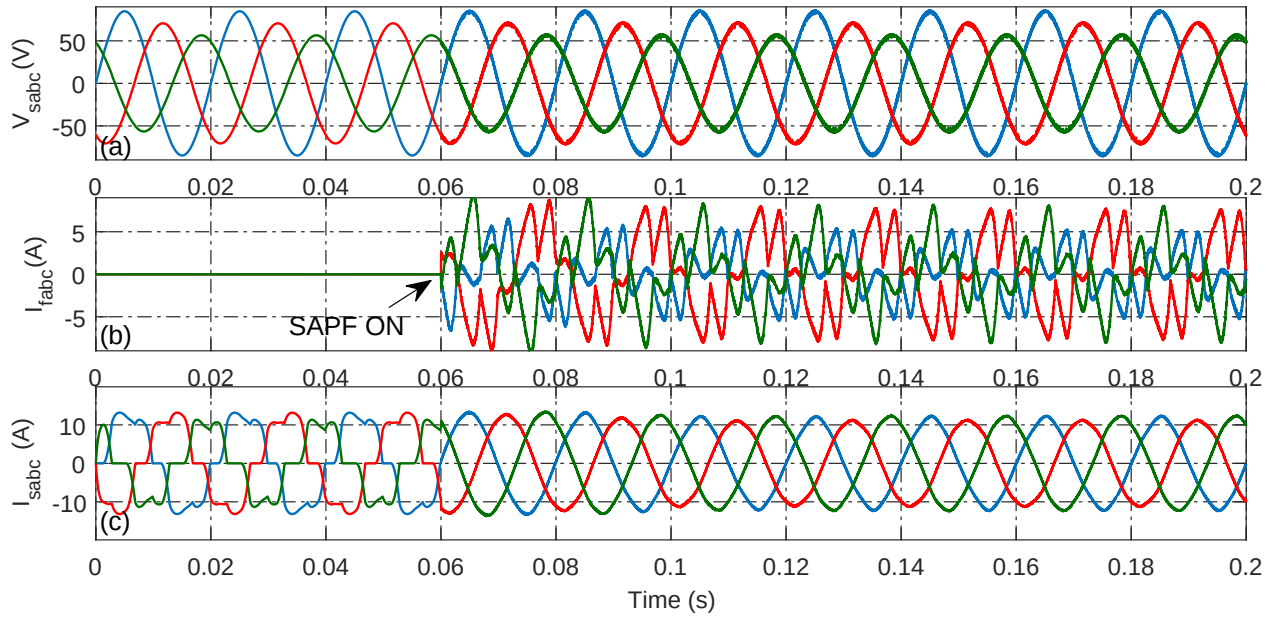


Figure II.26: Case b: a- Grid voltages, b- injected currents, and c- source currents

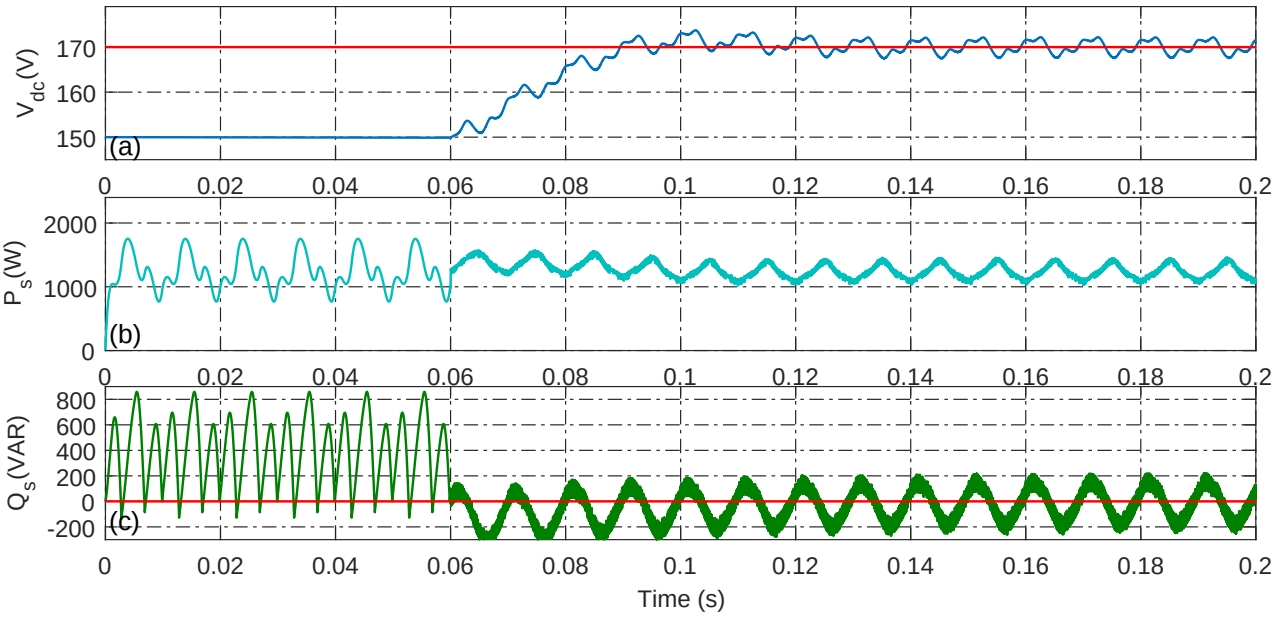


Figure II.27: Case b: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

c- Balanced distorted Source voltage: The SRF theory shows a good performance under utility grid with distorted voltages as shown in Figure (II.28-a). As it can be clearly seen in Figure (II.28-b), the harmonics are mitigated in the three-phase source currents and their THDs have been reduced ($is_a = 1.97\%$, $is_b = 1.95\%$, and $is_c = 1.91\%$)

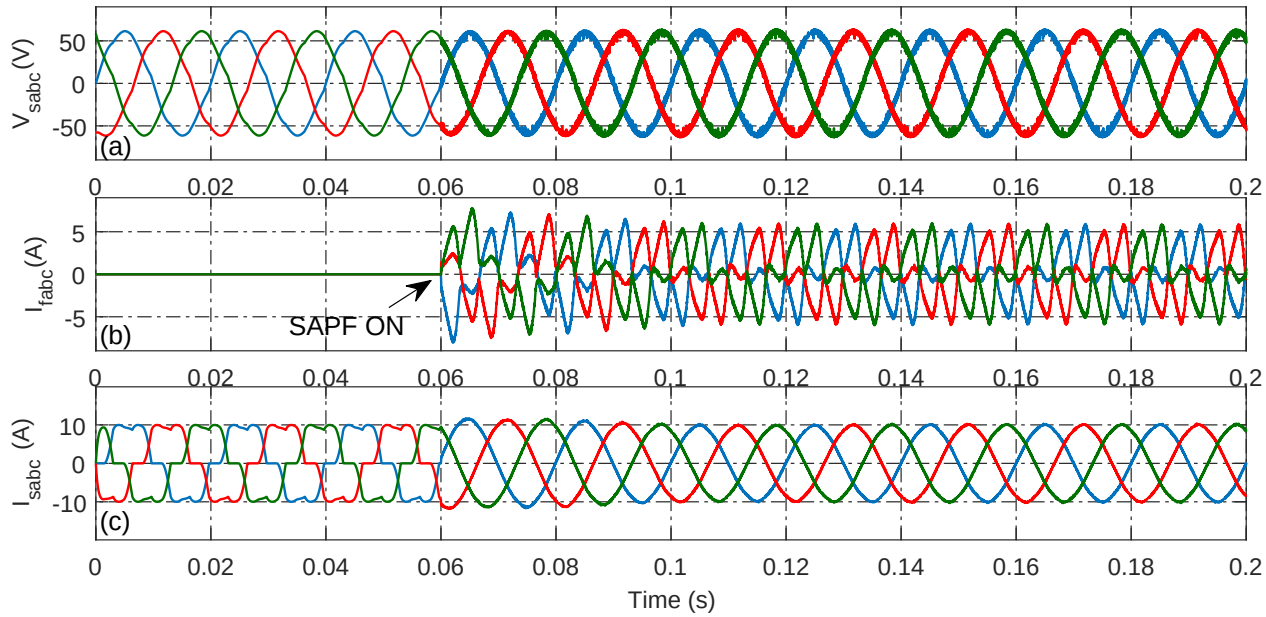


Figure II.28: Case c: a- Grid voltages, b- injected currents, and c- source currents

Moreover, the DC-link voltage is well regulated after a slightly longer transient period compared to PQ theory as illustrated in Figure (II.29-a). The instantaneous active power maintained stable and reactive power is well compensated as presented in Figure (II.29-b) and Figure (II.29-c) respectively.

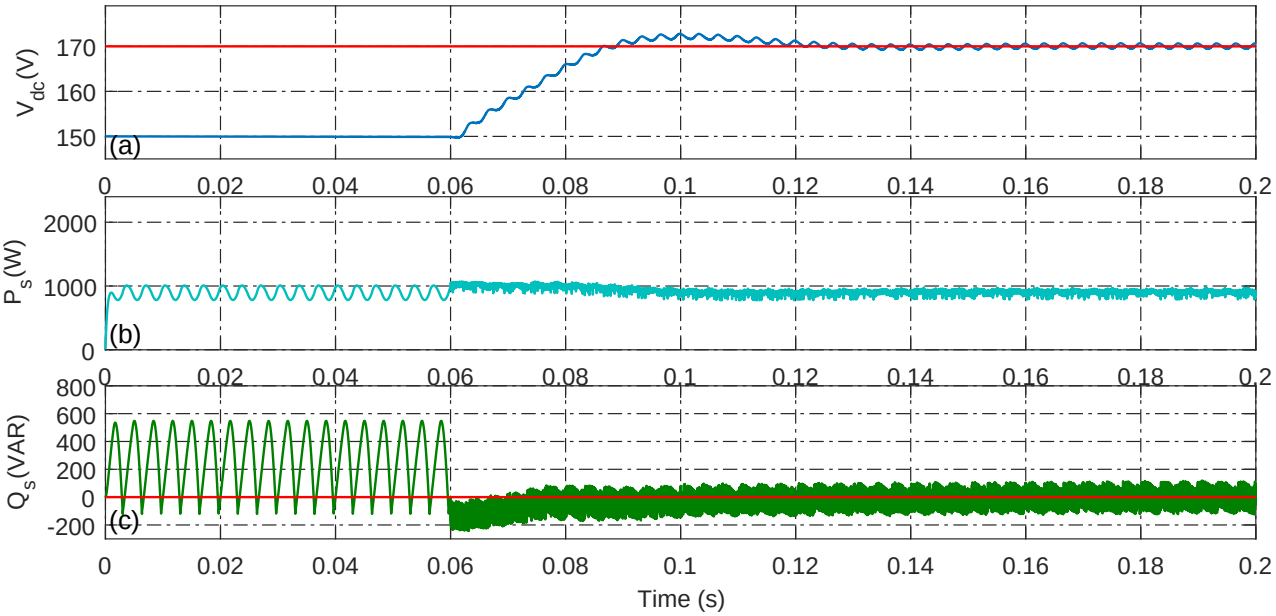


Figure II.29: Case c :a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

d- Unbalanced distorted Source voltage: SRF theory introduces a higher effectiveness of harmonics and unbalance elimination under unbalanced distorted utility grid voltages as shown in Figure (II.30-a). This can be seen in the resulting source currents with THDs below 5% ($is_a = 3.68\%$, $is_b = 3.56\%$, and $is_c = 2.77\%$) as shown in Figure (II.30-c). In Figure (II.31-a) the voltage of the DC-link maintained near to the reference value after a transient period of 0.03s with no significant drop and steady state error as in PQ theory. The instantaneous active power delivered to the nonlinear load remains stable as presented in Figure (II.31-b). Whereas, the reactive power is compensated with higher oscillations during the steady state compared to PQ theory as shown in Figure (II.31-c).

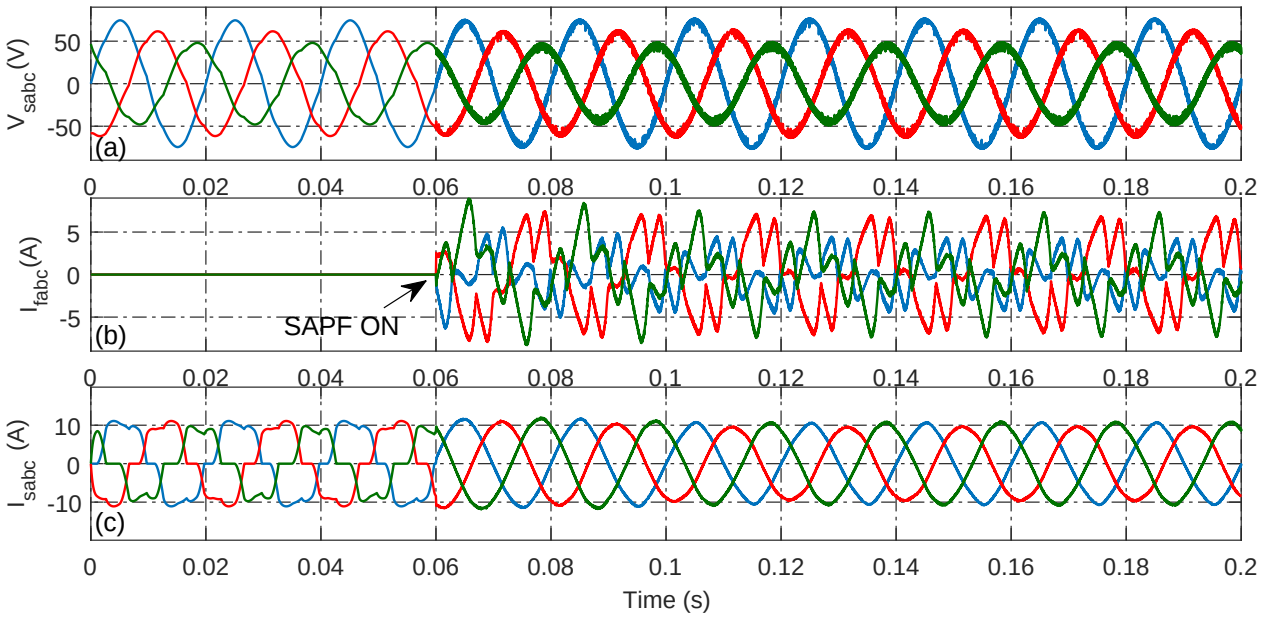


Figure II.30: Case d: a- Grid voltages, b- injected currents, and c- source currents

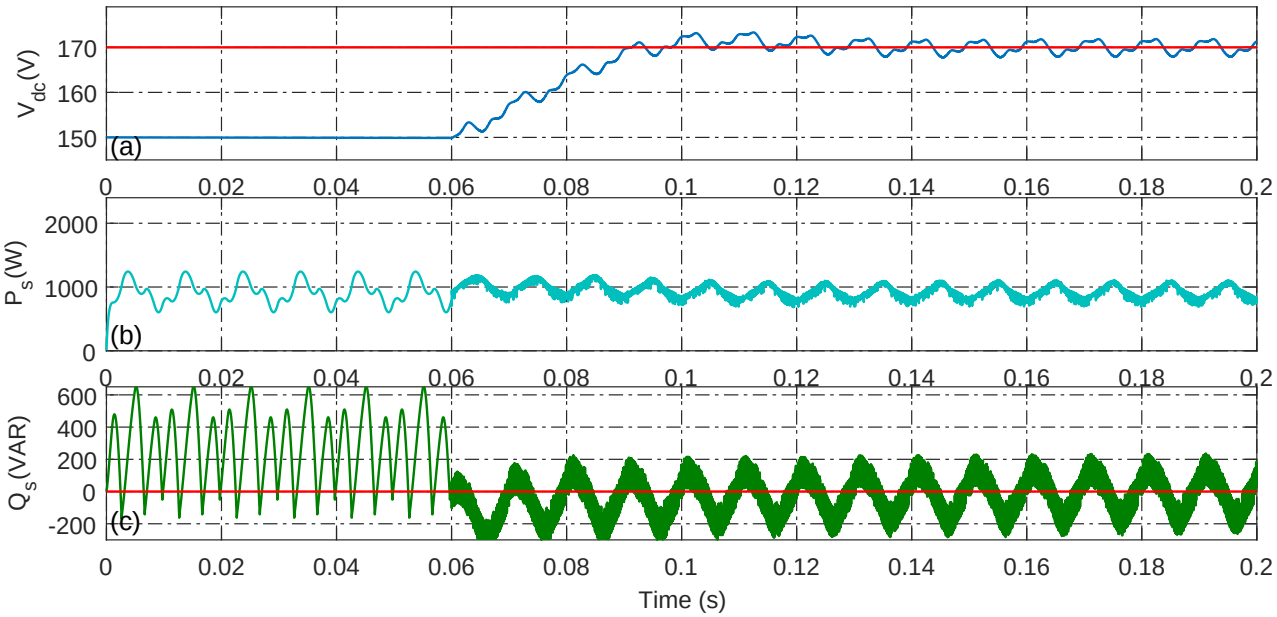


Figure II.31: Case d; a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

II.3.1.3.3 Evaluation of harmonic current estimators

Through the simulation results of SAPFs based on PQ theory and SRF method under different grid condition, SRF method provides better harmonics eliminations ($1.85\% < THD_{is} < 1.88\%$) under normal grid conditions compared to PQ theory which has lower performance ($3.28\% < THD_{is} < 3.64\%$).

Under unbalanced grid voltages, both SRF and PQ theory have been influenced. However, SAPF based on SRF still performing well and provides THDs less than 4%. On the other hand, the performance of SAPF based on PQ theory has been deteriorated and gives THDs above 12%.

In case of grid voltages distortion, SAPF based on SRF method gives lower source current THDs (under 2%) compared to the PQ theory (between 4% and 5%). Finally, under unbalanced distorted grid voltages the SAPF based on SRF method is still performing good and giving THDs within an acceptable range (under 4%), unlike in PQ theory which has a bad performance and gives a highly distorted source currents (above 14%).

In sum, through the results summarized in Table (II.4) and plotted in Figure (II.32), the SAPF based on SRF theory ensures a dominant performance against severe grid conditions compared to the system based on PQ theory.Thus, the SRF theory will be used for harmonic currents estimation.

Case	Control technique	Grid voltage (Vs)						Source current (Is)					
		Vsa		Vsb		Vsc		Isa		Isb		Isc	
		Peak (v)	THD (%)	Peak (v)	THD (%)	Peak (v)	THD (%)	Peak (A)	THD (%)	Peak (A)	THD (%)	Peak (A)	THD (%)
A	PQ	70.59	3.03	70.9	2.88	70.6	2.86	11.6	3.64	11.54	3.28	11.56	3.28
	SRF	70.6	2.80	70.6	2.91	70.59	2.82	11.51	1.85	11.51	1.88	11.51	1.86
B	PQ	84.71	2.74	70.6	2.81	56.46	3.68	12.36	12.88	10.79	15.96	12.15	13.21
	SRF	84.73	2.37	70.6	2.86	56.45	3.53	11.78	3.46	11.32	3.23	12.08	2.44
C	PQ	60.7	7.34	60.75	7.16	60.73	7.54	10.01	4.64	9.96	4.57	9.98	5.03
	SRF	60.78	6.90	60.78	7.22	60.78	6.96	9.92	1.97	9.93	1.95	9.92	1.91
D	PQ	73.8	6.32	61.69	7.42	45.97	10.64	11.8	14.55	9.0	18.4	10.67	15.47
	SRF	74.62	5.48	60.97	6.80	40.07	9.79	10.23	3.68	9.75	3.56	10.51	2.77

Table II.4: THDs and magnitudes of three-phase grid voltages and source currents

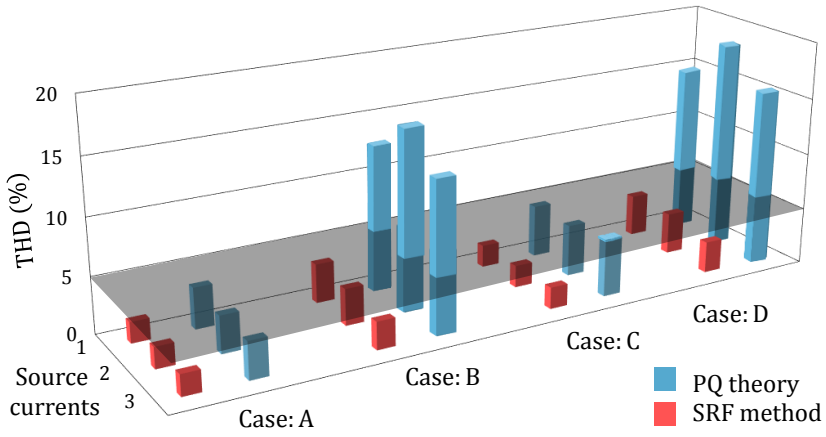


Figure II.32: THDs of three-phase source currents using PQ and SRF

II.3.2 Current control

II.3.2.1 Hysteresis current controller

The conventional hysteresis control is widely used due to its easy implementation and robustness. This strategy ensures satisfactory control of the current without needing the knowledge of the mathematical model of the system to be controlled or its parameters. This control technique based on establishing the error signal, the difference between the reference current ic_{abc} and the current produced by the voltage source inverter if_{abc}. This error is then compared to a hysteresis band in order to generate the control signals for the power switches. However, this control has a major disadvantage of the uncontrolled switching frequency of the power switches. Thus, the presence of a large amount of harmonics in the generated currents [17]. The control scheme of the hysteresis controller is illustrated in Figure (II.33).

II.3.2.2 PWM current control

The problem of the uncontrolled switching frequency introduced by hysteresis current controller can be solved by the PWM control technique by operating with a fixed frequency. This control technique is based on the reference voltage of the inverter generated by the comparison between the injected currents if_{abc} and the reference currents ic_{abc}. This reference voltages v_{fabc} are then compared with a high-frequency carrier signal [17]. Where, he output of the comparator provides the control signals for the switches.

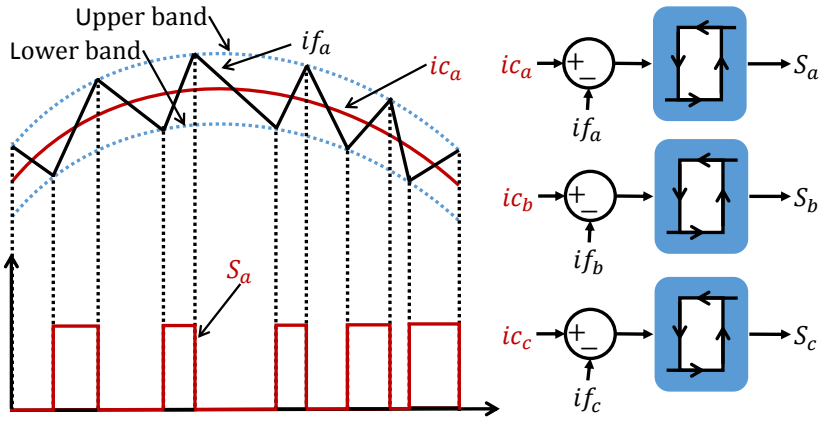


Figure II.33: Scheme of hysteresis current controller

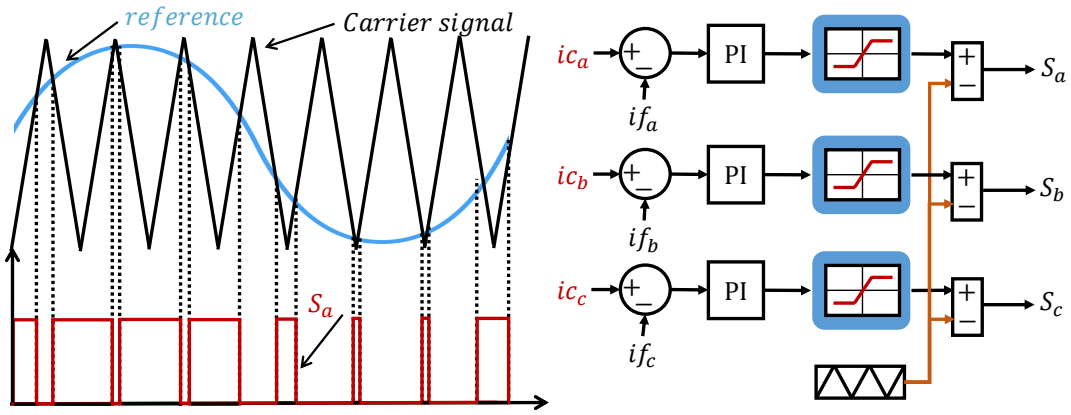


Figure II.34: Scheme of PWM current controller

Moreover, PI controllers are used in active power filters to track the reference compensating current generated by the identification control unit. The scheme of current controller based on PI regulator is illustrated in Figure (II.34).

The controller parameters can be calculated as follows:

$$K_{pi} = 2.\xi.\omega_{ci}.Lf - Rf \tag{II.55}$$

$$K_{ii} = Lf \cdot \omega_{ci}^2 \tag{II.56}$$

Where $\xi = 0.707$ and $\omega_{ci} = 2\pi.f_{ci}$, with f_{ci} is the cutoff frequency.

II.3.2.3 Backstepping current controller

Nonlinear backstepping control is a recursive operation based on the decomposition of a control system into lower sub-systems based on Lyapunov theory to ensure the stability of the entire control system [74, 75] . The control scheme of backstepping controller is shown in Figure (II.35).

The errors can be defined as:

$$e_1 = if_a - ic_a \tag{II.57}$$

$$e_2 = if_b - ic_b \tag{II.58}$$

$$e_3 = if_c - ic_c \tag{II.59}$$

Lyapunov functions are taken as follows:

$$V_1 = \frac{1}{2}e_1^2 \tag{II.60}$$

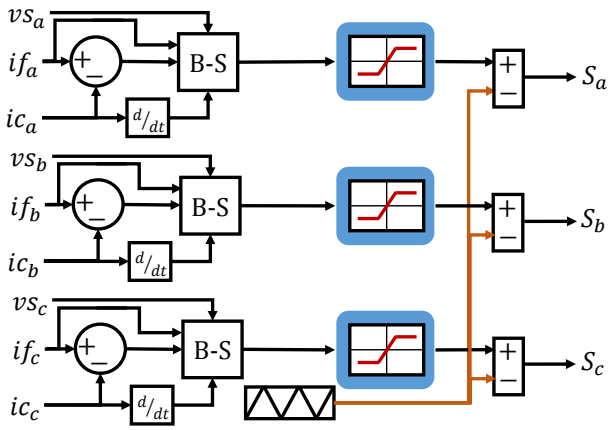


Figure II.35: Scheme of backstepping current controller

$$V_2 = \frac{1}{2}e_2^2 \tag{II.61}$$

$$V_3 = \frac{1}{2}e_3^2 \tag{II.62}$$

The derivatives of Lyapunov functions can be expressed by:

$$\dot{V}_1 = e_1\dot{e}_1 = e_1\left(\frac{1}{L_{fa}}\left(v_{fa} - vs_a - R_{fa}if_a\right) - \dot{i}_{ca}\right) \tag{II.63}$$

$$\dot{V}_2 = e_2\dot{e}_2 = e_2\left(\frac{1}{L_{fb}}\left(v_{fb} - vs_b - R_{fb}if_b\right) - \dot{i}_{cb}\right) \tag{II.64}$$

$$\dot{V}_3 = e_3\dot{e}_3 = e_3\left(\frac{1}{L_{fc}}\left(v_{fc} - vs_c - R_{fc}if_c\right) - \dot{i}_{cc}\right) \tag{II.65}$$

The reference output voltages can be obtained as:

$$v_{fa}^* = L_{fa}\left(\dot{i}_{ca} - k.e_1\right) + vs_a + R_{fa}if_a \tag{II.66}$$

$$v_{fb}^* = L_{fb}\left(\dot{i}_{cb} - k.e_2\right) + vs_b + R_{fb}if_b \tag{II.67}$$

$$v_{fc}^* = L_{fc}\left(\dot{i}_{cc} - k.e_3\right) + vs_c + R_{fc}if_c \tag{II.68}$$

Where, k is a positive constant.

II.3.2.4 Simulation results

In this section all the three discussed current controllers (hysteresis, PWM, and back-stepping current controllers) will be tested with the active power filter under nonlinear and dynamic load conditions. The three current controllers will be evaluated in terms of harmonic suppression and THD reduction of source current.

II.3.2.4.1 Hysteresis current controller

a- Nonlinear load: The overall scheme of SAPF based on hysteresis current controller is shown in Figure (II.36). The injected current controlled by the hysteresis controller of the first phase is pursuing accurately the reference compensating current generated by the SRF unit as presented in Figure (II.37-a). In Figure (II.37-b), it can be seen that the error between the reference and the injected current is less than $0.5A$. Therefore, harmonics are eliminated and the THD of the source current shown in Figure (II.37-c) is diminished from 22.5% to 1.85% as demonstrated in the THD spectrum illustrated in Figure (II.38) and table (B.1). The DC-link voltage is regulated after a transient period of 0.04s as shown in Figure (II.39-a). The oscillations of the instantaneous active power are minimized compared to the oscillations before the activation of the filter and reactive power is compensated as shown in Figure (II.39-b) and Figure (II.39-c) respectively.

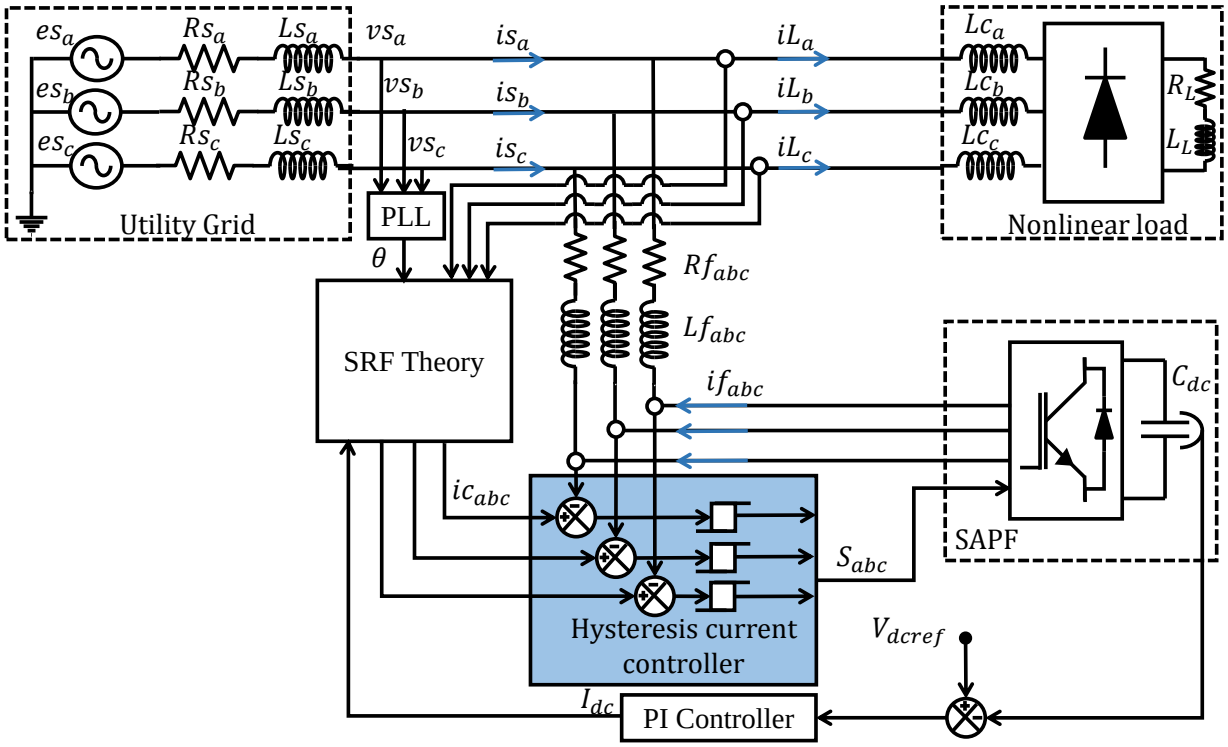


Figure II.36: Circuit diagram of SAPF based on hysteresis current controller

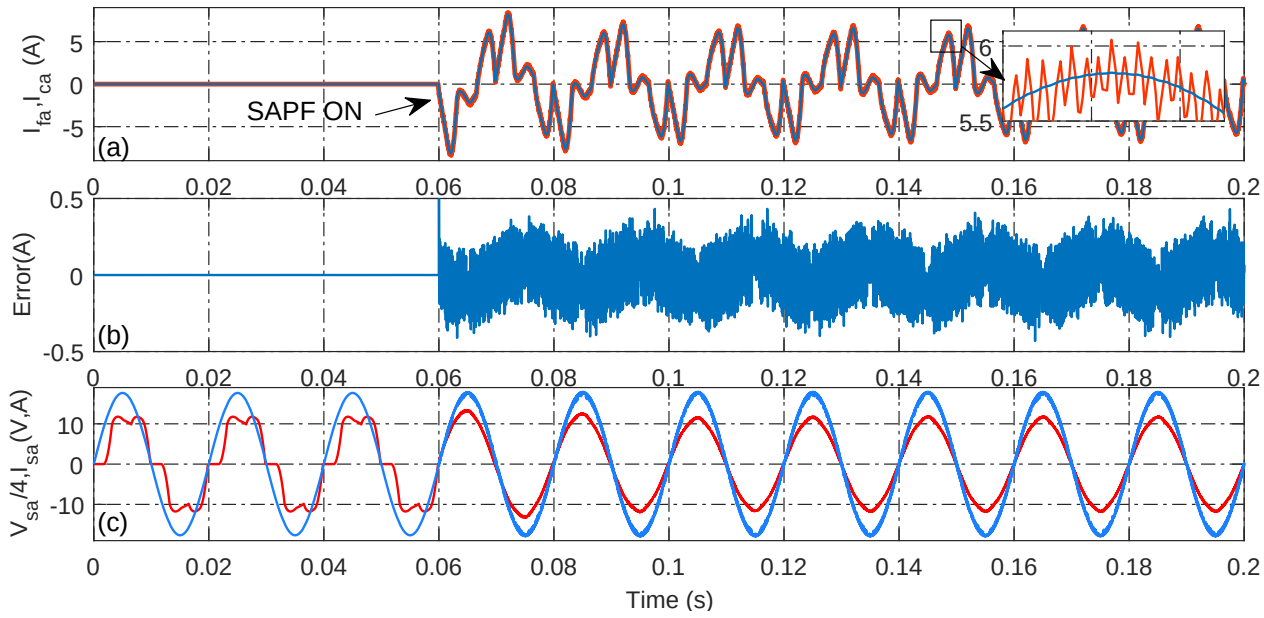


Figure II.37: Static load: a- injected current, b-tracking error, c-source current and voltage

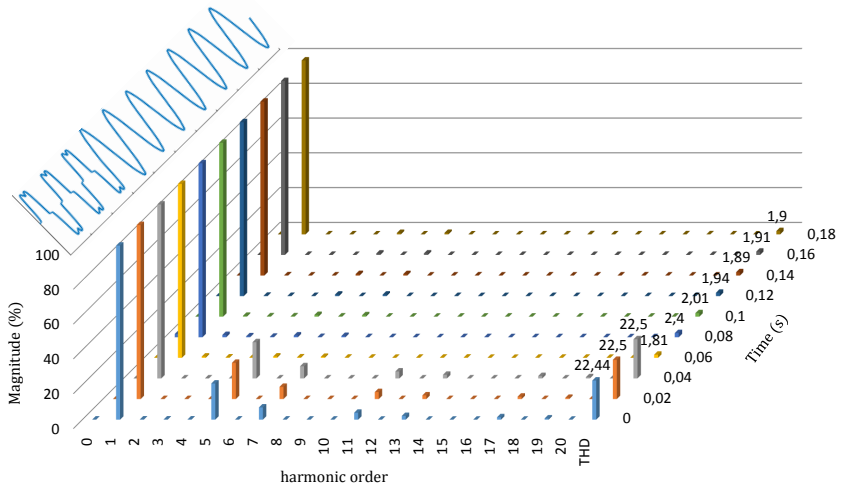


Figure II.38: THD of source current before and after the filtering

b- Dynamic load: In this test the performance of the filter based on hysteresis current controller has been tested under dynamic load conditions. This is done by applying a sudden load demand increase and decrease by 20%. In Figure (II.40-a) we can see that the source current has been increased accordingly during the period (0.3s-0.4s). The compensating currents have been increased correspondingly to fulfill the filtering under the new conditions as shown in Figure (II.40-b).

This can be seen in Figure (II.40-c), wherein the source current is kept quasi-sinusoidal and in phase with the source voltage despite the fast load variation.The voltage across the DC-link has encountered small deviations at the instants of load variation.

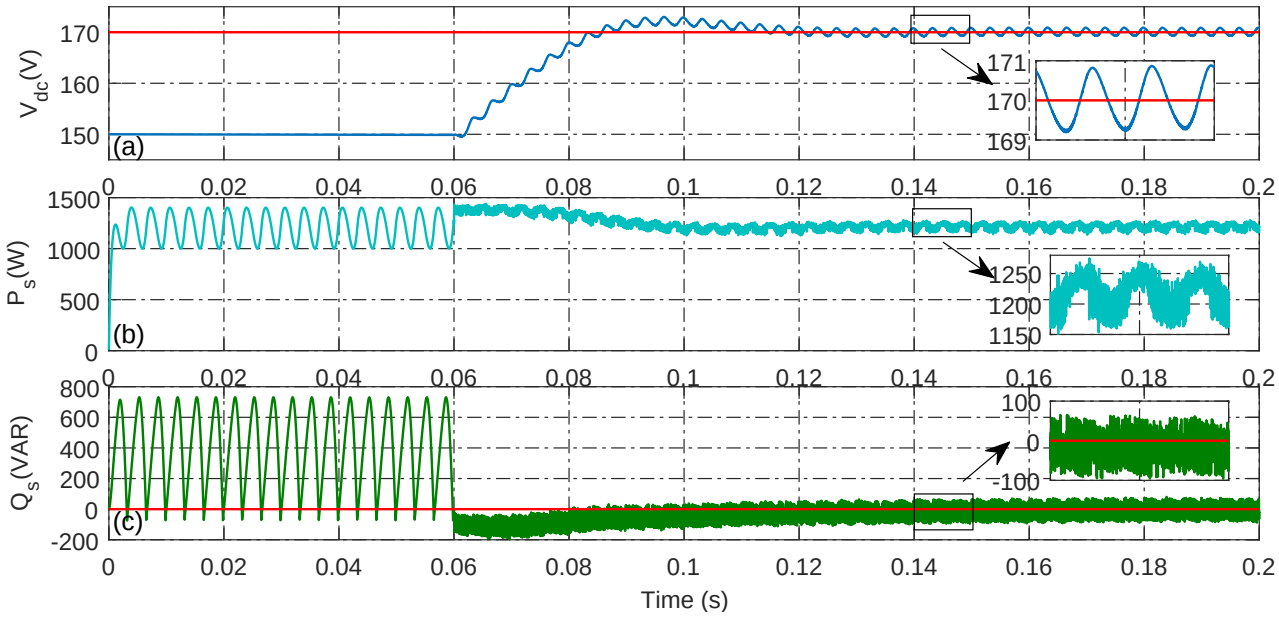


Figure II.39: Static load: a- DC-link voltage, b-instantaneous active power and c- instantaneous reactive power

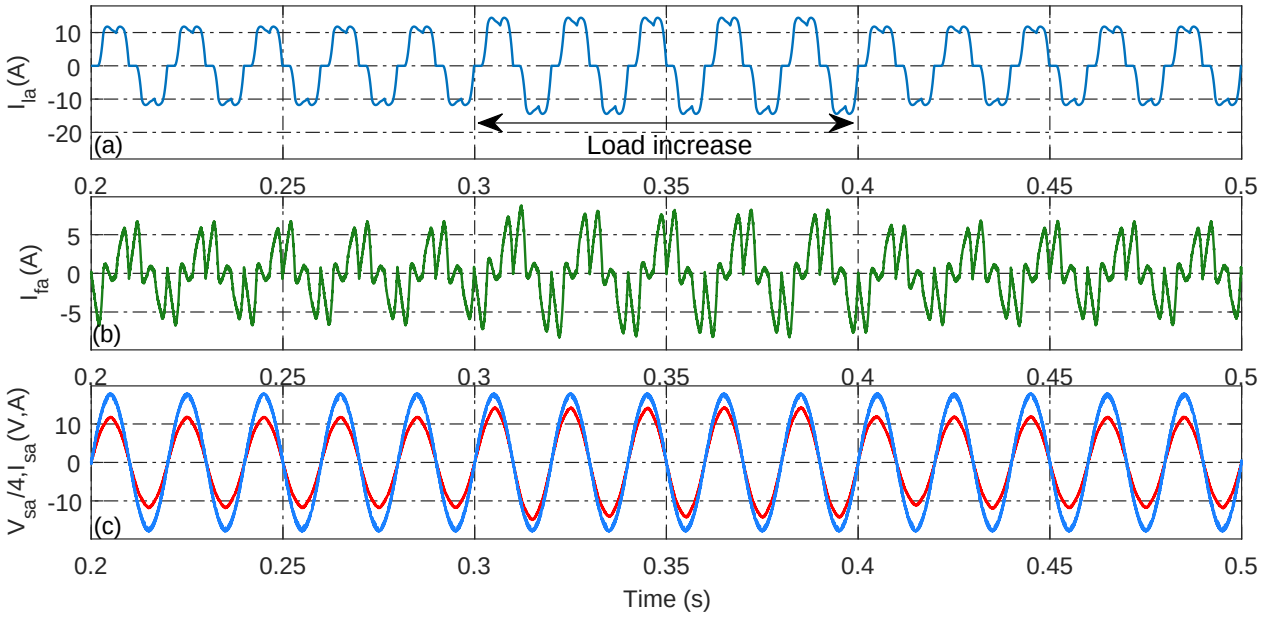


Figure II.40: Dynamic load: a- load current, b- injected current, c- source voltage and current

However, it has been regulated back after a transient period of 0.1s as demonstrated in Figure (II.41-a). The instantaneous active power of the main source has been increased to fulfill the new load requirement, whereas the reactive power is compensated as shown in Figure (II.41-b) and Figure (II.41-c) respectively.

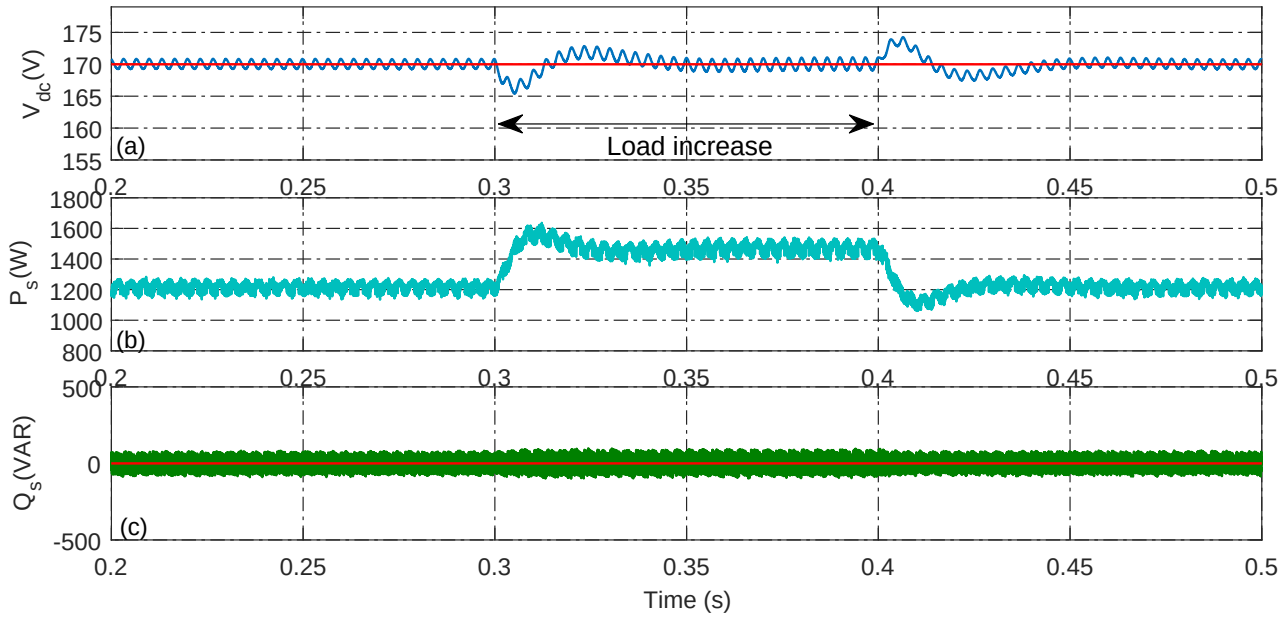


Figure II.41: Dynamic load: a- DC-link voltage, b- instantaneous active power and c- instantaneous reactive power

II.3.2.4.2 PWM current controller

a- Nonlinear load: The scheme of SAPF based on PWM current controller is illustrated in Figure (II.42). The error bandwidth between the reference compensation current and the injected current of the first phase using PWM current controller is inferior to the error of the hysteresis controller as shown in Figure (II.43-a) and Figure (II.43-b).This can be seen in the effectiveness of harmonics elimination from the source current shown in Figure (II.43-c) which has a better THD (1.79%) as illustrated in Figure (II.44) and table (B.2).

The DC-link voltage and the instantaneous active power of the main source are regulated after a transient period of $0.04s$ as shown in Figure (II.45-a) and Figure (II.45-b) respectively, and the reactive power is well compensated as in Figure (II.45-c).

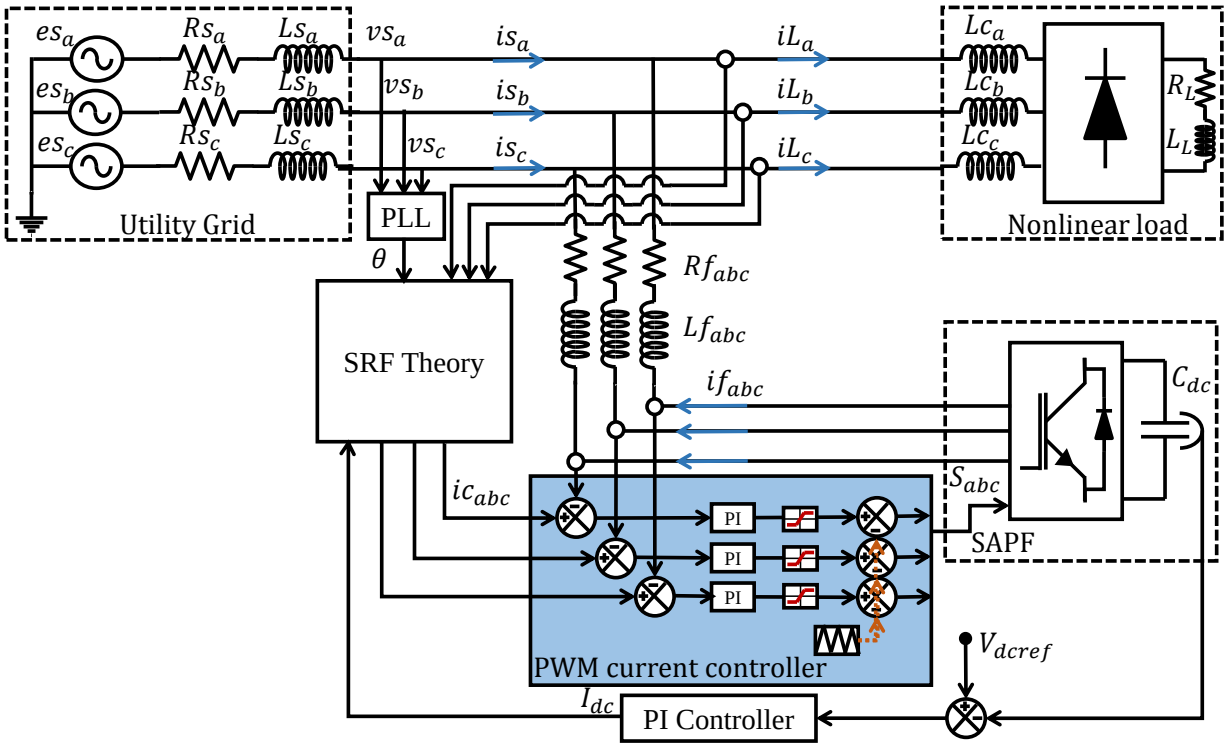


Figure II.42: Circuit diagram of SAPF based on PWM current controller

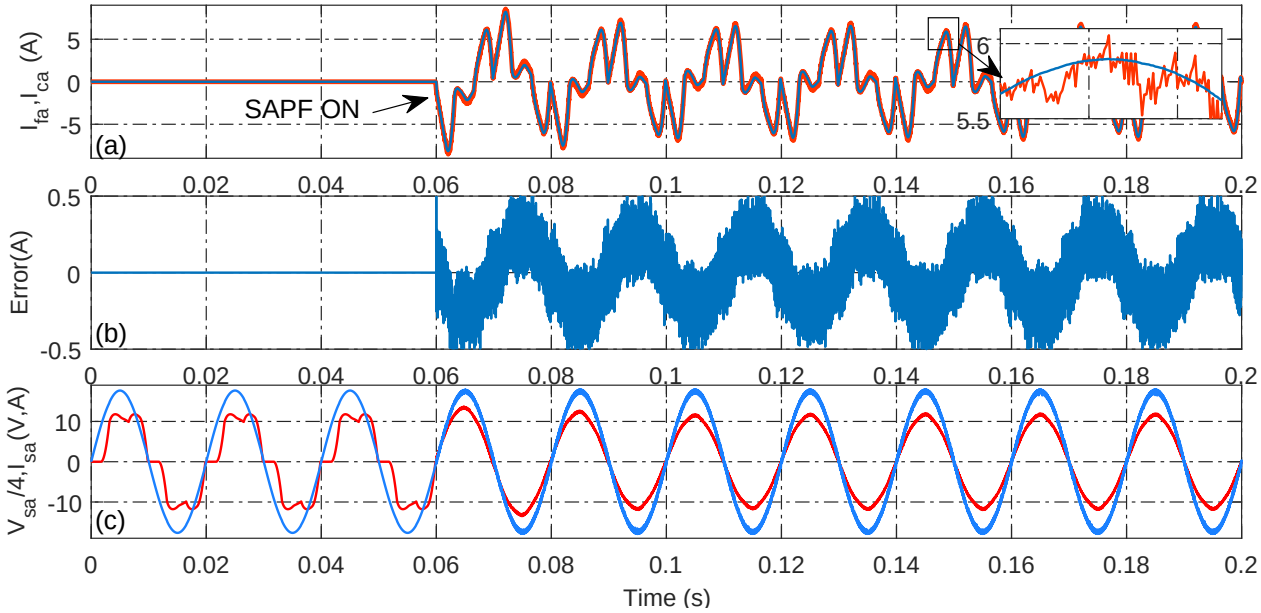


Figure II.43: Static load: a- injected current, b- tracking error, c- source voltage and current

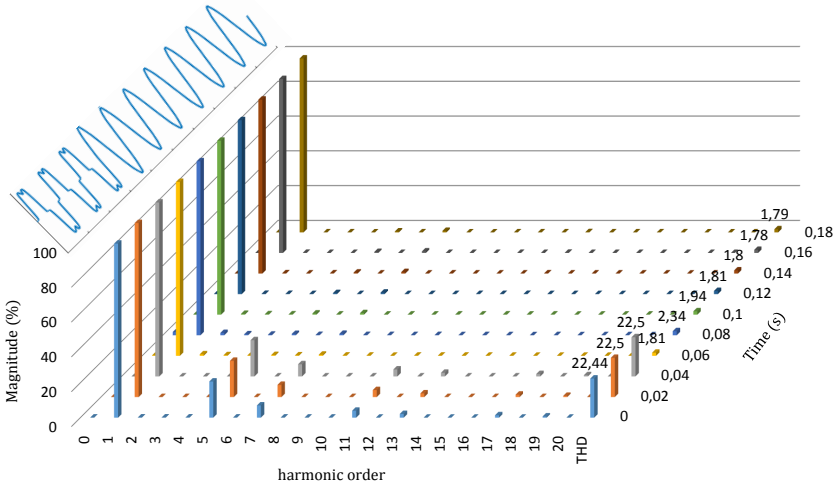


Figure II.44: THD of source current

b- Dynamic load: The load demand is increased by 20% during (0.3s-0.4s) as it is shown in Figure (II.46-a). It is clear in Figure (II.46-b) that the injected current have been increased accordingly to fulfil the new requirement to ensure the filtering operation. Therefore, the source current is decontaminated and the sudden load variation goes smooth with no overshoot as presented in Figure (II.46-c). Figure (II.47-a) illustrates the voltage across the DC-link which encountered small deviations at the instants of load variation. However, the voltage have been adjusted after a short transients of 0.02s. Moreover, the

instantaneous active power have been increased and decreased smoothly with no significant overshoots despite the quick variation and the reactive power maintained compensated as shown in Figure (II.47-b) and Figure (II.47-c) respectively.

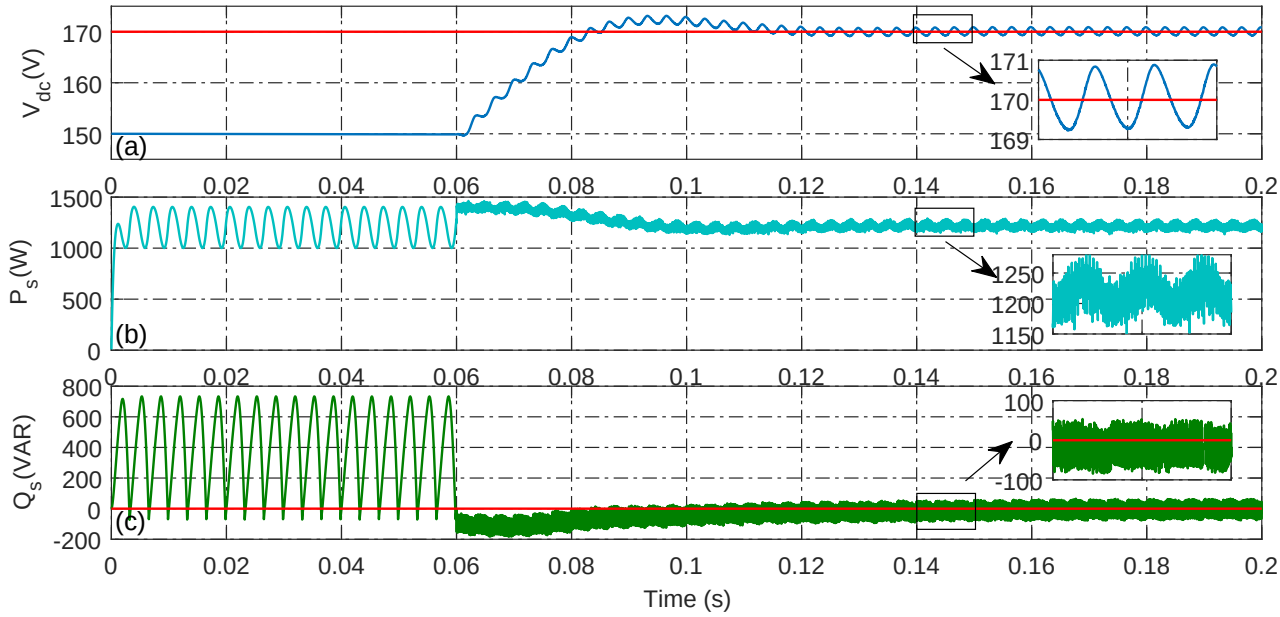


Figure II.45: Static load: a- DC-link voltage, b- instantaneous active power and c- instantaneous reactive power

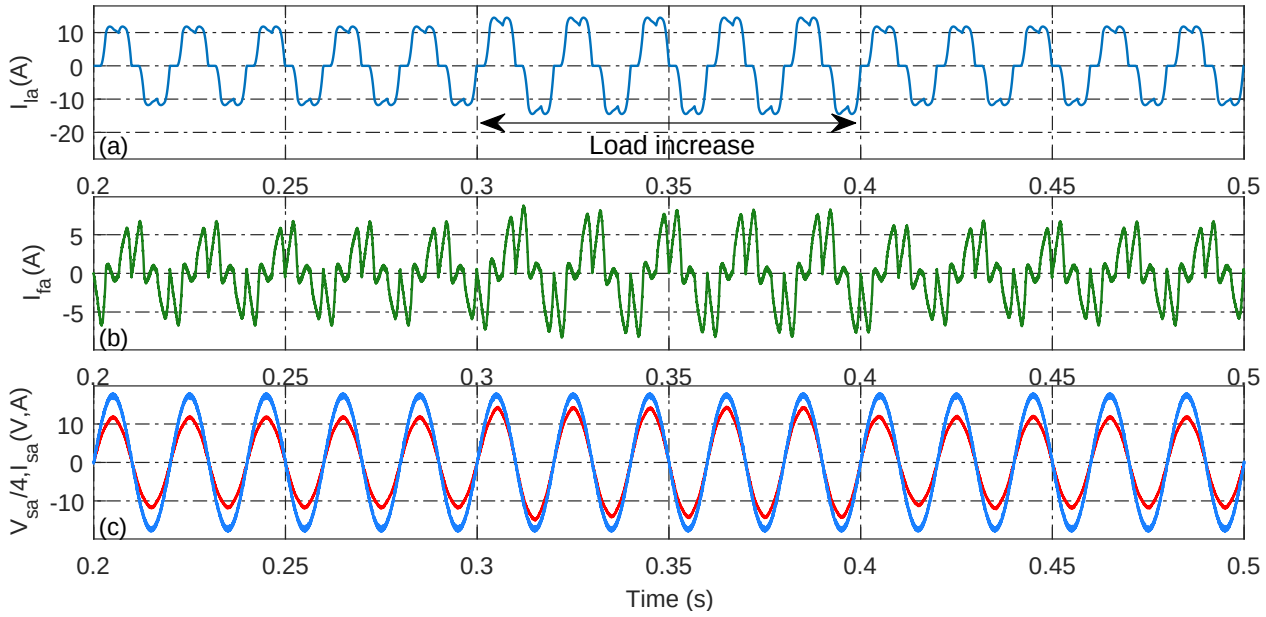


Figure II.46: Dynamic load: a- load current, b- injected current, c- source voltage and current

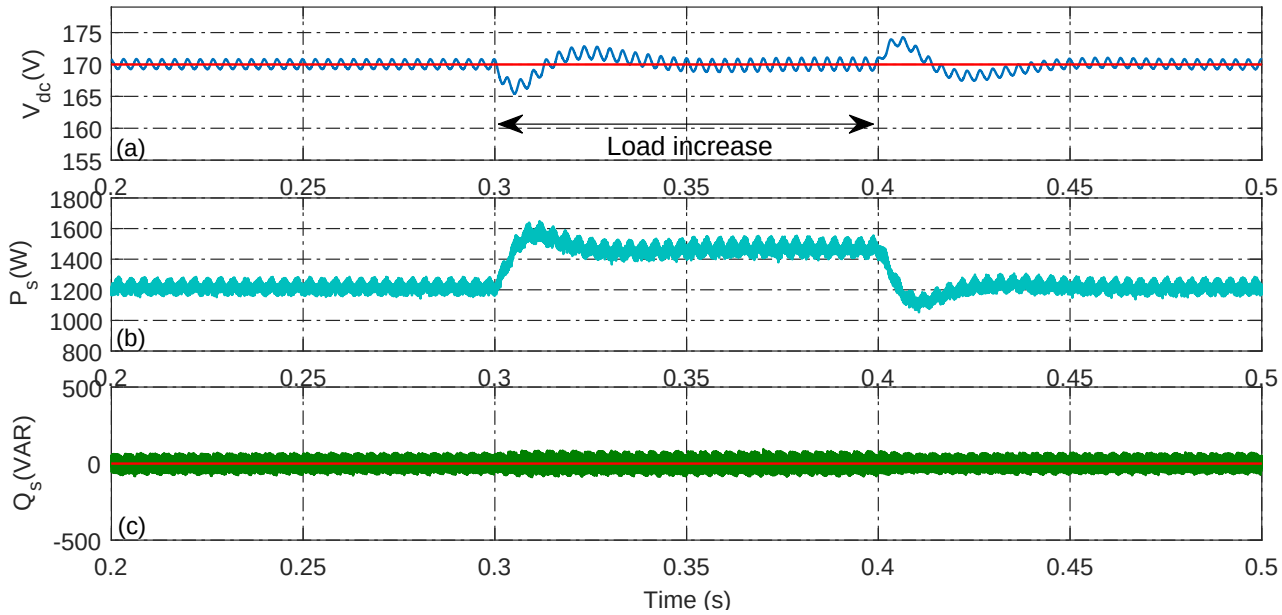


Figure II.47: Dynamic load: a- DC-link voltage, b- instantaneous active power and c- instantaneous reactive power

II.3.2.4.3 Backstepping current controller

a- Nonlinear load: The scheme of SAPF based on backstepping current controller is shown in Figure (II.48). As it can be seen in Figure (II.49-a), the backstepping current controller is giving a good current tracking as the error between the generated reference current and the injected current is less than $0.3A$ as shown in Figure (II.49-b).

Therefore the harmonics of the first phase source current illustrated in Figure (II.49-c) are well eliminated and its THD has been minimized from 22.5% to 1.6% as shown in Figure (II.50) and table (B.3). As in the previous controllers, the DC-link voltage is regulated , the oscillations of the instantaneous active power are minimized, and the reactive power is compensated as shown in Figure (II.51).

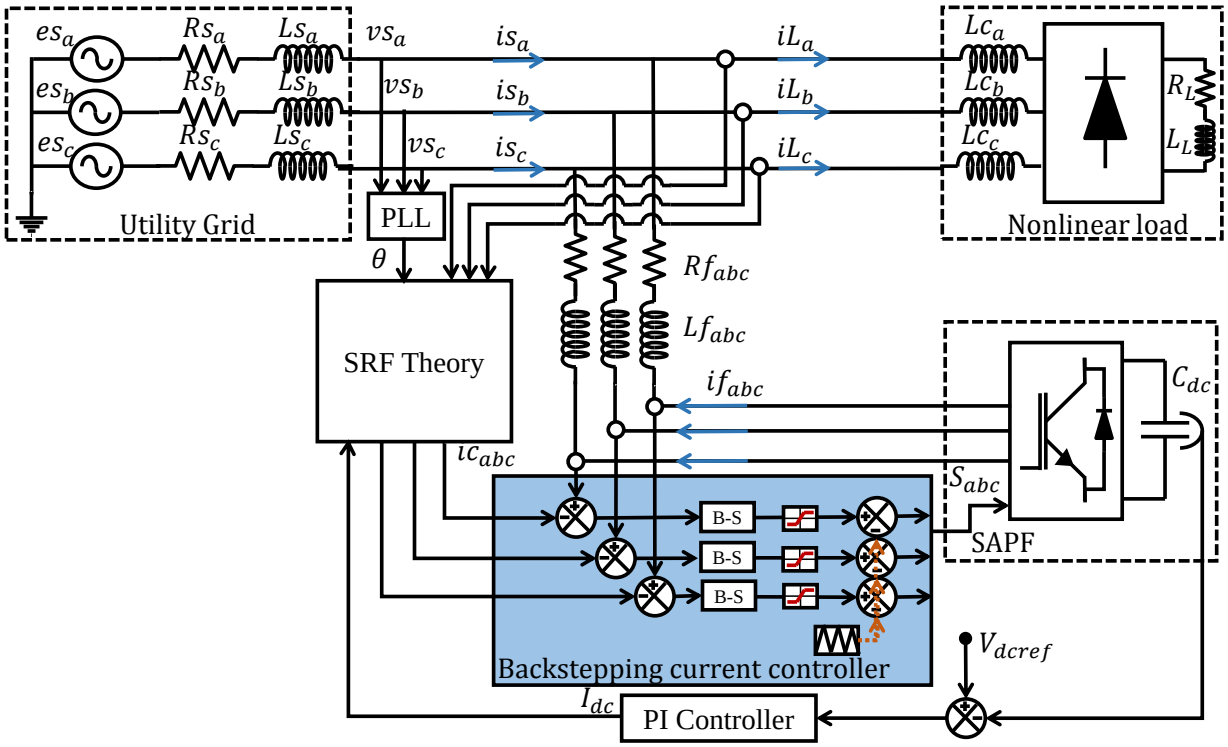


Figure II.48: Circuit diagram of SAPF based on backstepping current controller

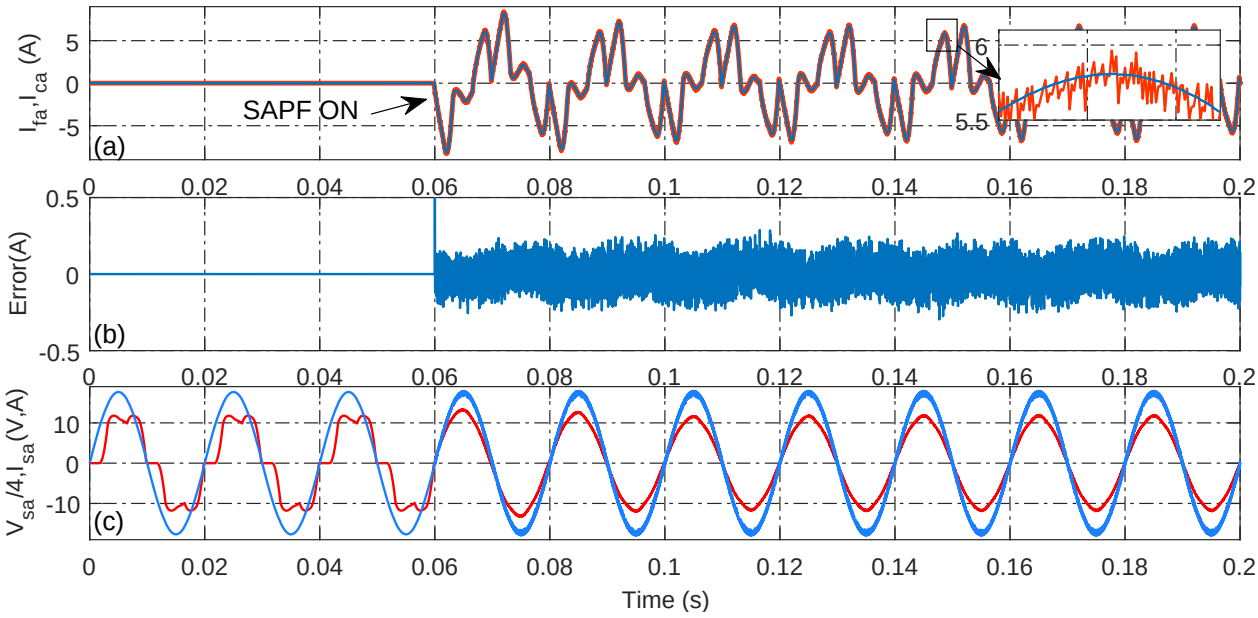


Figure II.49: Static load: a- injected current, b- tracking error, c- source voltage and current

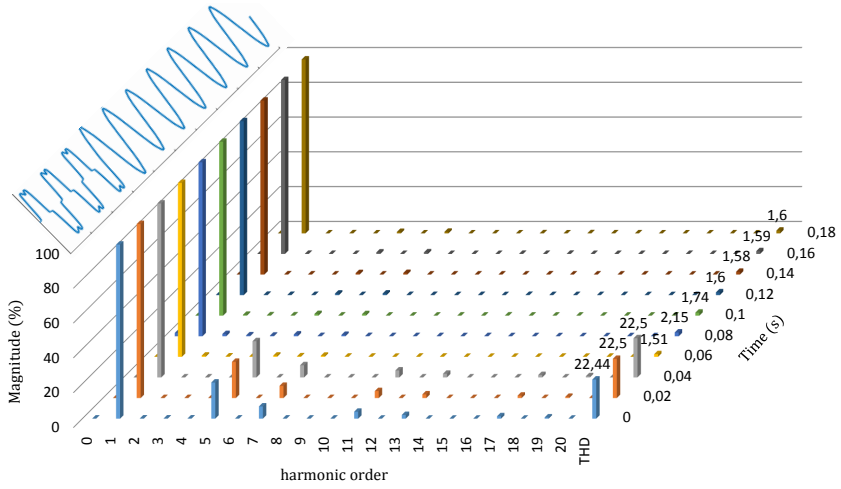


Figure II.50: THD of source current before and after the filtering

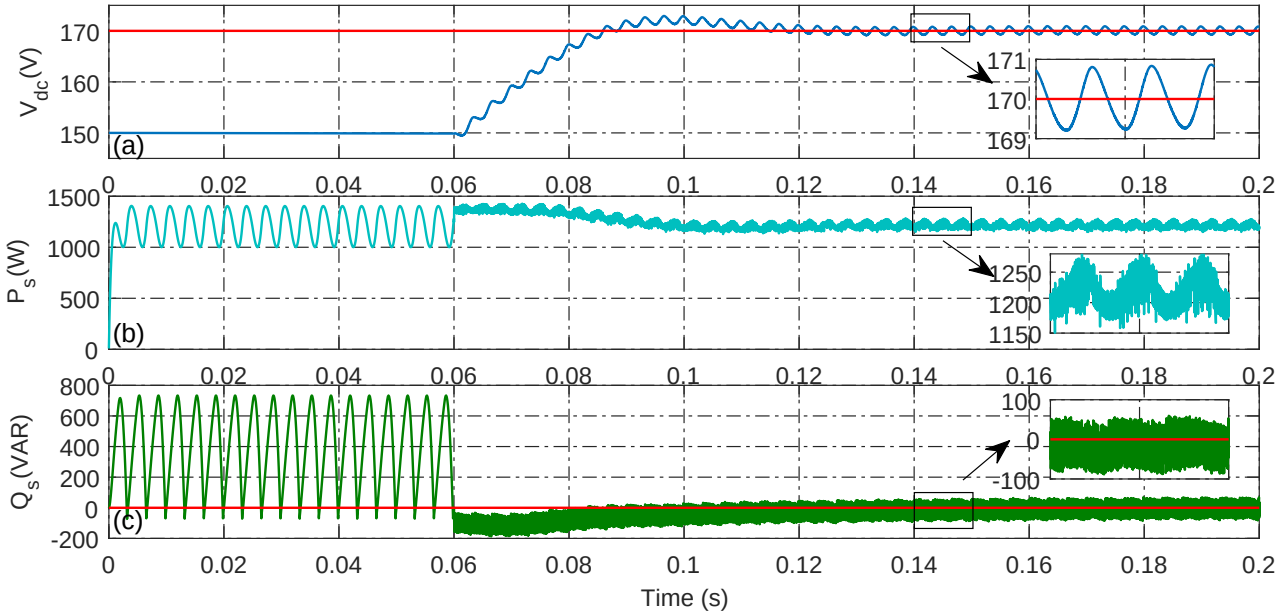


Figure II.51: Static load: a- DC-link voltage, b- instantaneous active power and c- instantaneous reactive power

b- Dynamic load: The active power filter based on backstepping current controller is tested under quick load variation as well as shown in Figure (II.52-a). The injected current is increased accordingly to maintain harmonic suppression as illustrated in Figure (II.52-b). In Figure (II.52-c), the source current is eventually kept decontaminated. The voltage across the DC-link has encountered small drop and raise at 0.3s and 0.4s to compensate the the active power demand required for the nonlinear load as illustrated in Figure (II.53-a).

The instantaneous active power has increased and decreased smoothly, whereas the reactive power is well compensated as shown in Figure (II.53-b) and Figure (II.53-c) respectively.

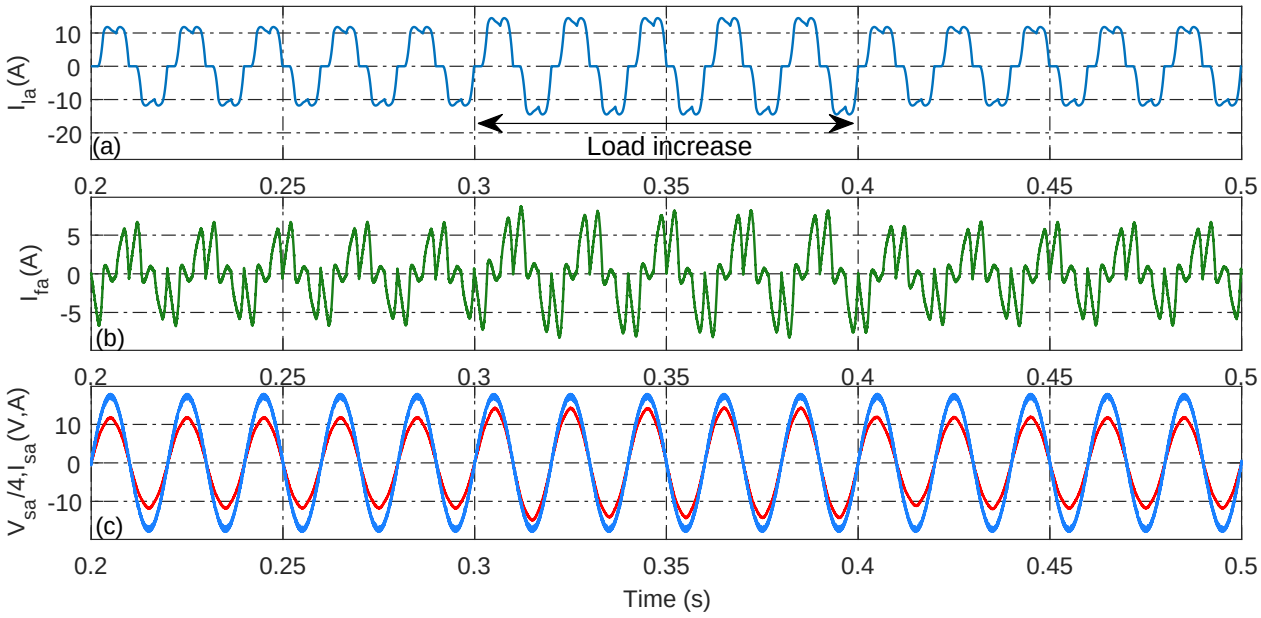


Figure II.52: Dynamic load: a- load current, b- injected current, c- source voltage and current

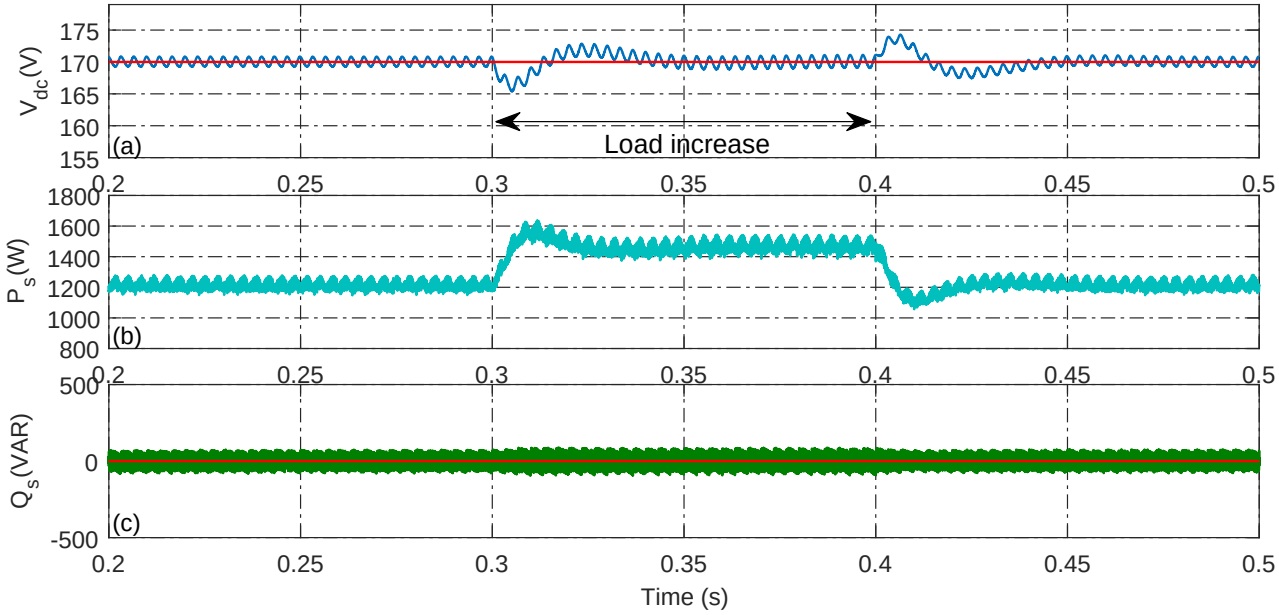


Figure II.53: Dynamic load: a- DC-link voltage, b- instantaneous active power and c- instantaneous reactive power

II.3.2.4.4 Evaluation of Current controllers

To choose the suitable current controller for the proposed system, an evaluation is carried out in terms of THD level of source current under nonlinear load and dynamic load conditions of hysteresis, PWM, and backstepping current controllers. For static nonlinear load the backstepping current controller gives higher harmonic elimination and thus a lower source current THD compared to PWM and hysteresis current controller as shown in Figure (II.54). Likewise, in case of applying a sudden load increase, backstepping current controller provides better source current THD during the entire load profile as illustrated in Figure (II.55). Therefore, the backstepping current controller will be used in the proposed shunt active power filter.

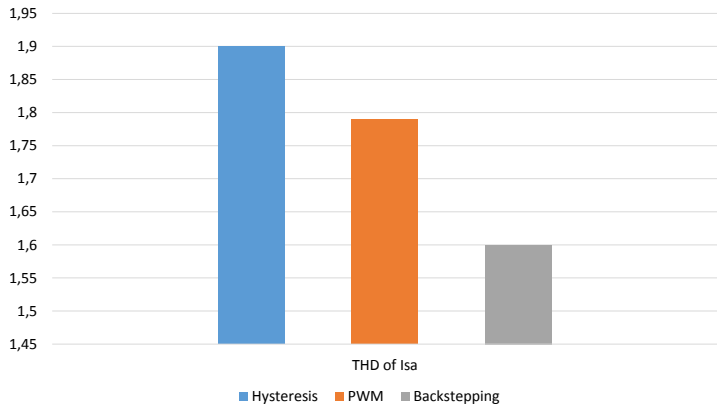


Figure II.54: THDs of hysteresis, PWM, backstepping current controllers for static nonlinear load

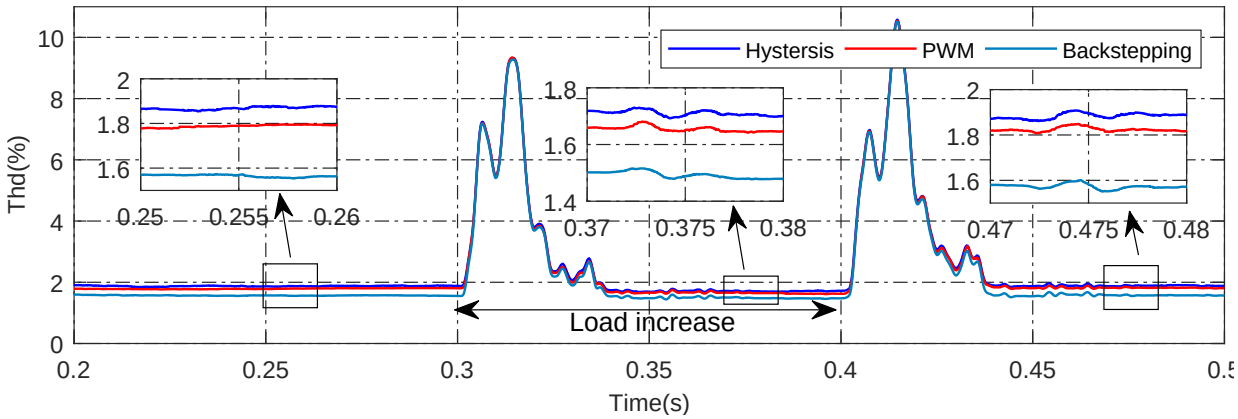


Figure II.55: THD profile of hysteresis, PWM, backstepping current controllers under dynamic load

II.4 Conclusion

In this chapter we have performed an overall evaluation of two harmonic identification techniques (PQ theory and SRF method) and three current controllers (hysteresis, PWM, and backstepping). In the first part we run the systems based on PQ and SRF theories under healthy and severe grid voltages which have been unbalanced and distorted. Secondly, we test the systems based on the mentioned current controller under static nonlinear load and under sudden load variation.

SAPFs based on the presented controllers are evaluated in terms of their efficiency in harmonic mitigation under the mentioned scenarios. Finally, through the presented simulation results, the SRF method will be used for harmonic current estimation and backstepping current controller for injected current control in the proposed configuration.

Chapter III

Photovoltaic system: two stage and single stage configurations

III.1 Introduction

This chapter is devoted to the second part of the proposed filter connected to the PV system. It presents the mathematical modelling of the different part in the PV system including the PV array, the conventional system based on two-stage configuration, and the proposed system based single-stage configuration. The conventional topology is based on the combination of DC-DC boost converter which tracks the maximum power and voltage source inverter which injects the compensating currents.

Whereas, in the proposed single-stage configuration, the impedance source inverters (Z-source inverter and Quasi Z-source inverter) perform the both tasks with one converter.

The last part of this chapter is dedicated to the presentation and application of different shoot through control approaches and MPP tracker.

III.2 Photovoltaic source

III.2.1 Photovoltaic cell

PV arrays are essentially composed of solar cells, which are able to generate electricity from solar irradiance. They can be combined in series and parallel depending on the desired level of current and voltage. Figure (III.1) shows the equivalent circuit of a single-diode photovoltaic (PV) cell [76]. By applying Kirchhoff's current law, the photo-current generated by a PV source can be expressed as follows::

$$I_{ph} = I_d + I_p + I_{pv} \tag{III.1}$$

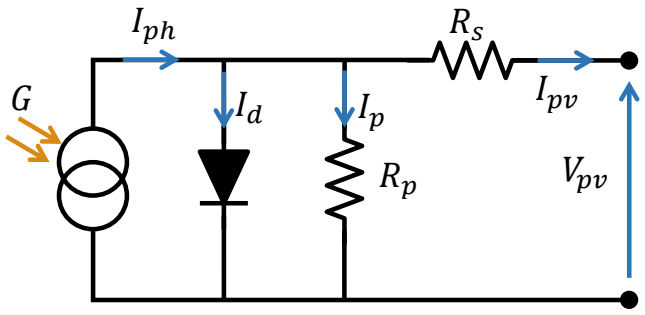


Figure III.1: PV cell equivalent circuit

Where I_{ph},I_d, I_p, and I_{pv} are the photo-current, diode current, the leaking current passing through the parallel resistor and the output current of a PV cell. The photo-current and the diode current are expressed by equations (III.2) and (III.3), respectively:

$$I_{ph} = \left(\frac{G}{G_{ref}}\right) \cdot (I_{ph,ref} + u_{sc} \cdot \Delta T) \tag{III.2}$$

Where $G_{ref} = 1000W/m2$ is the irradiance at the standard test condition (STC),G is the irradiance $(W/m2)$,$I_{ph,ref}$ is the photo current at STC, u_{sc} is the short-circuit temperature coefficient (A/K) and ΔT is the difference between the actual temperature T_C and the reference temperature $T_{Cref} = 298.15K$.

$$I_d = I_0 \cdot \left[\exp\left(\frac{V_{pv} + R_S \cdot I_{pv}}{A \cdot N_S \cdot V_T}\right) - 1\right] \tag{III.3}$$

where I_0 is the reverse saturation or the leakage current of the diode which can be written as:

$$I_0 = DT_C^3 \cdot \exp\left(\frac{-q\varepsilon_G}{A \cdot k}\right) \tag{III.4}$$

According to equations (1)-(3), the output current is given by:

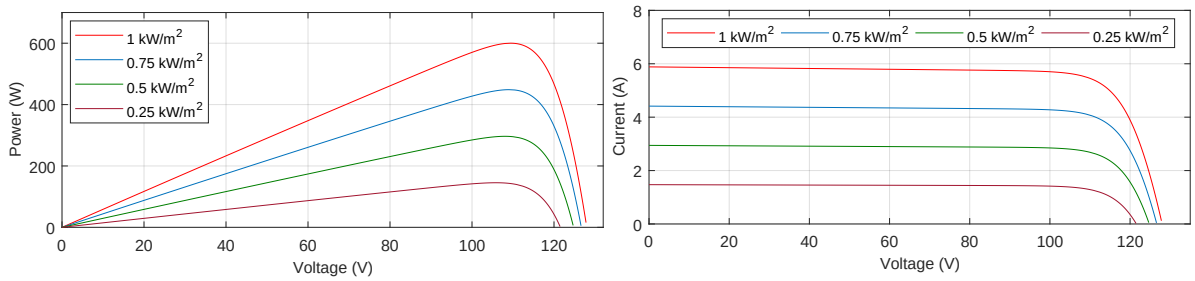
$$I_{pv} = \left(\frac{G}{G_{ref}}\right) \cdot (I_{ph,ref} + u_{sc} \cdot \Delta T) - I_0 \cdot \left[\exp\left(\frac{V_{pv} + R_S \cdot I_{pv}}{A \cdot N_S \cdot V_T}\right) - 1\right] - \frac{V_{pv} + R_S \cdot I_{pv}}{R_p} \tag{III.5}$$

Where V_{pv} is the PV output voltage, R_S is the series resistance (Ω), Rp is the parallel resistance (Ω),N_S is the number of PV cells connected in series, A is the ideality factor which depends on PV cell technology, V_T is the thermal voltage (26 mV at 300 K for a silicon cell),k is the Boltzmann constant $1.38110^{-23}J/K$ and $q$is the electron charge $1.602\ 10^{-19}C$ [77].

III.2.2 PV electrical characteristics

The PV source used in the proposed system is a PV array composed of two series 305-W-SPR-305-WHT PV modules [78]. The parameters of this module are listed in Table (A.2).

The P–V and I–V characteristic curves of the whole PV system under different irradiance (250, 500, 750 and 1000 W/m2) and constant temperature 25°C are plotted in Figure (III.2) .



(a) (b)

Figure III.2: a- P-V characteristics b- I-V characteristics

III.3 Two stage operation systems

The equivalent circuit of DC-DC boost converter is illustrated in Figure (III.3-a). Wherein, the power switch is connected in parallel and controlled to extract the maximum power from the PV source [79]. The DC-DC boost converter has two operation states according to the state of the power switch. Figure (III.3-b) illustrates the first case where the switch is ON. In this case the DC source is separated from the load due to the reverse biasing of the diode Db. Thus, the coil Lb stores all the power produced by the DC source, while the load is fed by the capacitor C_{dc}. In the second case where the power switch is OFF as shown in Figure (III.3-c), the diode Db is forward biased and the power produced by the DC source is delivered directly to the load. The output voltage increases due to the voltage across the coil Lb which is added to the DC input voltage.

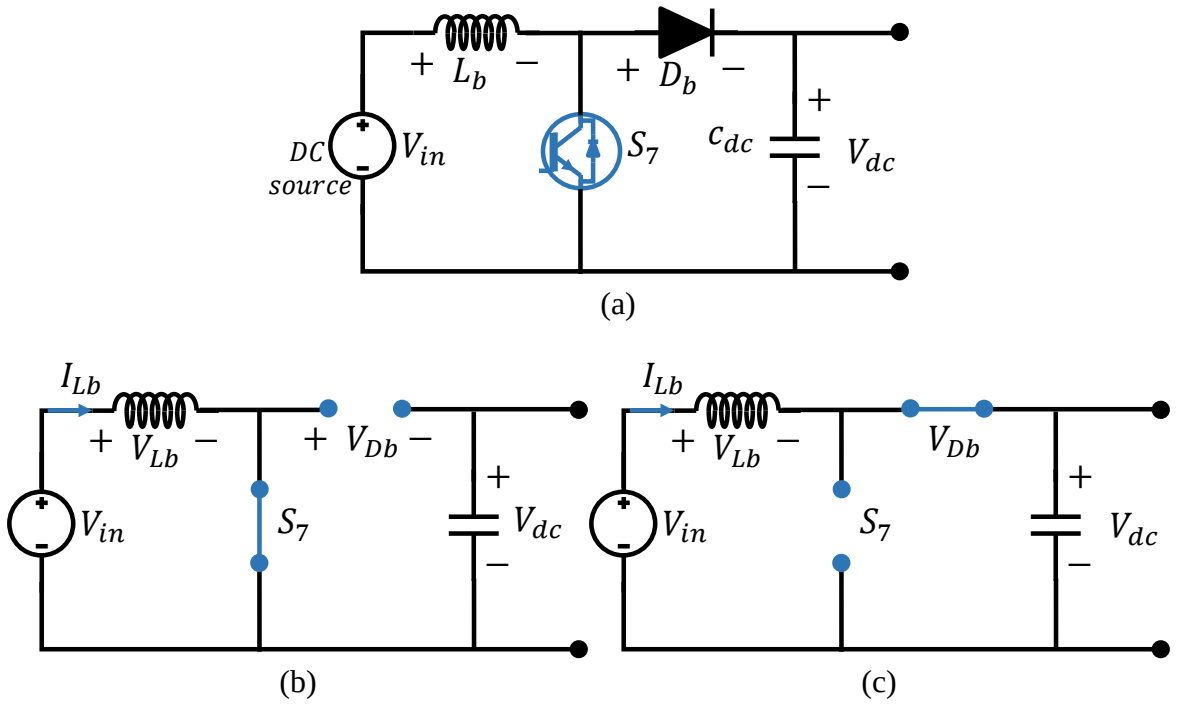


Figure III.3: a- DC-DC Boost converter equivalent circuit, b- ON state, and c- OFF state

In the first case while the switch is ON, the input voltage can be expressed by:

$$V_{in} = L_b \frac{dI_{Lb}}{dt} \tag{III.6}$$

In this case the current is increased by ΔIL_{b-on} where:

$$\Delta I_{Lb-on} = \int_0^{dT} dl_{Lb} = \int_0^{dT} \frac{V_{in} \cdot dt}{L_b} = \frac{V_{in} \cdot dT}{L_b} \tag{III.7}$$

Where d is the duty cycle which varies between 0 and 1. Next, in the second case while the switch is OFF as shown in Figure (III.3-c). The voltage across the inductor can be expressed as follows:

$$L_b \frac{dl_{Lb}}{dt} = V_{in} - V_{dc} \tag{III.8}$$

During this state the inductor current is varied by :

$$I_{Lb-off} = \int_{dT}^{(T} dIL_b = \int_{dT}^{T} \frac{(V_{in} - V_{dc}) \cdot dt}{L_b} = \frac{(V_{in} - V_{dc}) \cdot (1-d) \cdot T}{L_b} \tag{III.9}$$

The energy stored in the inductor is the same at the beginning and at the end of switching cycle, thus the total variation of the thus the inductor current has to be the same at the

start and end of the commutation cycle. This means the overall variation of the inductor current is zero as follows:

$$\Delta I_{Lb-on} + \Delta I_{Lb-off} = \frac{V_{in} \cdot dT}{L_b} + \frac{(V_{in} - V_{dc}) \cdot (1-d)T}{L_b} = 0 \tag{III.10}$$

Which leads to the following expression:

$$V_{dc} = \frac{1}{(1-d)}.V_{in} \tag{III.11}$$

III.4 Single stage operation systems

III.4.1 Z-source inverter

Z-source inverter (ZSI) was first proposed in 2003 [12]; this new topology helps overcome the existing problems associated with the conventional configurations. By adopting this topology, there is no need for an additional DC–DC converter due to the ZSI boosting feature which makes it capable of ensuring the functionalities of DC–DC and DC–AC converters with only one single configuration. The ZSI network makes the inverter stable and suitable for a wide range of input voltage [13]. In this topology, a symmetrical impedance network is placed as an interface between the DC source and the voltage source inverter which is called a Z-source network. A Z-source network is composed of two capacitors and two inductors as shown in Figure (III.4-a). A ZSI has the same two states as the classical voltage source inverter,namely, active state and zero state. The first state can be generated by six switching states where the DC voltage is applied directly across the load. The second state can be produced by two switching states where the load terminals are shorted through either lower or upper three devices.In addition to one extra zero state, named the shoot-through zero state, this unique state can be obtained by gating on both the upper and the lower switches of the same leg simultaneously. This scenario is forbidden in the conventional voltage source inverter and may damage the devices. ZSI has two operating modes: non-shoot-through mode and shoot-through mode [12]. The equivalent circuits of these modes are shown in figures (III.4-b) and (III.4-c), respectively.

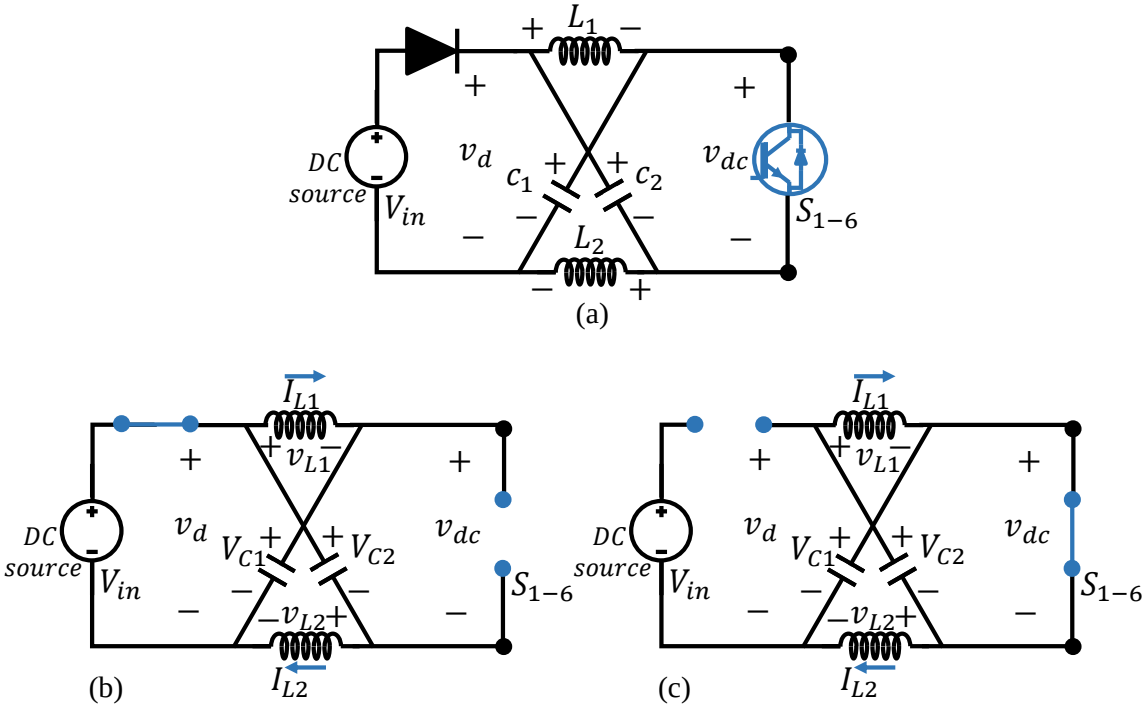


Figure III.4: a- ZSI equivalent circuit, b- non-shoot through state, and c- shoot through state

Because the Z-source network is identical:

$$V_{C1} = V_{C2} = V_C \tag{III.12}$$

$$v_{L1} = v_{L2} = v_L \tag{III.13}$$

From the circuit given in Figure (III.4-c) wherein the ZSI operates in the shoot-through mode for an interval T_0 during one switching cycle T:

$$v_{dc} = 0 \tag{III.14}$$

$$V_C = v_L \tag{III.15}$$

$$v_d = 2V_C \tag{III.16}$$

When the ZSI operates in the non-shoot-through mode during T_1 as $T = T_0 + T_1$

$$v_L = V_{in} - V_C \tag{III.17}$$

$$v_d = V_{in} \tag{III.18}$$

$$v_{dc} = V_C - v_l = 2V_C - V_{in} \tag{III.19}$$

The average voltage across the inductor is null during one switching period T in the steady state as follows:

$$V_L = \overline{v_L} = \frac{T_0 V_C + T_1 (V_{in} - V_C)}{T} = 0 \tag{III.20}$$

$$\frac{V_C}{V_{in}} = \frac{T_1}{(T_1 - T_0)} \tag{III.21}$$

The peak DC-link voltage can be expressed as:

$$\hat{V}_{dc} = BV_{in} \tag{III.22}$$

where B is the boost factor, given by:

$$B = \frac{T}{(T_1 - T_0)} \tag{III.23}$$

The output peak-phase voltage is then:

$$\hat{V}_{ac} = MB\frac{V_{in}}{2} \tag{III.24}$$

where M is the modulation index. Finally, the capacitor voltage can be calculated by the following equation:

$$V_C = \frac{1 - D_0}{1 - 2D_0} V_{in} \tag{III.25}$$

where D_0 is the shout-through duty ratio and is equal to T_0/T.

III.4.2 Quasi Z-source inverter

Figure (III.5-a) shows the equivalent circuit of Quasi Z-source inverter (QZSI). This topology has two states (non-shoot through state and shoot through state) same as in the conventional ZSI. The non-shoot through state includes six active states and two zero states of the conventional VSI, while the extra shoot through state can be generated by switching on the upper and lower switches of the same leg at the same time [12, 13, 80]. Equivalent circuits of both states are illustrated in figures (III.4-b) and (III.4-c). From the circuit illustrated in Figure 4-c, when QZSI operates in the non-shoot through state during the period T_1:

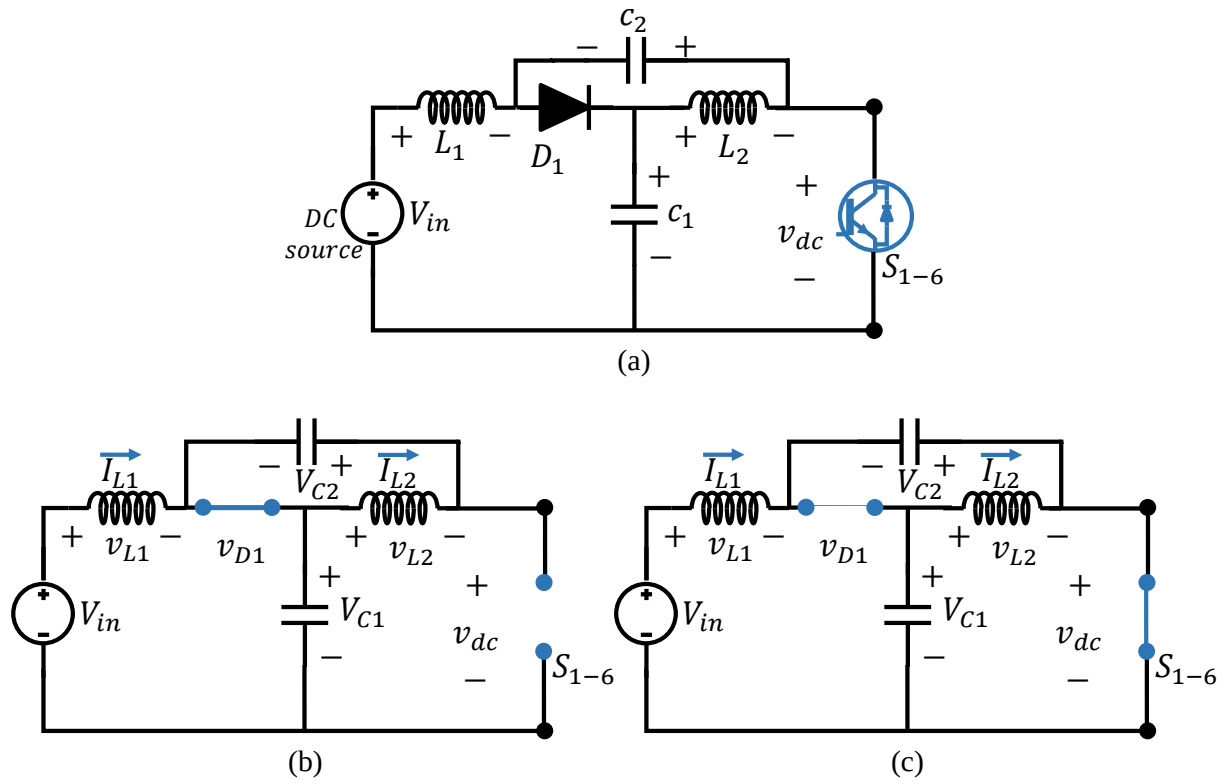


Figure III.5: a- QZSI equivalent circuit, b- non-shoot through state, and c- shoot through state

$$v_{L1} = V_{in} - V_{C1} \quad v_{L2} = -V_{C2} \tag{III.26}$$

$$v_{dc} = V_{C1} + V_{C2} \quad v_{D1} = 0 \tag{III.27}$$

During T_0, the period of the shoot through stat:

$$v_{L1} = V_{C2} - V_{in} \quad v_{L2} = V_{C1} \tag{III.28}$$

$$v_{dc} = 0 \quad v_{D1} = V_{C1} + V_{C2} \tag{III.29}$$

For one full switching period T, the average voltages across the inductors are null as expressed by:

$$V_{L1} = \overline{v_{L1}} = \frac{T_0 \cdot (V_{C2} + V_{in}) + T_1 \cdot (V_{in} - V_{C1})}{T} = 0 \tag{III.30}$$

$$V_{L2} = \overline{v_{L2}} = \frac{T_0 \cdot (V_{C1}) + T_1 \cdot (-V_{C2})}{T} = 0 \tag{III.31}$$

Thus

$$V_{C1} = \frac{T_1}{(T_1 - T_0)} \cdot V_{in} \tag{III.32}$$

$$V_{C2} = \frac{T_0}{(T_1 - T_0)} \cdot V_{in} \tag{III.33}$$

And the peak DC-link voltage can be obtained by:

$$\hat{v}_{dc} = V_{C1} + V_{C2} = B \cdot V_{in} \tag{III.34}$$

Where B is the boost factor and it can be expressed by:

$$B = \frac{1}{(1 - 2.D_0)} \tag{III.35}$$

Where D_0 is the shoot through duty ratio and its equal T_0/T, the peak DC-link voltage can be expressed with respect to the voltage across the first capacitor as follows:

$$\hat{v}_{dc} = \frac{V_{C1}}{(1 - D_0)} \tag{III.36}$$

According to [80], [81], quasi z-source inverter inherits all the advantages introduced by the conventional Z-source inverter besides to its unique features :

- Continuous input current and minimal Electromagnetic interference (EMI) within its circuit,
- Reduced source stress,
- Lower component ratings,
- Lower inrush current at start-up,
- Reduced voltage stress on the second capacitor,
- Smaller ripple distortions at lower boost factor,
- Negligible clipping of DC-link voltage waveform at lower boost factor.

Thus, the quasi Z-source topology will be used to interface the PV source in the proposed shunt active power filter.

III.4.3 Shoot-through control techniques

The shout-through zero state is generated when both the upper and lower switches of any phase are turned on at the same time, it can be produced in seven cases: one phase leg, tow phase legs and three phase legs. There are various control techniques for the impedance source topology namely, Simple boost control (SBC) [82], Maximum Boost Control (MBC) [83], Maximum constant Boost control (MCBC) [84], and Maximum Constant Boost Control with third harmonic injection (MCBCT) [85].

III.4.3.1 Simple Boost Control

In this control method the six active states of the traditional PWM stayed the same in addition to a positive straight line equal to the positive peak value of the sinusoidal voltage and negative straight line equal to the negative peak value of the sinusoidal voltage [86], as illustrated in Figure (III.6).

The duty ratio is varied according to the comparison between the two lines and the triangular signal, the inverter operates in the shoot-through mode in case when the positive straight line is lower than the triangular signal or the negative one is higher than the triangular signal, however, the inverter operates in the active mode during the rest period [87]. In this control approach the shoot-through duty ratio varies inversely with the modulation

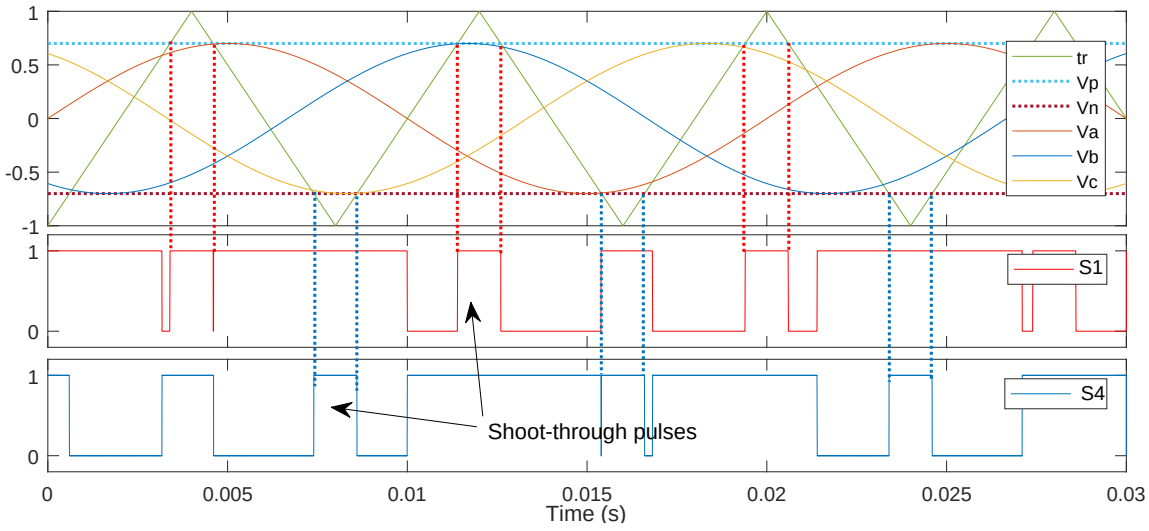


Figure III.6: Simple boost control scheme

index as expressed in the following equation:

$$D_0 = 1 - M \tag{III.37}$$

Where M is the modulation index.

The voltage gain of the Z-source inverter and the boost factor are respectively:

$$G = \frac{M}{2M-1} \tag{III.38}$$

$$B = \frac{1}{2M-1} \tag{III.39}$$

Finally the peak voltage stress at the input side of the inverter can be expressed as:

$$\hat{v_{dc}} = \frac{1}{2M-1} V_{in} \tag{III.40}$$

III.4.3.2 Maximum Boost Control

The maximum boost control strategy has been proposed as a solution to minimize the high stress voltage across the inverter switches produced the simple boost control method and maximize the shoot-through duty ratio, for such reason all the zero states are converted to a shoot-through states, therefore whenever the triangular wave is bigger than the positive peak of the reference signal or lower than the negative one the inverter operates in the shoot-through mode, otherwise it operates one of the six active states same as in the traditional PWM [12], the scheme of this control technique is shown in Figure (III.7).

Contrary to the simple boost control, the shoot-through duty ratio varies every cycle [86], however, it average value can be expressed as:

$$D_0 = \frac{2\pi - 3\sqrt{3}M}{2\pi} \tag{III.41}$$

The voltage gain and the boost factor in this control technique can be approximated as follows:

$$G = \frac{\pi M}{3\sqrt{3}M - \pi} \tag{III.42}$$

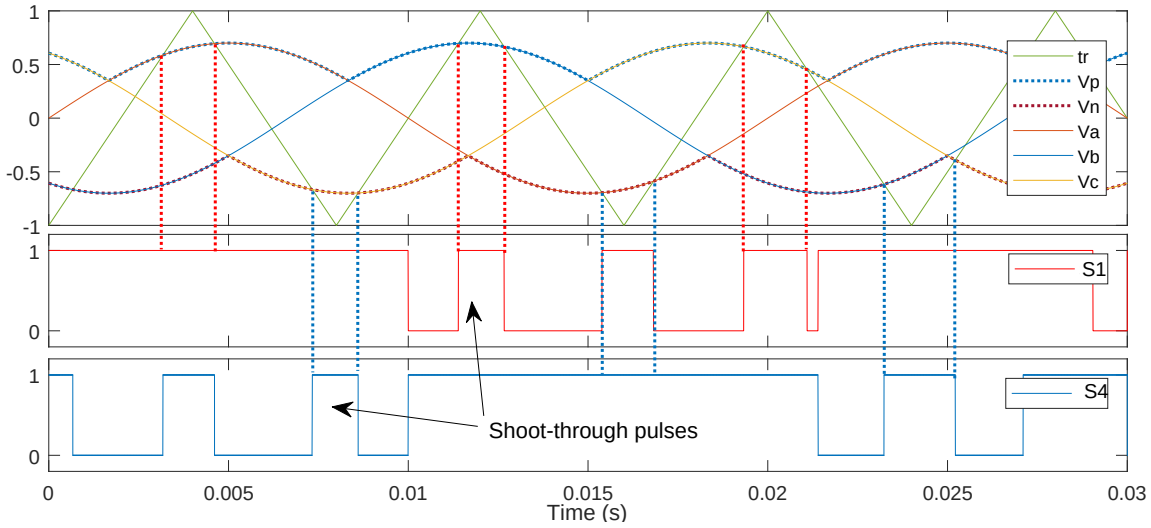


Figure III.7: Maximum constant boost control scheme

$$B = \frac{\pi}{3\sqrt{3}M - \pi} \tag{III.43}$$

Therefore, the peak DC-link voltage is:

$$\hat{v_{dc}} = \frac{3\sqrt{3}G - \pi}{\pi} V_{in} \tag{III.44}$$

III.4.3.3 Maximum Constant Boost Control

Due to the problem of the varying shoot-through duty ratio in the maximum boost control method, a new control strategy called maximum constant boost control has been proposed in [84]. This control strategy guarantees a constant shoot-through duty ratio, a high boost factor and reduced voltage stress. In this strategy two envelopes V_p and V_n have been used as shown in Figure (III.8), whenever the triangular signal is bigger than the positive envelope or smaller than the negative one, the inverter operates in shoot-through mode, otherwise the inverter is operating same as in the traditional six active states [84].

The two used envelopes are periodical with a frequency equals three times the reference signal frequency.

In the first part $(0, \pi/3)$ the envelopes can be expressed as:

$$V_p = \sqrt{3}M + sin(\theta - \tfrac{2\pi}{3})M \tag{III.45}$$

$$V_n = sin(\theta - \tfrac{2\pi}{3})M \tag{III.46}$$

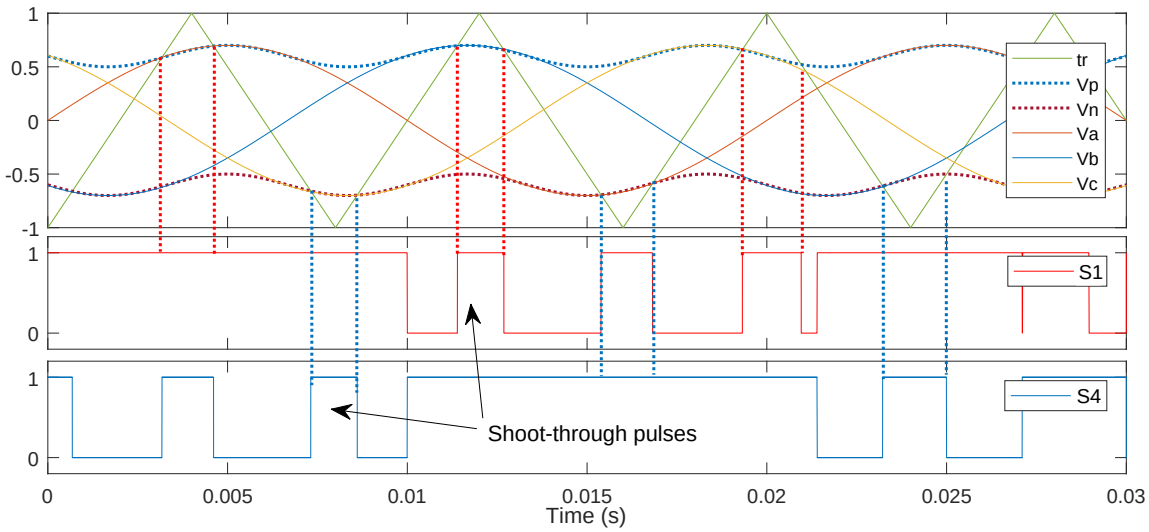


Figure III.8: Maximum constant boost control scheme

While in the second part $(/3, 2\pi/3)$ they can be calculated by:

$$V_p = sin(\theta)M \tag{III.47}$$

$$V_n = sin(\theta)M - \sqrt{3}M \tag{III.48}$$

From Figure (III.8), the distance between the two envelopes are the same, which makes the shoot-through duty ratio constant and can be approximated by the formula:

$$D_0 = 1 - \frac{\sqrt{3}M}{2} \tag{III.49}$$

The voltage gain and the boost factor meet the equations (III.50) and (III.51) respectively:

$$G = \frac{M}{\sqrt{3}M-1} \tag{III.50}$$

$$B = \frac{1}{\sqrt{3}M-1} \tag{III.51}$$

The voltage gain in this control technique increases from 0 to infinity by decreasing the modulation index from 1 to $(\sqrt{3}/3)$ [88].

III.4.3.4 Maximum constant boost control with third harmonic injection

There is another way to implement the maximum constant boost control strategy by injecting a third harmonic signal whose amplitude equals to one-sixth of the sinusoidal and frequency equals three times the main frequency as illustrated in Figure (III.9).

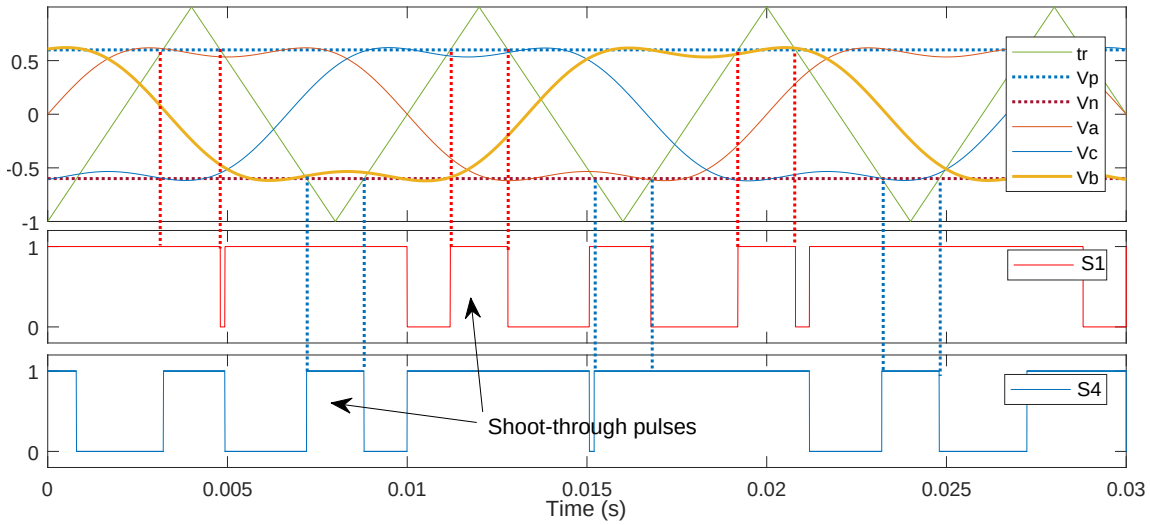


Figure III.9: Maximum constant boost control with third harmonic injection with third harmonic injection

The advantage of this method is that the modulation index range is increased to $(2\sqrt{3}/3)$ instead of 1 in the conventional maximum constant boost control. In addition, this method overcomes the problem of the variable shoot-through duty ratio and provide a constant shoot through duty ratio can be represented by two straight lines same as in the simple boost control [82].

The voltage gain can be calculated as:

$$G = \frac{\pi M}{3\sqrt{3}M - \pi} \tag{III.52}$$

The boost factor and DC-link voltage can be expressed by equations (III.53) and (III.54) respectively:

$$B = \frac{\pi}{3\sqrt{3}M - \pi} \tag{III.53}$$

$$\hat{v_{dc}} = \frac{3\sqrt{3}G - \pi}{\pi} V_{in} \tag{III.54}$$

III.5 Maximum power point tracking

Maximum power point tracking (MPPT) approaches can be divided into direct and indirect methods as detailed in (Appendix C). among the indirect methods there are the Short-circuit current (SCC) [89] and fractional open circuit voltage (OCV) based methods [90], which have a simple structure compared to the other methods. However, they impose an ongoing measurement for the SCC and OCV, leading eventually to a PV power losses. For the direct methods there are perturbation and observation (P&O) strategy which is extensively adopted due to its simple implementation. However, this method acts on the perturbation of the generated reference voltage. Therefore, an extra regulator is needed. In addition, the maximum power point could be missed by the PO tracker in case of highly unsteady environmental conditions.Hill climbing method has the same flowchart as P&O technique. However, it acts directly on the duty cycle [31].

III.5.1 Incremental conductance MPP tracker

Among the direct methods, the incremental conductance (InC) method which is widely used owing to its accurate operating and quick response under both steady and unsteady environmental conditions [91]. This method is based on the rate of change of the photovoltaic power with respect to the photovoltaic voltage as given by the following equations:

$$\frac{dP_{pv}}{dV_{pv}} = \frac{d(I_{pv}V_{pv})}{dV_{pv}} \tag{III.55}$$

$$\frac{dP_{pv}}{dV_{pv}} = I_{pv} + V_{pv}\frac{dI_{pv}}{dV_{pv}} \tag{III.56}$$

From equation (III.56), when the operating point reaches the maximum power point the equation becomes:

$$\frac{dP_{pv}}{dV_{pv}} = 0 \Rightarrow \frac{dI_{pv}}{dV_{pv}} = -\frac{I_{pv}}{V_{pv}} \tag{III.57}$$

When the operating point is located at the left of the maximum power point, the equation (III.56) becomes:

$$\frac{dP_{pv}}{dV_{pv}} > 0 \Rightarrow \frac{dI_{pv}}{dV_{pv}} > -\frac{I_{pv}}{V_{pv}} \tag{III.58}$$

Therefore, the photovoltaic voltage should be increased to reach the maximum power. When the operating point is located at the right of the operating point, we obtain:

$$\frac{dP_{pv}}{dV_{pv}} < 0 \Rightarrow \frac{dI_{pv}}{dV_{pv}} < -\frac{I_{pv}}{V_{pv}} \tag{III.59}$$

In this case, the photovoltaic voltage should be decreased to reach back the maximum power. Moreover, the maximum power point can be reached be comparing the instantaneous conductance I_{pv}/V_{pv} to incremental conductance dI_{pv}/dV_{pv} [31]. The flowchart of the incremental conductance technique is illustrated in Figure (III.10).

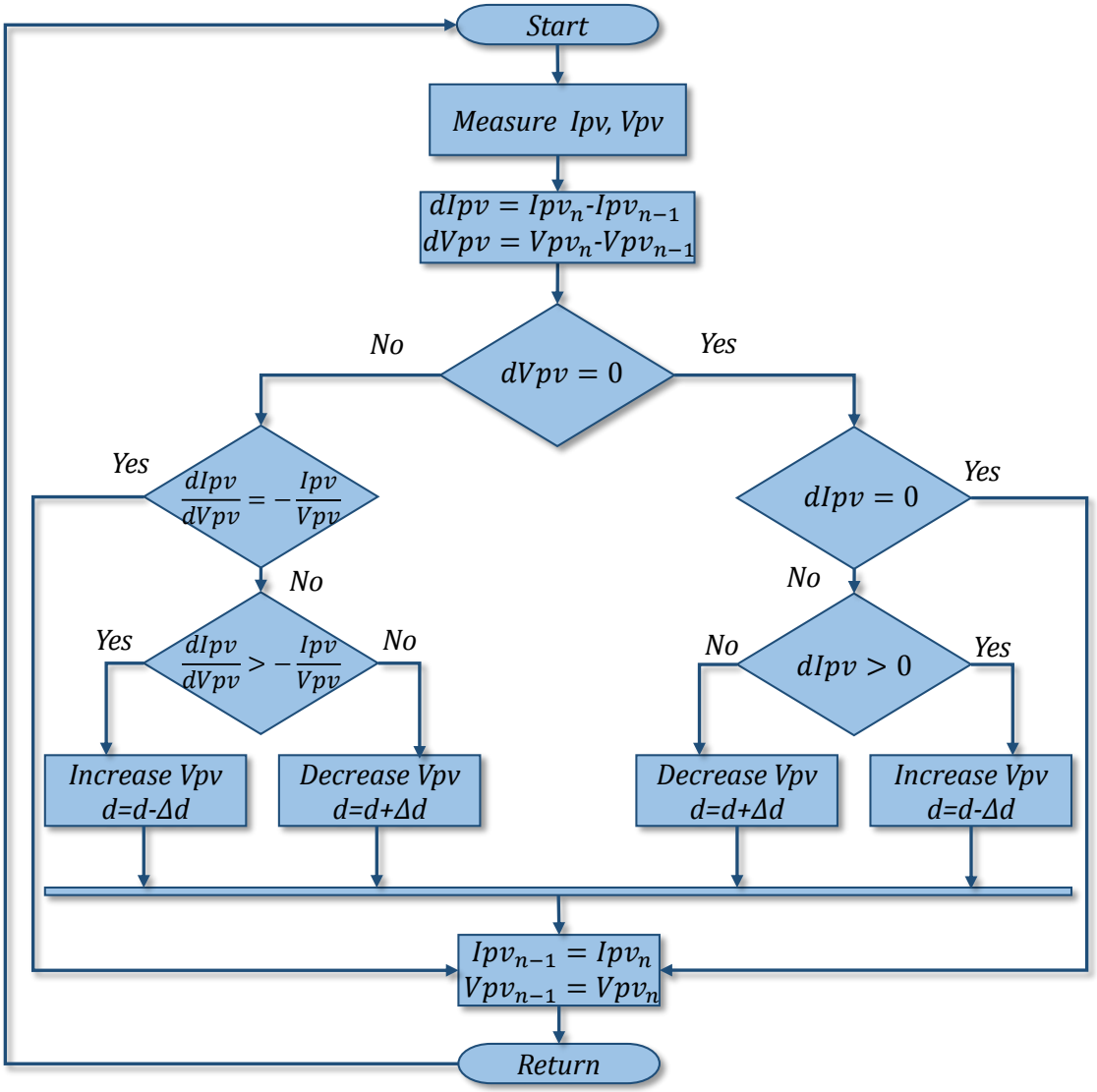


Figure III.10: Incremental conductance MPPT flowchart

III.6 Conclusion

In this chapter we presented both the conventional filter connected to a PV system through a DC-DC boost converter and the proposed filter configuration based on impedance source inverter. The single-stage conversion chain ensures the tasks of the conventional DC-DC converter plus VSI using one converter (impedance source inverter) since it is easily able to track the maximum power and controls the injected current using one control scheme. Eventually, the size and the complexity of the overall system is decreased.
Furthermore, the improved Quasi Z-source inverter offers promising features and overcomes the shortcomings of the classical topology. Therefore, Quasi Z-source inverter will be used in the proposed active power filter connected to a PV system based on single-stage conversion chain.Moreover, simple boost approach is used owing to its simple implementation and constant shoot through duty ratio and incremental conductance MPP tracker is used to track the maximum power.

Chapter IV

Shunt active power filter connected to a PV system

IV.1 Introduction

The shunt active filter is connected to the PV source through two stage configuration based on DC-DC boost converter and one stage configuration based on QZSI. To perform an extensive analysis, the both configurations shown in Figure (IV.1) and Figure (IV.2) are tested under dynamic load, unsteady irradiance, and faulty conditions. The comparison is performed in terms of harmonic suppression efficiency, MPP tracking accuracy and power conversion ratio under unsteady irradiance, and power loss and current peak under faulty conditions. The simulation parameters of the conventional and the proposed systems are listed in Tables (A.1) and (A.2).

IV.2 Overall control strategy

In the overall control scheme shown in Figure (IV.3) the synchronous reference theory is used to extract the harmonic and reactive components from the source current and identify the compensating reference current. Then, the injected current tracks the reference currents and the error between them is minimized by the backstepping controller. The generated signal is compared to a 5 kHz triangular signal to generate the switching signals.In the two stage configuration the DC-link control is maintained directly by comparing the reference voltage and the measured voltage and minimizing the error using anti-windup PI controller.

However, this strategy is difficult to achieve in the single stage configuration because of the pulsating nature of the DC-link voltage waveform. Furthermore, the peak value of the DC-link voltage can be controlled indirectly by controlling the voltage across the QZSI

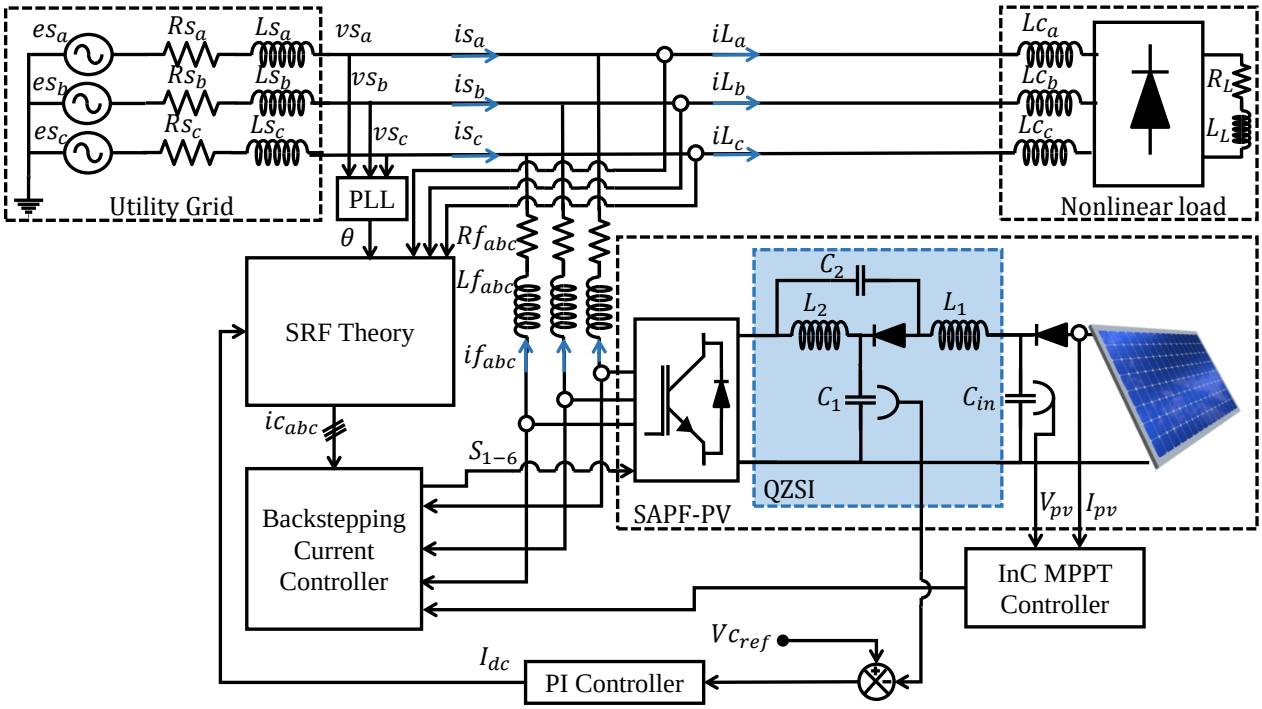


Figure IV.1: Configuration of SAPF based on two-stage PV system

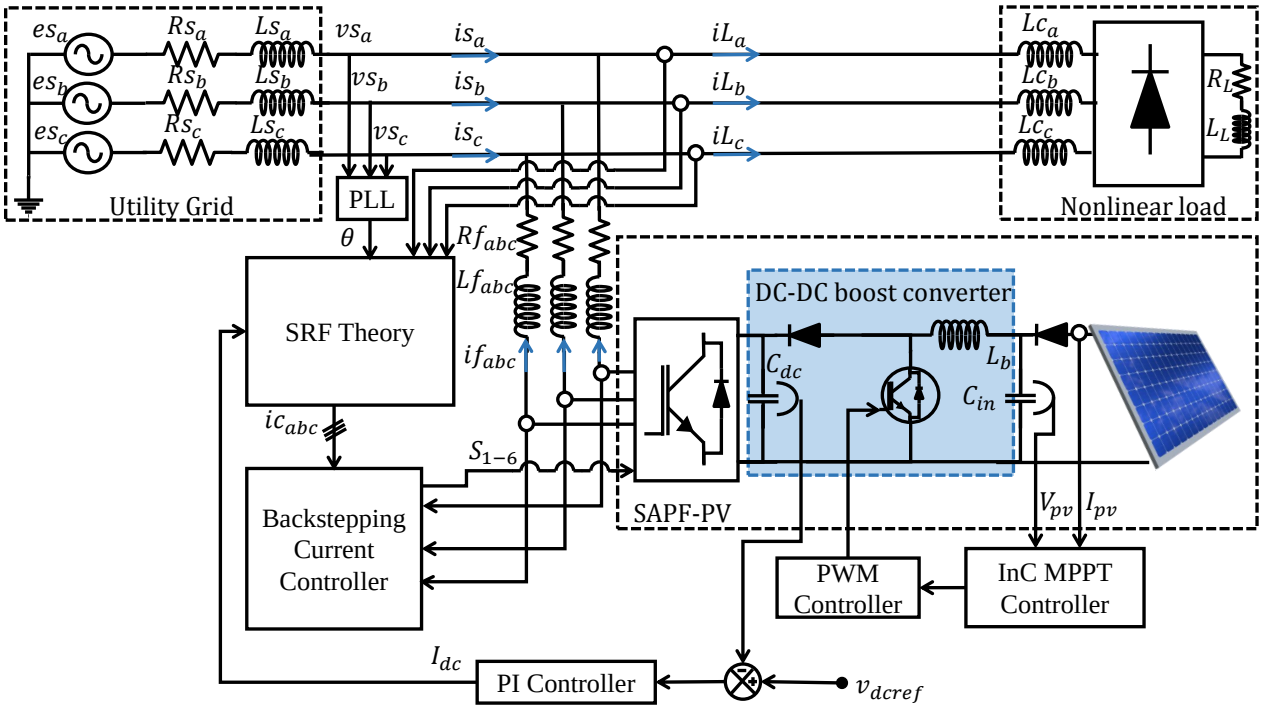


Figure IV.2: Configuration of SAPF based on single-stage PV system

capacitor according to equation (III.36). The MPP tracking can be ensured by incremental conductance MPP tracker which controls the DC-DC boost converter in two stage configuration. On the other hand, the incremental conductance MPP tracker is used to generate the shoot through duty ratio which adjusts the two PWM extra lines (V_p,V_n)of the Simple Boost Control strategy used in the single stage configuration.

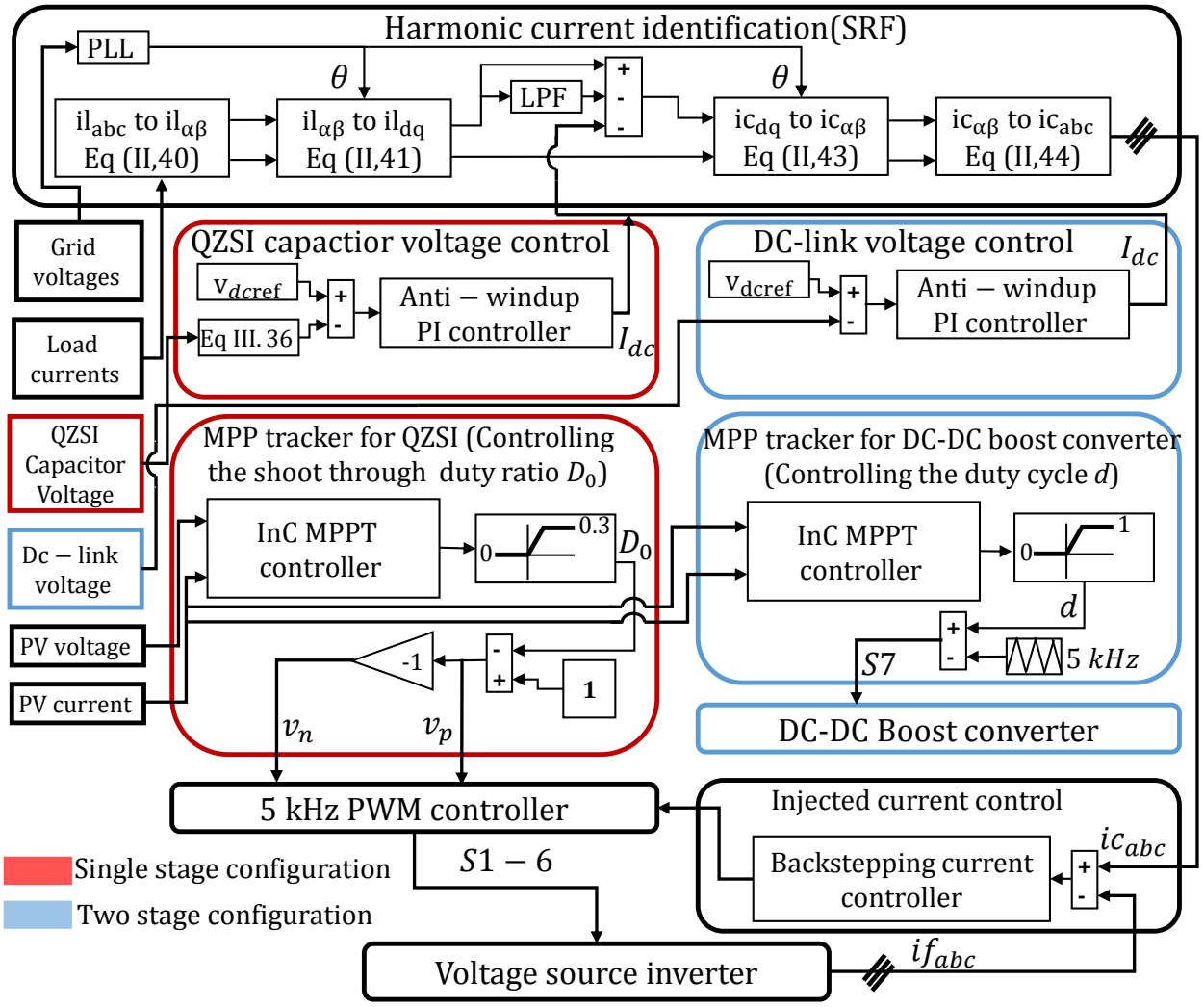


Figure IV.3: Overall control strategy

IV.3 Simulation results

IV.3.1 Under dynamic load

IV.3.1.1 SAPF based on two-stage PV system

The shunt active power filter connected to the PV source through a two stage configuration has been tested under fixed temperature of 25 C^o and irradiance of 500 W/m^2 and sudden load variation during 0.3s and 0.4s by a 20% increase as it is obvious in Figure (IV.4-a).As presented in Figure (IV.4-b) the injected current has been increased accordingly to ensure the filtering operation under the new load requirement. Despite the quick variation, the source current has been maintained sinusoidal (with THD of 2%) and in phase with the grid voltage as illustrated in Figure (IV.4-c). The DC-link voltage has encountered small deviations at the instants of load increase and decrease. However, it has been regulated after 0.05s as shown in Figure (IV.5-a). The instantaneous active power of the main source has been increased and decreased smoothly and the reactive power is compensated despite the slight increase during the load increase as illustrated in Figure (IV.5-b) and Figure (IV.5-c) respectively.

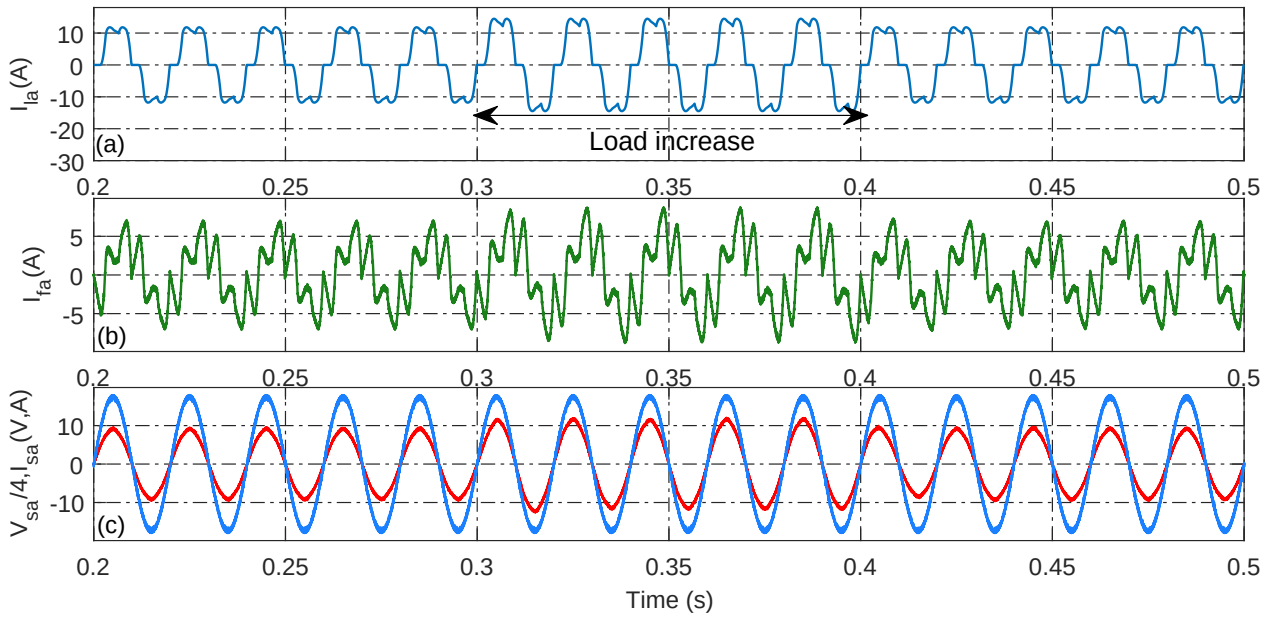


Figure IV.4: Dynamic load: a- load current, b- injected current, c- source voltage and current

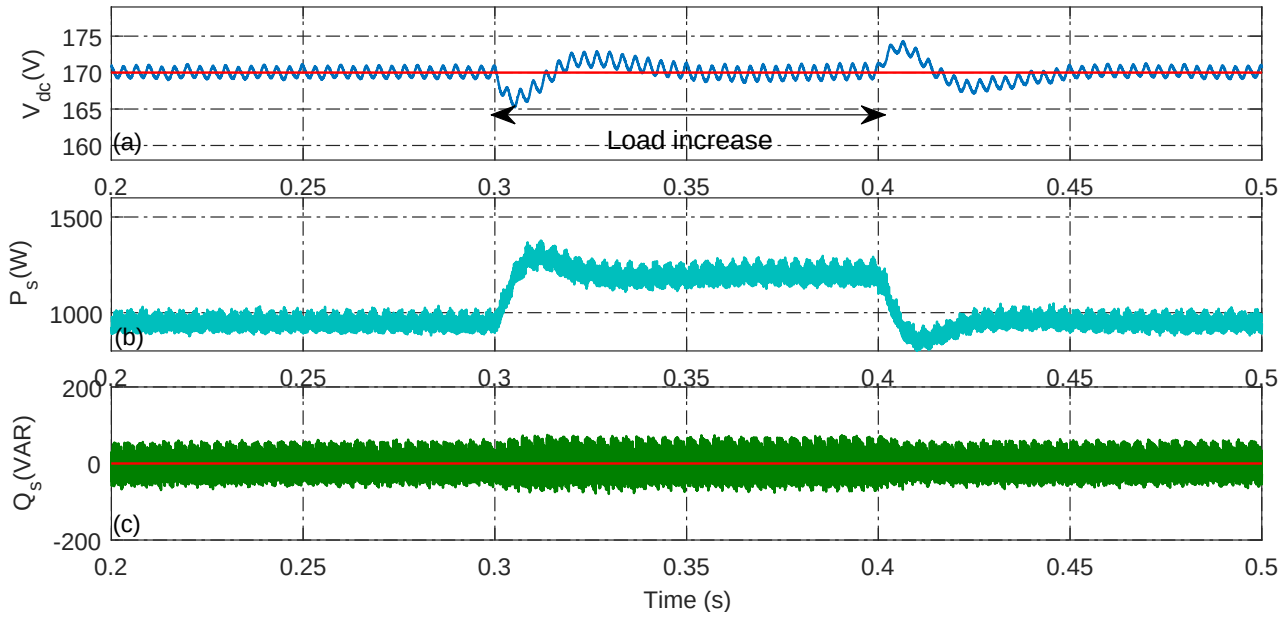


Figure IV.5: Dynamic load: a- DC-link voltage, b- instantaneous active power, and c- instantaneous reactive power

IV.3.1.2 SAPF based on single-stage PV system

In this test the shunt active power filter which is connected to a PV source through a single stage configuration based on quasi Z-source inverter has been run under the same circumstances as the first configuration. We apply a sudden 20% load demand increase during 0.3s and 0.4s as presented in Figure (IV.6-a). As it can be seen in Figure (IV.6-b), the filter adjusts the magnitude of the injected current to fulfill the harmonic elimination under the new condition. Therefore, the harmonics of the source current are well eliminated and the source current has a sinusoidal wave with THD of (1.57%) and in phase with the grid voltage during load demand increase as shown in Figure (IV.6-c). The voltage across the DC-link has two levels, during the non-shoot through state it has been indirectly regulated to follow the reference value by controlling the voltage across the QZSI capacitor to follow the reference DC-link voltage. Whereas On it equals 0 during the shoot though state due to short-circuiting the upper and the lower switch in the same leg. During load increase the capacitor voltage is regulated after small drop and raise to support the sudden load variation as shown in Figure (IV.7-a).

The instantaneous active power has been increased and decreased smoothly with no significant overshoot as presented in Figure (IV.7-b). Finally, the reactive power is well compensated as illustrated in Figure (IV.7-c).

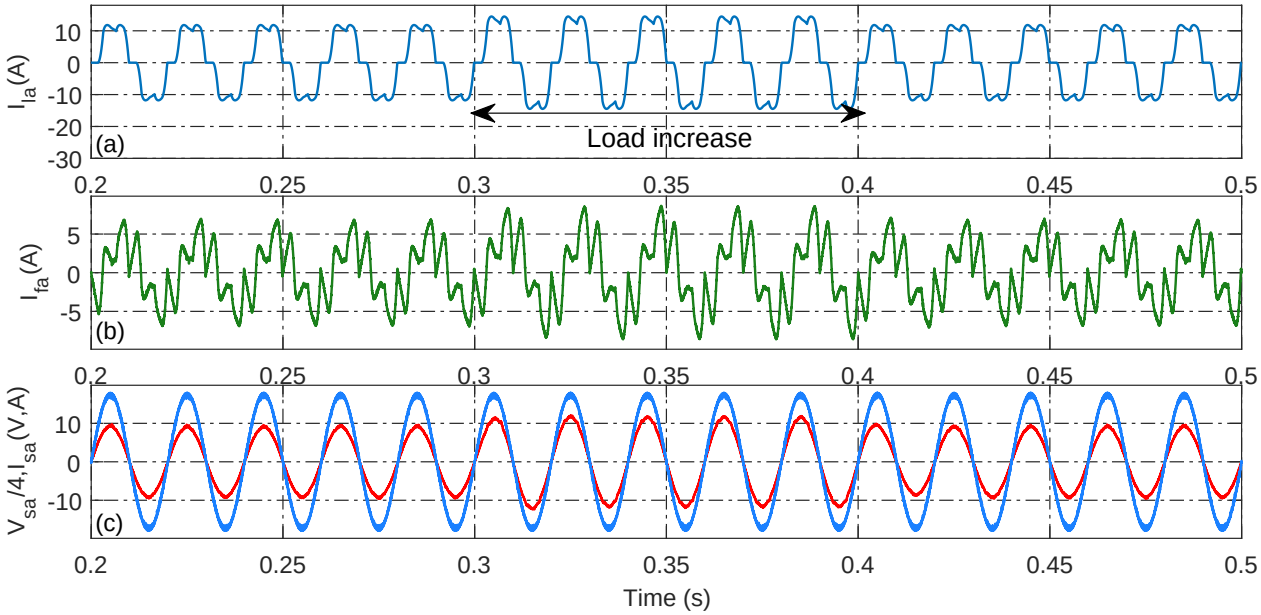


Figure IV.6: Dynamic load: a- load current, b- injected current, c- source voltage and current

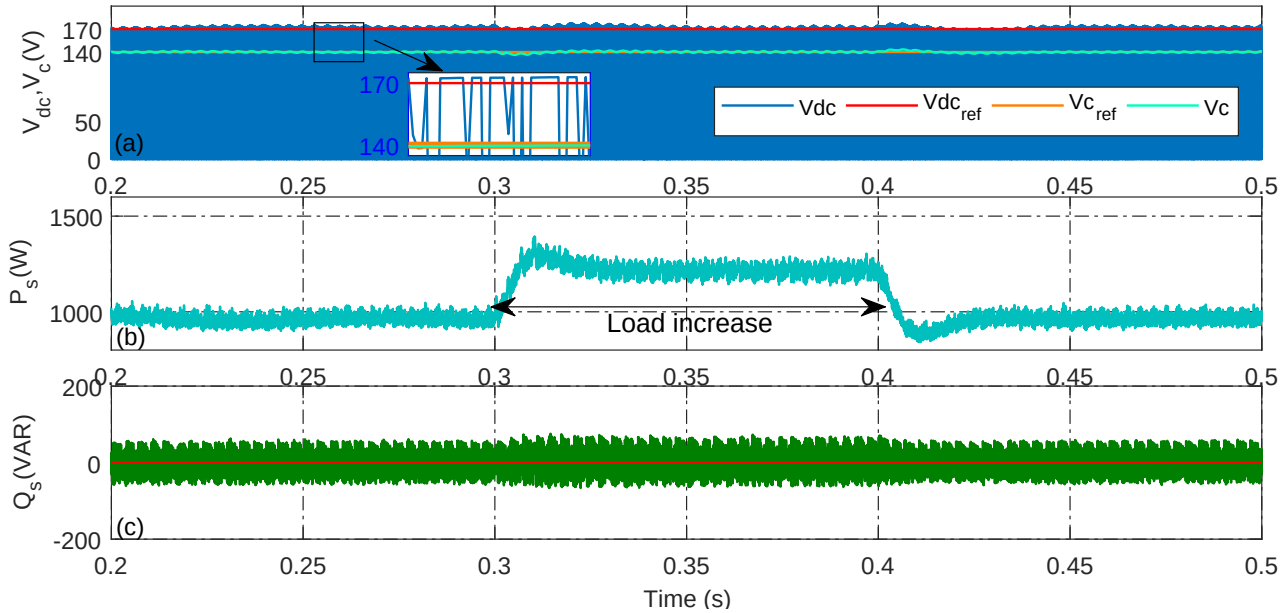


Figure IV.7: Dynamic load: a- DC-link and capacitor voltage, b- instantaneous active power, and c- instantaneous reactive power

IV.3.2 Under unsteady irradiance

To further investigate the performance of the traditional filter based on two-stage PV system and the proposed filter based on single-stage PV system, we test system under a varying irradiance.

IV.3.2.1 SAPF based on two-stage PV system

Figure (IV.8-a) shows that the load current is totally distorted due to the harmonic components produced by the nonlinear load. The harmonics of the source current are eliminated and its magnitude has been decreased due to the increase of the irradiance from $500W/m^2$ to $1000W/m^2$ as shown in Figure (IV.8-b). The reactive power is well compensated through the entire irradiance profile as illustrated in Figure (IV.8-c).

As it can be observed in Figure (IV.9-a), the voltage across the DC-link has encountered small peaks at the instants of irradiance increase. However, it is regulated to follow the reference voltage after a transient period of 0.03s. The active power produce by the utility grid has been decreased due to the power injected by the PV system as shown in Figure (IV.9-b). In Figure (IV.9-c), the PV power is tracking the maximum power very accurately despite the quick variation of irradiance.

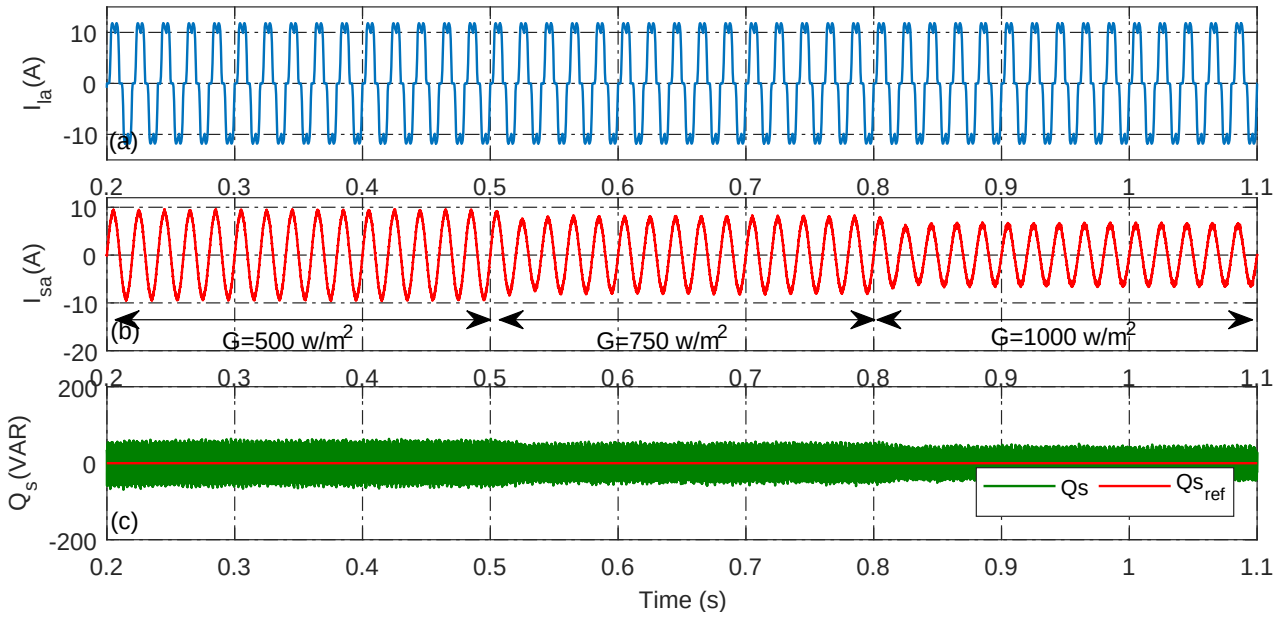


Figure IV.8: Unsteady irradiance: a- load current, b- source current, and c- reactive power

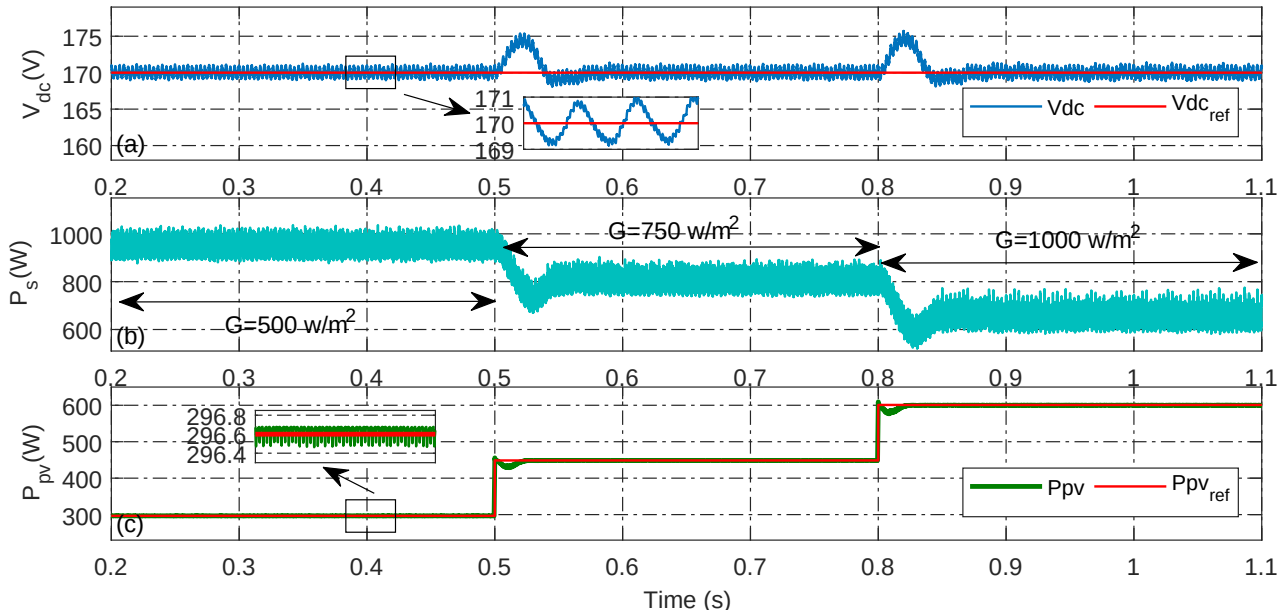


Figure IV.9: Unsteady irradiance: a- DC-link voltage, b- instantaneous active power, and c- PV power

IV.3.2.2 SAPF based on single-stage PV system

To validate the performance of the proposed filter based on single-stage PV system, we run the system under an unsteady irradiance as in the previous simulation. Figure (IV.10-a) shows the source current which is filtered and its THD has been minimized to reach 1.83%.

On the same hand the magnitude of the source current has been decreased owing to the power injected by the PV system. It is observed that the active power in the proposed configuration has less steady state oscillations compared to the conventional configuration as illustrated in Figure (IV.10-b). Moreover, the proposed configuration provides better reactive power compensation as shown in Figure (IV.10-c).

Despite the irradiance quick variation, the peak value of the voltage across the DC-link is regulated to track the reference value during the non-shoot through state by controlling the voltage across the QZSI capacitor which is regulated after small deviations at the 0.5s and 0.9s. The DC-link voltage and the QZSI capacitor voltage are shown in Figure (IV.11-a) and (IV.11-a) respectively.

The proposed configuration provides good MPP tracking but not as in the traditional configuration as illustrated in Figure (IV.11-c).

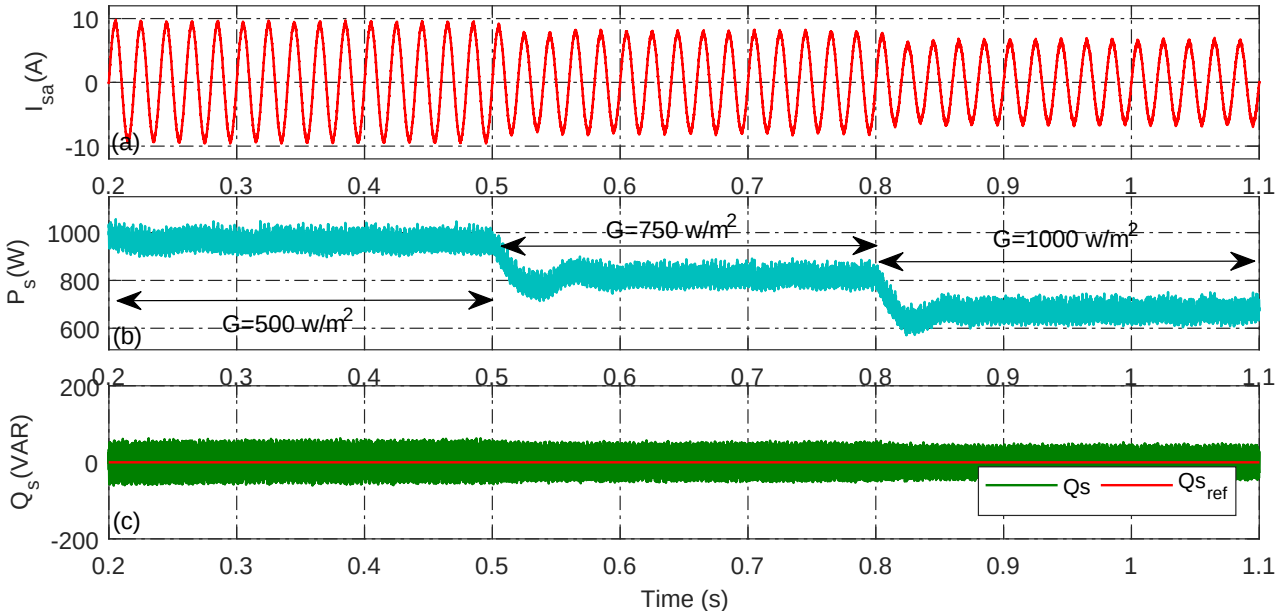


Figure IV.10: Unsteady irradiance: a- source current, b- instantaneous active power, and c- instantaneous reactive power

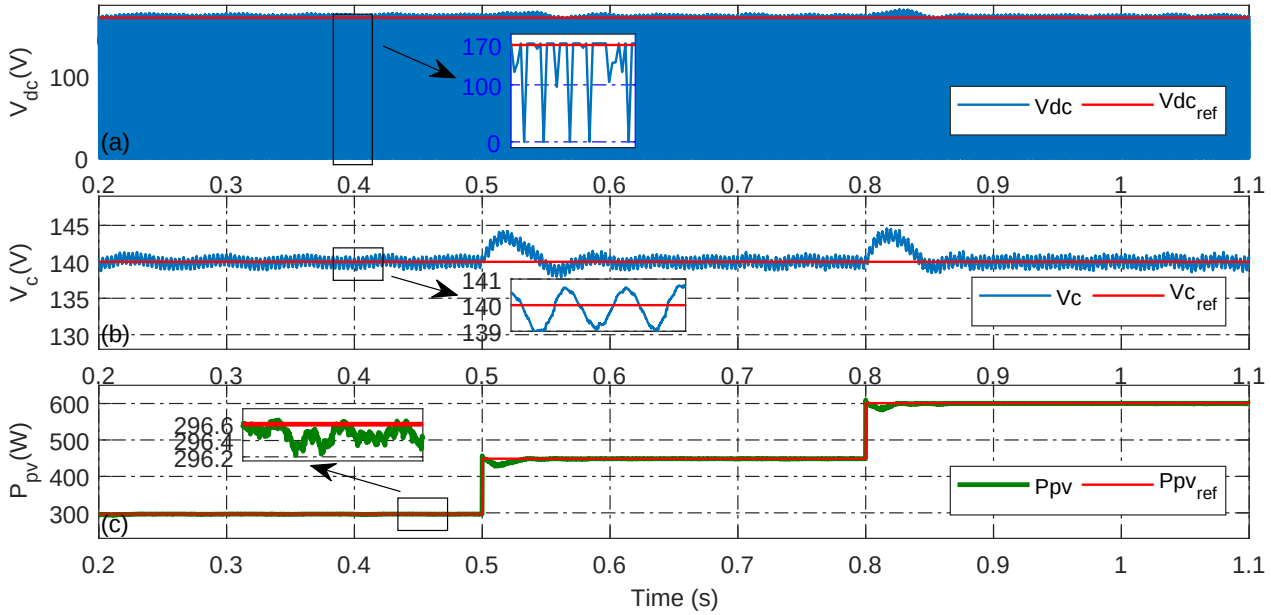


Figure IV.11: Unsteady irradiance: a- DC-link voltage, b- QZSI capacitor voltage, and c- PV power

IV.3.3 Under short-circuit fault

IV.3.3.1 SAPF based on two-stage PV system

In this test we provoke a short-circuit fault by applying a continuous conducting in the upper switch of the first phase during 100 μs. This causes high peak in the source current (about 17 A) above the peak during the normal operation as shown in Figure (IV.12-a).

As it is clearly seen in Figure (IV.12-b), the injected current encountered negative peaks. Moreover, short-circuiting the upper and the lower switch of the same leg causes a DC-link voltage drop to 0 v. After a recovery period of 0.05s, the DC-link voltage follows the reference voltage as illustrated in Figure (IV.12-c). As it is observed in Figure (IV.13-a), the fault causes high active power increase (>3 kW).

Moreover, the reactive power has encountered high deviations as well during the fault as shown in Figure (IV.13-b). The fault affects the DC side by causing drops in the PV power which tracks the maximum power after recovery period of 0.15s as illustrated in Figure (IV.13-c).

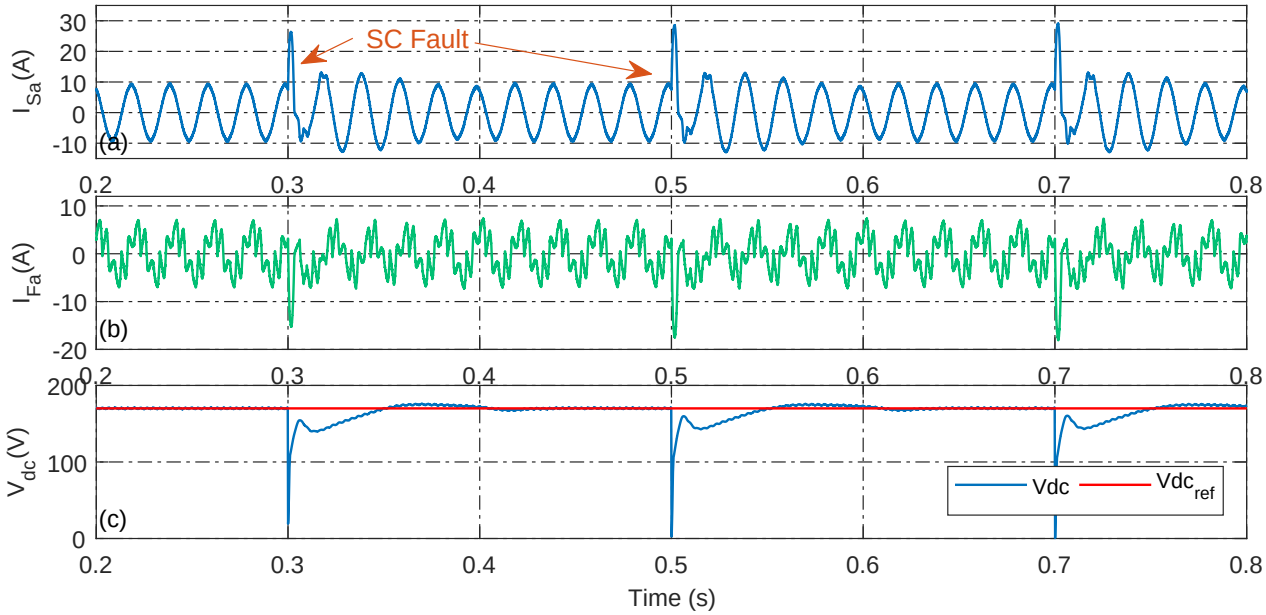


Figure IV.12: SC fault: a- source current, b- injected current, and c- DC-link voltage

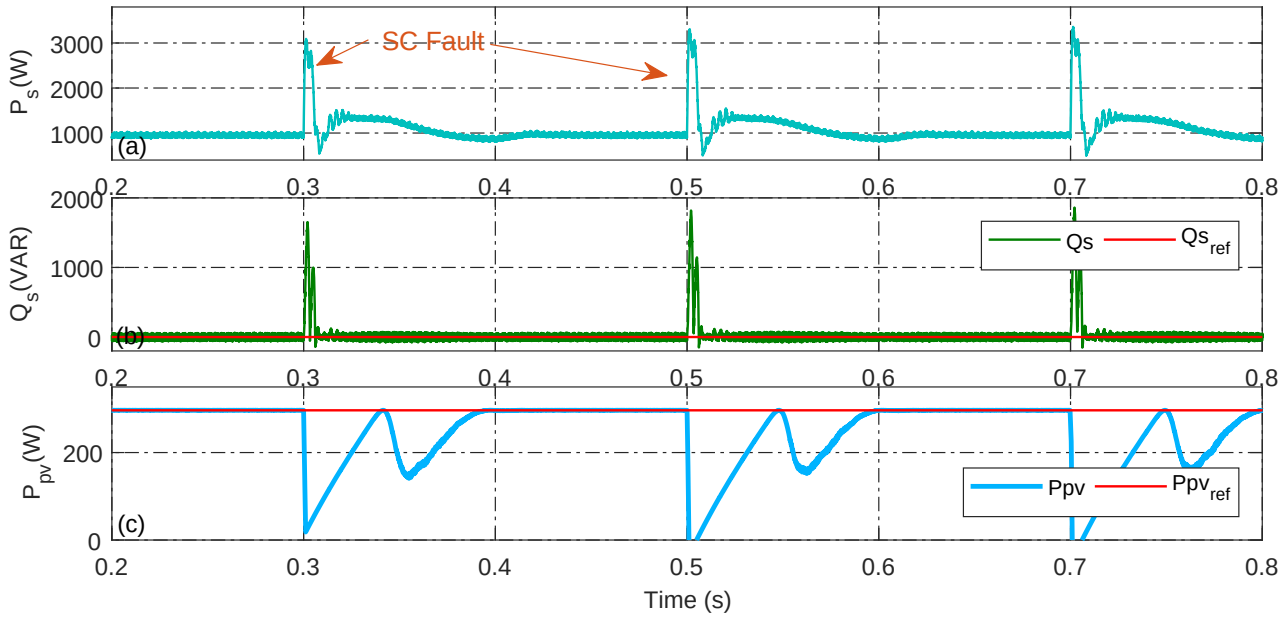


Figure IV.13: SC fault: - instantaneous active power, b- instantaneous reactive power, and c- PV power

IV.3.3.2 SAPF based on single-stage PV system

Unlike in the conventional configuration, due to the network of passive components used in the proposed configuration, the short-circuit fault causes almost no significant peaks in the source current and the injected current as illustrated in Figure (IV.14-a) and Figure (IV.14-b) respectively. The fault causes noticeable peaks in the voltage across the DC-link and across the QZSI capacitor. however, they track the reference voltages after recovery period of 0.05s as shown in Figure (IV.14-c).

Moreover, the instantaneous active power of the main power source has smaller peaks compared to the conventional configuration as presented in Figure (IV.15-a). As it is shown in Figure (IV.15-b), the compensation of reactive power shown in Figure (IV.15-b) has not been influenced by the fault unlike in the conventional configuration wherein the reactive power has encountered significant peaks. Moreover, the PV power tracks the MPP after small drops and recovery period of 0.05s as illustrated in Figure (IV.15-c).

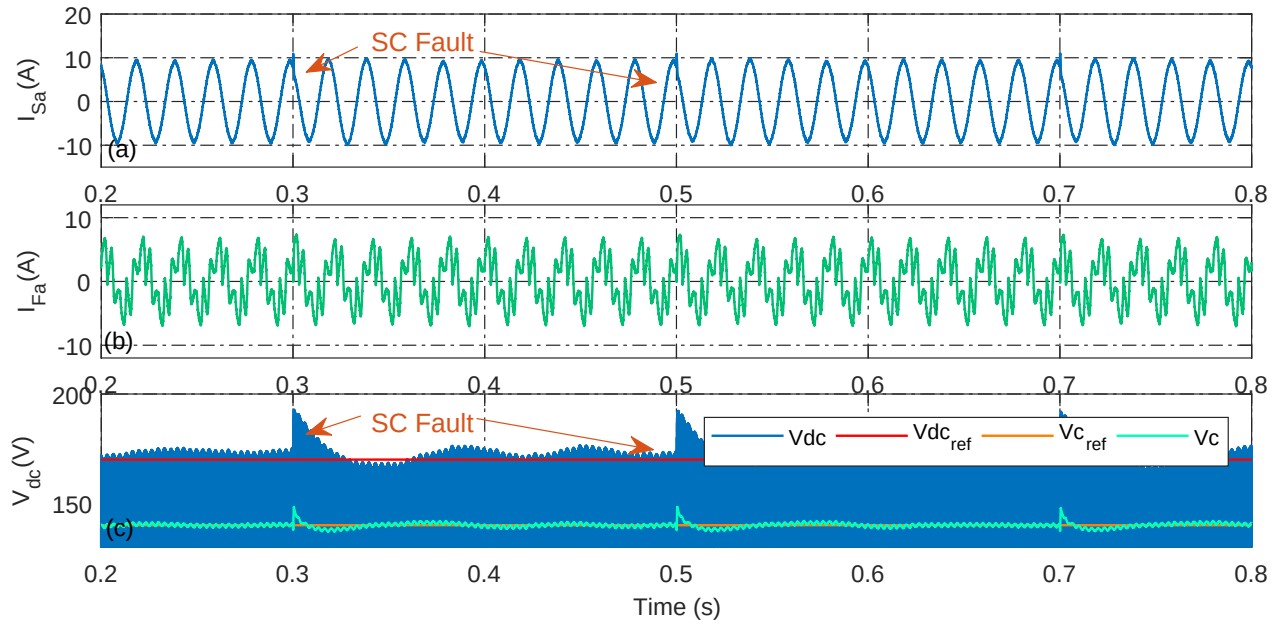


Figure IV.14: SC fault: a- source current, b- injected current, c- DC-link and QZSI capacitor voltage

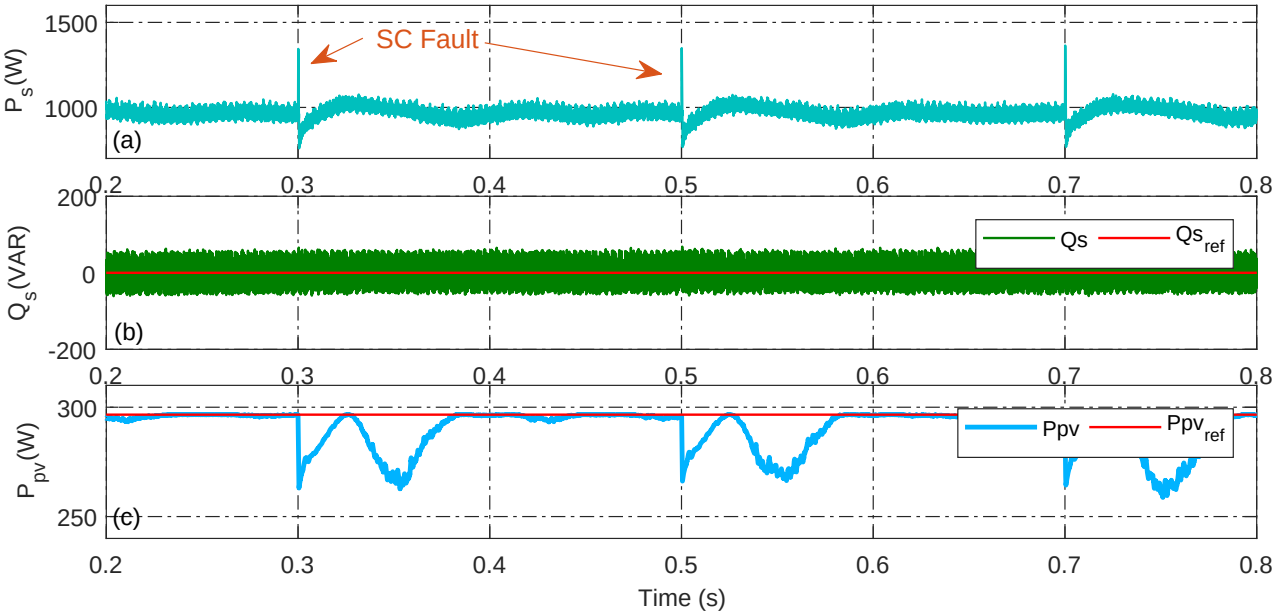


Figure IV.15: SC fault: a- instantaneous active power, b- instantaneous reactive power, and c- PV power

IV.3.4 Overall evaluation

The configuration of SAPF based on two-stage PV system and single-stage PV system are evaluated in terms of their performance in suppressing the harmonic components from the source current under dynamic load condition. From Figure (IV.16), it is clearly seen that the proposed configuration provides better harmonic mitigation during the entire steady state profile ($1.57\% < THDis < 1.85\%$) compared to the THD provides by the conventional configuration ($1.96\% < THDis < 2.48\%$).

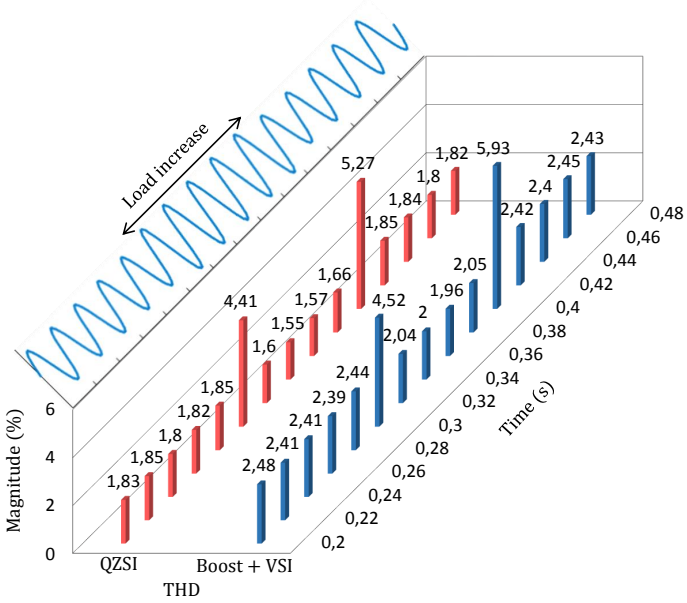


Figure IV.16: THD profile of source current under dynamic load

Under unsteady irradiance the proposed configuration gives better harmonic mitigation through the entire irradiance profile: 1.78% under $500W/m^2$, 2.32% under $750W/m^2$, and 3.21% under $1000W/m^2$ compared to the THD of the source current filtered by the conventional configuration: 2.46% under $500W/m^2$, 3.2% under $750W/m^2$, and 5.14% under $1000W/m^2$ as shown in Figure (IV.17).

For the power conversion efficiency, the conventional configuration ensures higher ratio between 92.7% under $500W/m^2$ and 95.9% under $1000W/m^2$ compared to the proposed configuration which provides a power conversion ration between 87.3% under $500W/m^2$ and 93.5% under $1000W/m^2$ as shown in Figure (IV.18).

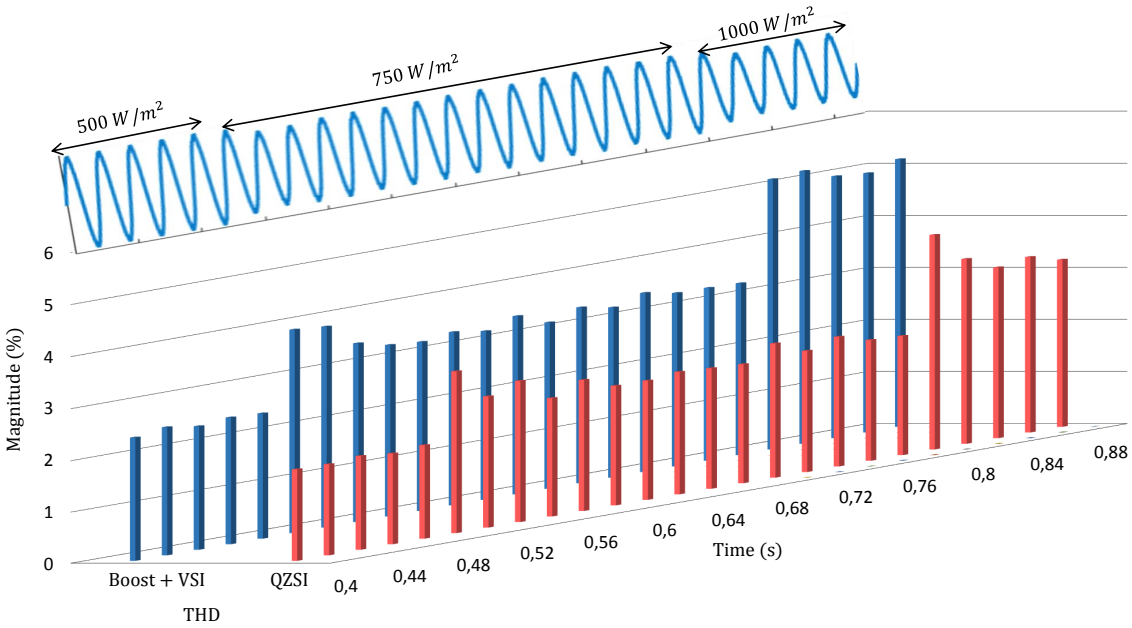


Figure IV.17: THD profile of source current under unsteady irradiance

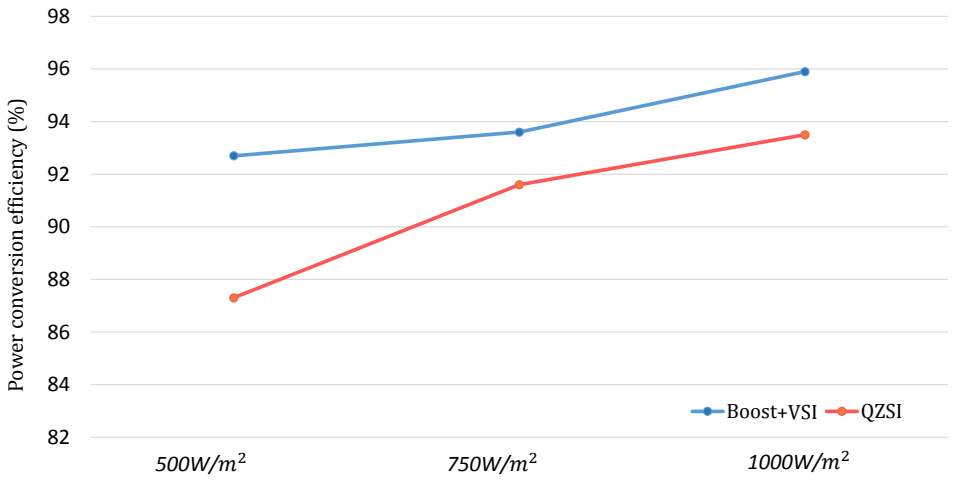


Figure IV.18: Power conversion efficiency

Under short-circuit fault the proposed configuration shows a good fault tolerance compared to the conventional configuration. This can be seen in Figure (IV.19), wherein the power loss in the grid side which is under 1% from the usual power consumption during the normal operation compared to the grid power loss using the conventional configuration (18%).

Eventually, a high peak current (17 A) is introduced the conventional configuration which may damage the system. Unlike in the proposed configuration which introduced no current peak. In the DC side, the proposed configuration has encountered a 2.5% power loss due to the applied short-circuit fault. Whereas, the conventional configuration has encountered higher PV power loss (24%) as illustrated in Figure (IV.19).

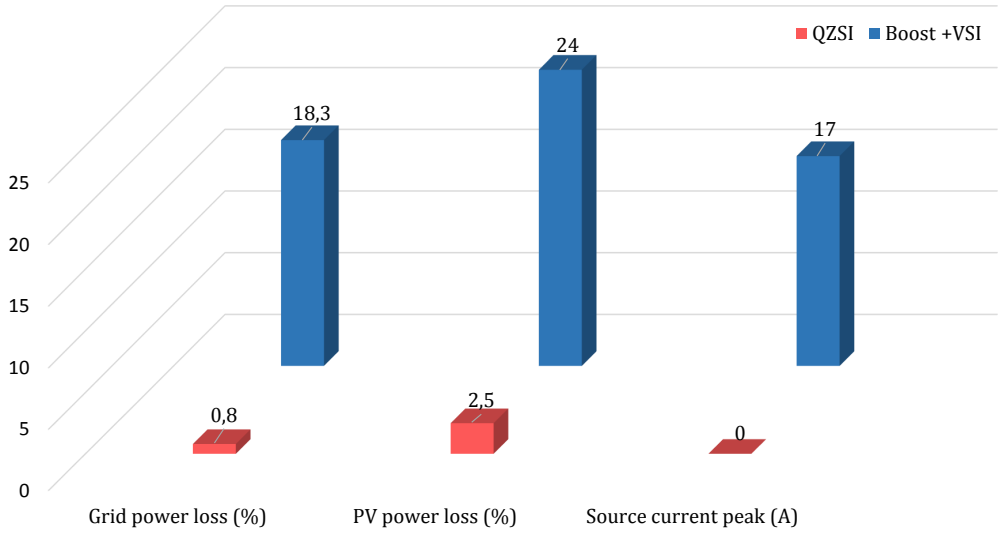


Figure IV.19: Power loss during short-circuit fault

IV.4 Hardware in the loop validation

IV.4.1 HIL setup

The proposed shunt active power filter based on single-stage PV system has been validated using a hardware in the loop (HIL) setup. The power parts of the circuit including: utility grid, PV source, active power filter, three phase diode rectifier, and coupling inductors are emulated using OP5600 real-time digital simulator instead of the physical equipment. Whereas, all the control algorithms are implemented in a dSPACE DS1103 board (Appendix D.1).

OP5600 digital simulator sends 12 analog signals (3 signals of three-phase grid voltages, 3 signals of three-phase load currents, 3 signals of three-phase injected currents, 1 signal of the voltage across the QZSI capacitor, and 2 signals of PV current and voltage). Those signals are received by DS1103 card through the ADC inputs as shown in Figure (IV.20). After performing the calculations using the received signals, DS1103 controller generates 6 pulse width modulated PWM signals. The generated switching signals is sent to QZSI power switches implemented in OP5600 (Appendix D.2). The HIL setup is illustrated in Figure (IV.21).

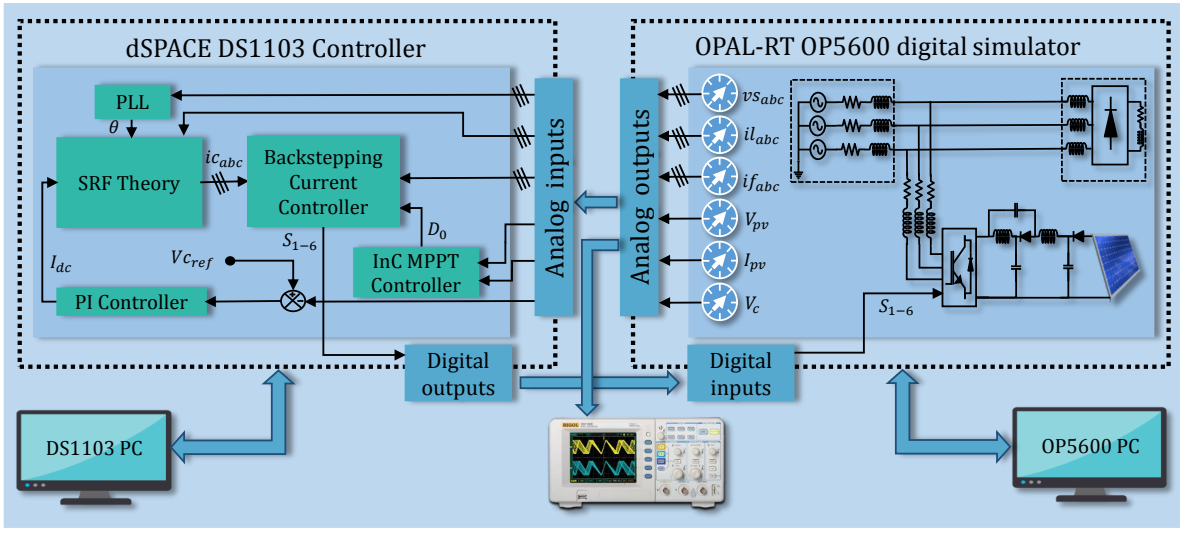


Figure IV.20: Diagram of HIL setup

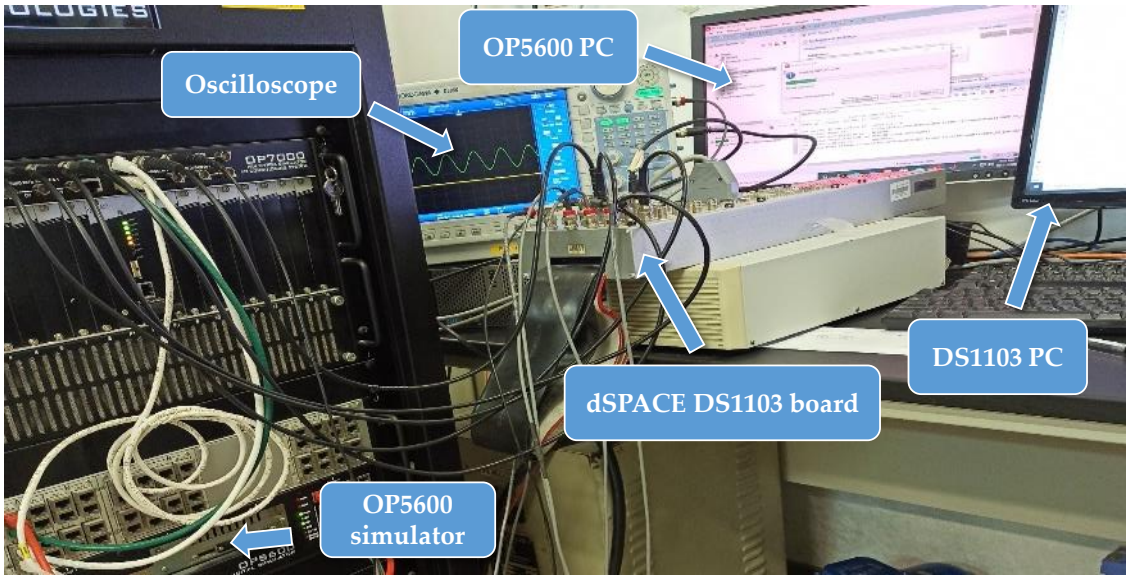


Figure IV.21: HIL setup

IV.4.2 Hardware in the loop results

The proposed SAPF configuration is tested under dynamic load conditions using HIL implementation. As shown in Figure (IV.22), the load demand is increased by 10%, the source current is increased accordingly without any significant overshoot. The voltage across the QZSI capacitor is maintained quasi-constant despite the sudden load variation, and the reactive power is well compensated as shown in the zoom boxes in Figure (IV.23). As it can be seen in Figure (IV.24), the irradiance is increased from $300W/m^2$ to $700W/m^2$. The magnitude of the source current has been decreased due to the increase of the injected current by the PV system, whereas the reactive power has been compensated despite the sudden irradiance change. All the signals are zoomed and plotted under $300W/m^2$ and $700W/m^2$ in Figure (IV.25-a) and (IV.25-b) receptively.

In Figure (IV.26), the MPP tracker is tracking the maximum power despite the applied irradiance sudden increase and decrease. The voltage across the QZSI capacitor is well regulated and the DC-link voltage has encountered slight increase during irradiance increase.

In Figure (IV.27-a), a 100 µs short circuit is applied on the proposed configuration. the fault causes small drops in the magnitude of the source current and the voltage across the QZSI capacitor. however, the voltage is regulated after short recovery time.

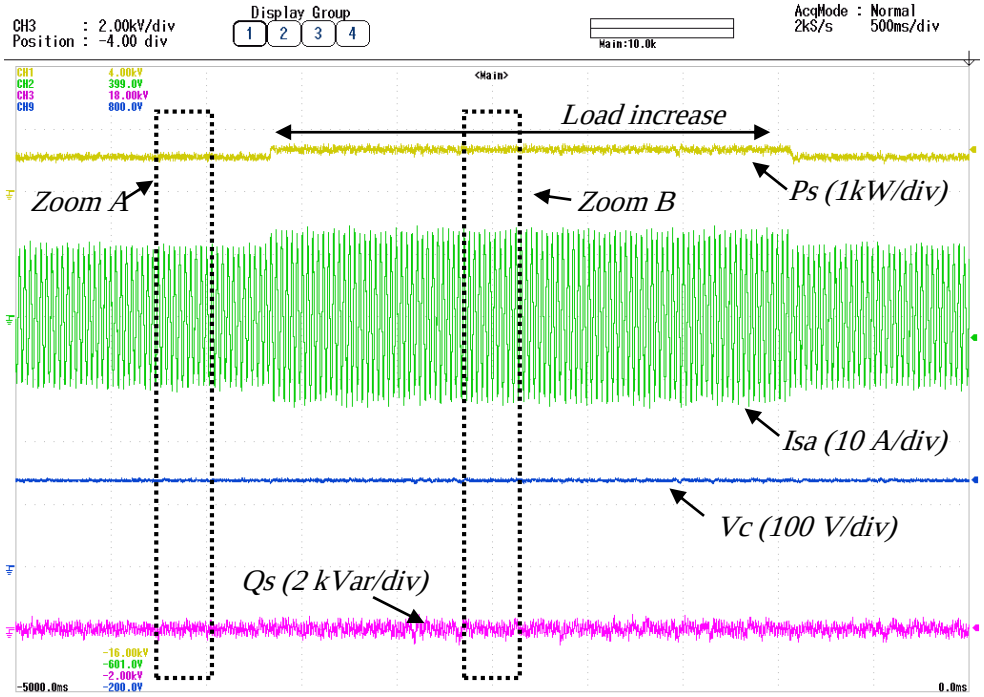
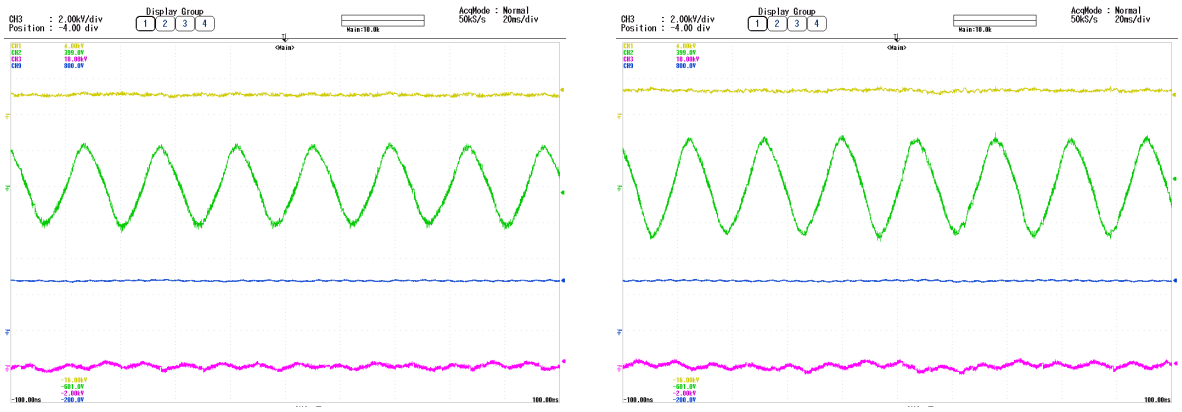


Figure IV.22: Grid active power, source current, QZSI capacitor voltage, and reactive power



(a) (b)

Figure IV.23: a) Zoom A, b) Zoom B

On the same hand, the instantaneous active and reactive power have not been influenced by the fault. Whereas, the PV voltage encountered small drop at the instant of short-circuit fault as shown in Figure (IV.27-b). Finally, the HIL results validates the results obtained by simulations.

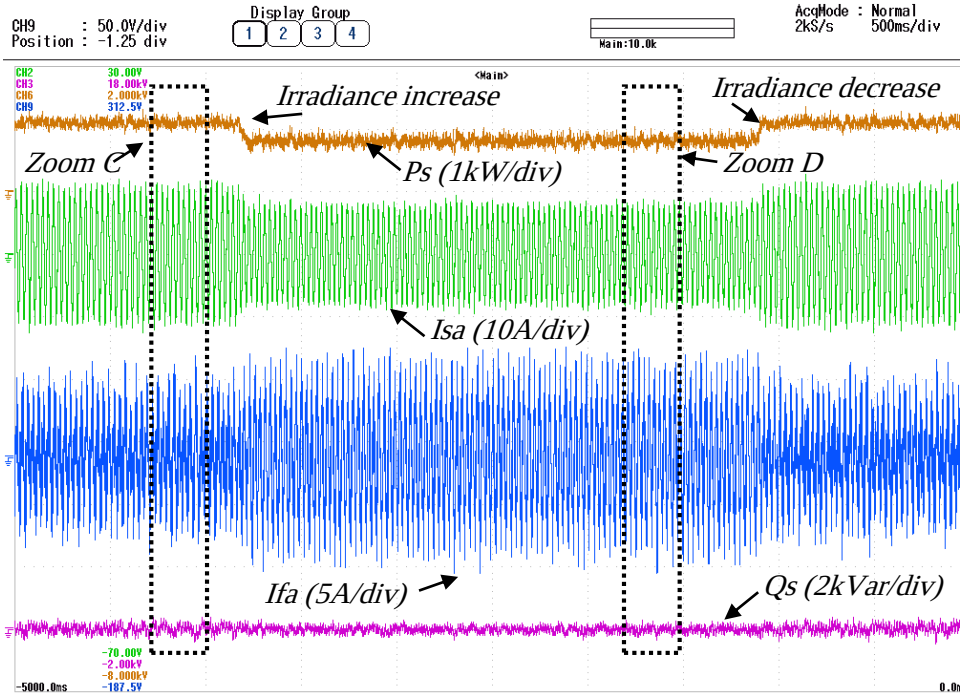
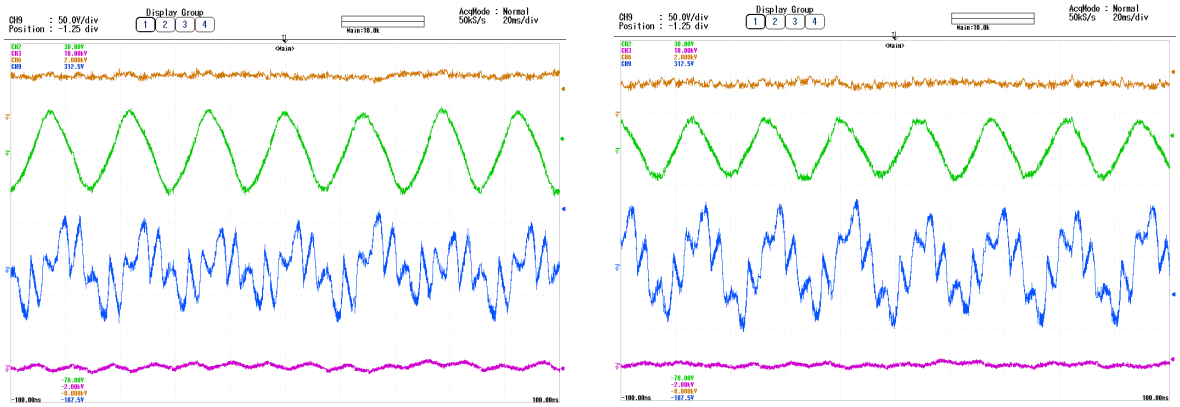


Figure IV.24: Active power, source current, injected current, and reactive power



(a) (b)

Figure IV.25: a) Zoom C, b) Zoom D

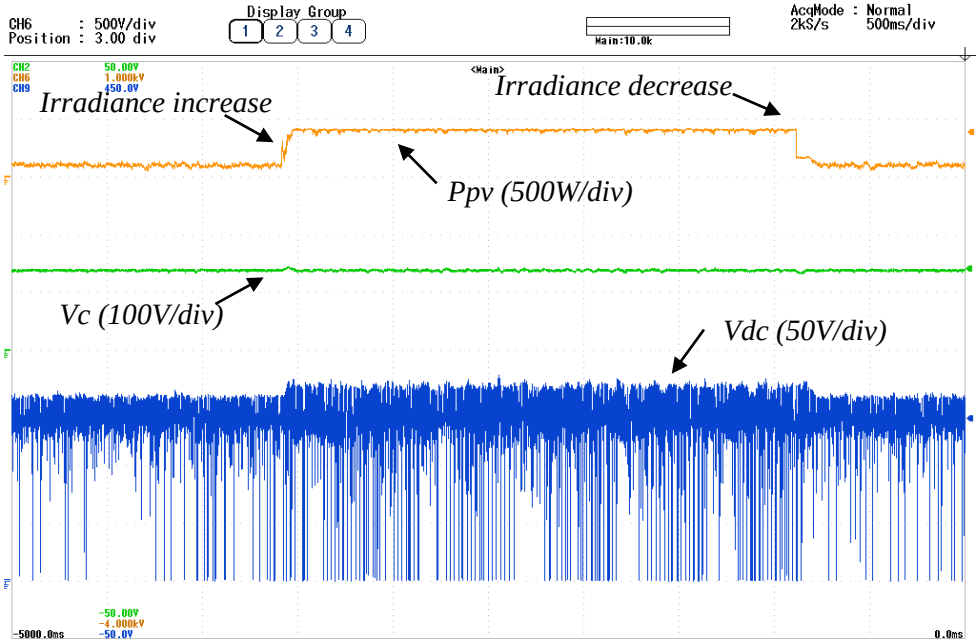
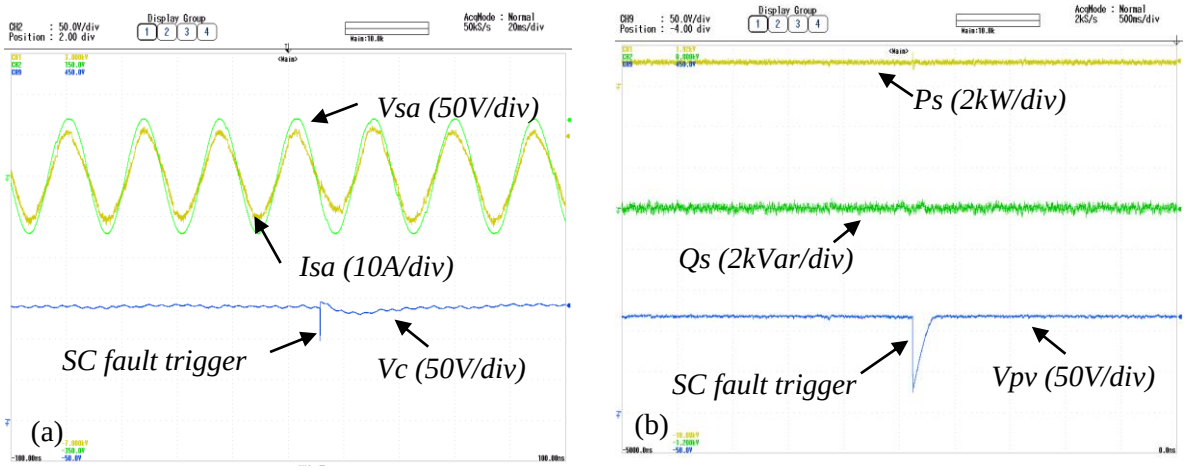


Figure IV.26: PV power, QZSI capacitor voltage, and DC-link voltage



(a) (b)

Figure IV.27: a) source voltage and current, QZSI capacitor voltage, b) instantaneous active and reactive power, PV power

IV.5 Conclusion

This chapter is devoted to the validation and overall evaluation of the conventional filter based on two-stage PV system and the proposed filter based on single-stage PV system. The both system have been run under several scenarios such as dynamic load, unsteady irradiance, and faulty conditions. The evaluation has showed that the proposed configuration is more efficient in harmonic suppression under all conditions. The both configuration provide a high MPP tracking accuracy with slightly higher power conversion ratio for the conventional configuration.Moreover, the proposed configuration has showed a dominant performance and fault tolerance during short-circuit failure compared to the conventional filter which has introduced a deteriorated performance, higher current peak, and higher power loss. Further hardware in the loop tests have been carried out using dSPACE DS1103 and OP5600 to validate the proposed filter based single stage configuration.

General conclusion

In this thesis a new shunt active power filter topology has been proposed. Wherein, the main objective of the proposed system is to benefit from the use of renewable energy source and the integration of single stage PV system based on impedance source inverter. Indeed this converter allows ensuring the functions of the traditional two stage operation topologies with one single configuration.

Firstly, the instantaneous PQ theory and synchronous reference frame method are applied under severe grid conditions. Wherein the SRF method shows a dominant performance in terms of harmonics mitigation compared to the PQ theory. Secondly, for the injected current control hysteresis, PWM, and backstepping current controllers are evaluated under static nonlinear load and dynamic load conditions. It was found that the backstepping current controller ensures higher harmonic suppression compared to the other controllers.

On the other side, an extensive simulation of the conventional shunt active power filter based on two stage PV system through DC-DC boost converter and the proposed shunt active power filter based single stage PV system using Quasi z-source inverter under dynamic load conditions, unsteady irradiance, and short-circuit failure is carried out. Despite its lower conversion ration, the proposed configuration introduces higher THD diminution, good reactive power compensation, high MPP tracking accuracy, and dominant fault tolerance during short-circuit fault. Moreover, the proposed configuration ensures lower power loss in the DC and the grid sides, no current peak, and smaller recovery time compared the conventional configuration.

To further validate the proposed filter based on single stage PV system, a hardware in the loop validation is carried out. The HIL results show the good performance of the proposed filter which are in agreement with the simulation results.

Finally, the research carried out in this dissertation has given new ideas for future work regarding using impedance source topologies for interfacing renewable energy sources in multi-task shunt active power filters which ensure both active power injection to the grid

and power quality enhancement. Future research can be performed in the following areas:

- Investigating the performance of the proposed shunt active power filter based on single-stage PV system under other power quality problems such as voltage sags and swells.
- The use of improved impedance source topologies such as: Trans-Z-source inverter and Y-source inverter and extending their use to hybrid power filters.
- The use of hybrid renewable energy systems.
- The use of improved shoot-through control approaches and MPP trackers based on advanced techniques such as (ANN, fuzzy logic, and ANFIS)

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Appendix A

A.1 Simulation and HIL parameters

Parameter	**Value**
Utility grid	
Source voltage (V_s)	50 Vrms
Grid frequency (f_s)	50 Hz
Source Resistance (R_s)	10 mΩ
Source Inductance (L_s)	50 µH
Nonlinear load	
Input inductance (L_c)	2 mH
Load inductance (L_l)	0.5 mH
Load resistance (R_l)	10 Ω
SAPF	
Coupling filter inductance (L_f)	2 mH
Coupling filter resistance (R_f)	10 mΩ
DC-link capacitor (C_{dc})	1100 µF
Backstepping constant (k_1)	5.10^6
DC-link voltage PI gains (kp_{dc}), (ki_{dc})	0.19 17.37
Switching frequency (f_{sw})	5 kHz
Simulation sampling time (T_s)	$5.10^{-}6$
HIL sampling time (T_s)	$2.10^{-}5$

Table A.1: Utility grid, nonlinear load, and SAPF parameters

Parameter	**Value**
PV Module	
Cells per module ($Ncell$)	96
Voltage at maximum power (V_{mp})	54.7 V
Current at maximum power (I_{mp})	5.49 A
Open circuit voltage (V_{oc})	64 V
Short-circuit current (I_{sc})	5.87 A
Temperature coefficient of (V_{oc})	-0.2727
Temperature coefficient of (I_{sc})	0.0617
Maximum power (P_{mp})	300.303 W
Two-stage PV system	
DC-DC boost inductance (L_b)	0.2 mH
Input capacitor (C_{in})	1 mF
Single-stage PV system	
QZSI inductances (L_1), (L_2)	0.2 mH
QZSI capacitors (C_1), (C_2)	1100 µF
Input capacitor (C_{in})	1 mF
HIL: (L_1), (L_2), (L_b)	50 µH

Table A.2: PV systems parameters

Appendix B

Harmonic	Mag %	Ang- Deg	Harmonic	Mag %	Ang- Deg
(DC) 0 Hz	0.01	90	(h11) 550 Hz	0.04	109.4
(Fnd) 50 Hz	100	0.0	(h12) 600 Hz	0.05	-72.5
(h2) 100 Hz	0.02	79.1	(h13) 650 Hz	0.12	240.2
(h3) 150 Hz	0.07	-21.9	(h14) 700 Hz	0.01	89.8
(h4) 200 Hz	0.3	-84.9	(h15) 750 Hz	0.04	-72.1
(h5) 250 Hz	0.8	-9.7	(h16) 800 Hz	0.04	176.1
(h6) 300 Hz	0.04	29.7	(h17) 850 Hz	0.07	227.9
(h7) 350 Hz	0.85	164.4	(h18) 900 Hz	0.03	44.6
(h8) 400 Hz	0.02	-22.3	(h19) 950 Hz	0.07	-62.9
(h9) 450 Hz	0.05	-60.3	(h20) 1000 Hz	0.02	-24.7
(h10) 500 Hz	0.02	169.7	THD of Is_a:		1.9%

Table B.1: THD of source current using hysteresis controller

Harmonic	Mag %	Ang- Deg	Harmonic	Mag %	Ang- Deg
(DC) 0 Hz	0.01	270	(h11) 550 Hz	0.04	252.5
(Fnd) 50 Hz	100	0.0	(h12) 600 Hz	0.03	-24.1
(h2) 100 Hz	0.04	4.5	(h13) 650 Hz	0.13	239.6
(h3) 150 Hz	0.04	22.1	(h14) 700 Hz	0.03	101.5
(h4) 200 Hz	0.01	-39.8	(h15) 750 Hz	0.03	116.3
(h5) 250 Hz	0.55	-11.8	(h16) 800 Hz	0.03	80
(h6) 300 Hz	0.04	245.9	(h17) 850 Hz	0.03	138.2
(h7) 350 Hz	0.88	163.3	(h18) 900 Hz	0.01	132.5
(h8) 400 Hz	0.02	94.7	(h19) 950 Hz	0.02	38.4
(h9) 450 Hz	0.02	-46.3	(h20) 1000 Hz	0.03	-14.7
(h10) 500 Hz	0.03	66.4	THD of Is_a:		1.79%

Table B.2: THD of source current using PWM controller

Harmonic	Mag %	Ang- Deg	Harmonic	Mag %	Ang- Deg
(DC) 0 Hz	0	90	(h11) 550 Hz	0.09	61.5
(Fnd) 50 Hz	100	0.3	(h12) 600 Hz	0.04	5.2
(h2) 100 Hz	0.09	-5.4	(h13) 650 Hz	0.11	230.1
(h3) 150 Hz	0.04	-24.1	(h14) 700 Hz	0.02	-78.0
(h4) 200 Hz	0.01	-40.7	(h15) 750 Hz	0.03	29.0
(h5) 250 Hz	0.84	-8.9	(h16) 800 Hz	0.03	15.5
(h6) 300 Hz	0.01	167.5	(h17) 850 Hz	0.04	266.4
(h7) 350 Hz	0.9	168.3	(h18) 900 Hz	0.04	-40.5
(h8) 400 Hz	0.01	151.7	(h19) 950 Hz	0.03	-74.8
(h9) 450 Hz	0.03	-25.6	(h20) 1000 Hz	0.01	-84.8
(h10) 500 Hz	0.01	117.3	THD of Is_a:		1.60%

Table B.3: THD of source current using backstepping controller

Appendix C

C.1 Direct MPP trackers

C.1.1 P&O technique

The perturb and observe technique is based essentially on disturbing the PV voltage and observing the behavior of the PV power. This can be expressed by the following equation:

$$dP_{pv}/dV_{pv}$$

The solution of the ration expressed in equation can be located within three intervals. The first situation where $dP_{pv}/dV_{pv} > 0$, the operating point is located at the left of the maximum power point, so the variation of the voltage is kept in the same direction to reach the maximum power point.

The second situation when the ration dP_{pv}/dV_{pv} is negative, in this case the operating point is situated at the right of the maximum power point, so in this case the variation need to be reversed to reach back the mximum power [10].The flowchart of P&O method is illustrated in figure (C.1).

C.1.2 Hill climbing method

Hill climbing method is an improved algorithm of P&O MPPT technique. In the conventional PO technique the controller adjusts the reference voltage to be tracked by the regulator which generates the corresponding duty cycle. In the hill climbing method, the controller acts directly on the duty cycle which reduces the complexity of the conventional PO technique [31], [92]. The flowchart of hill climbing method is shown in figure (C.2).

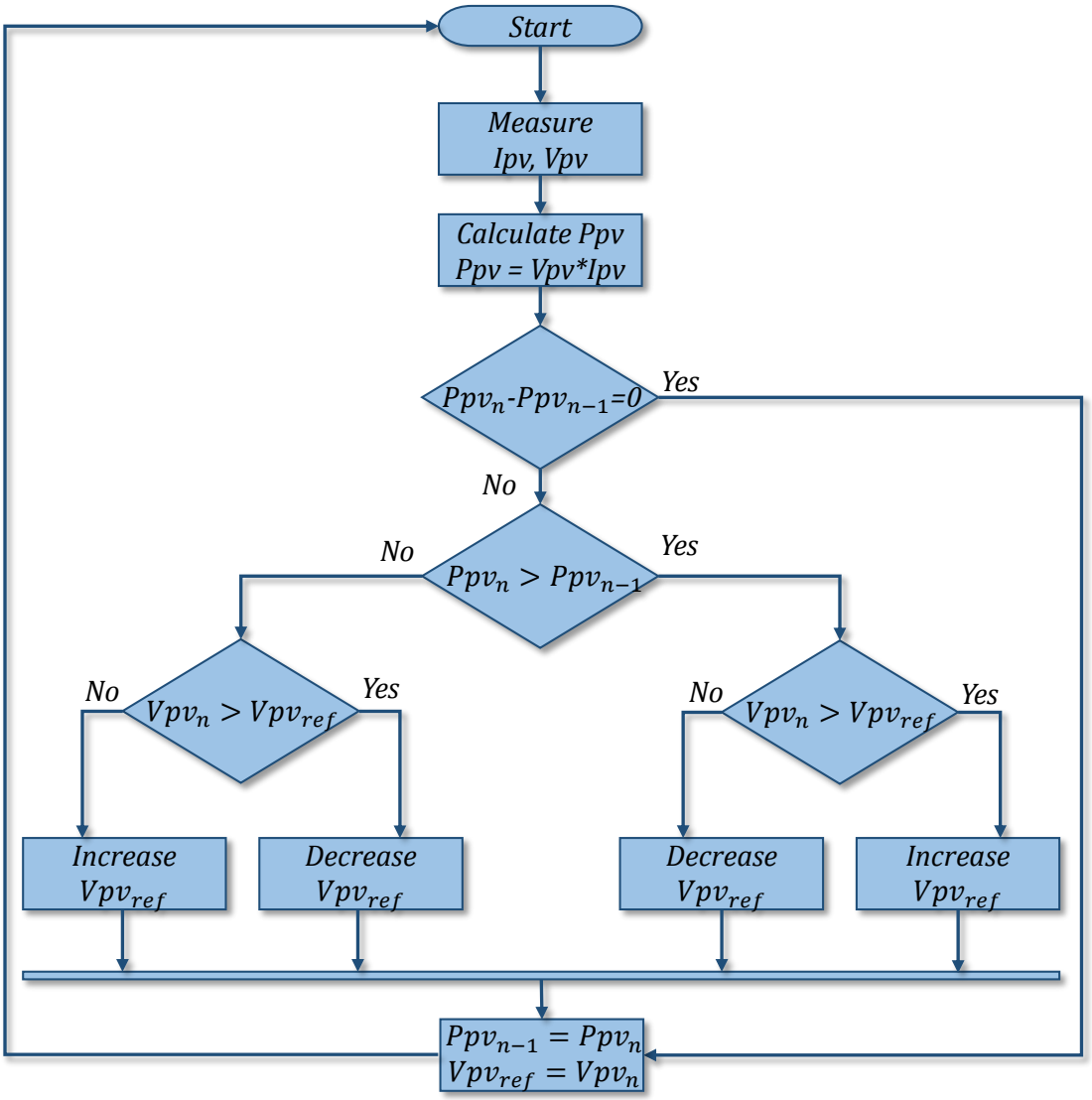

Figure C.1: P&O MPPT flowchart

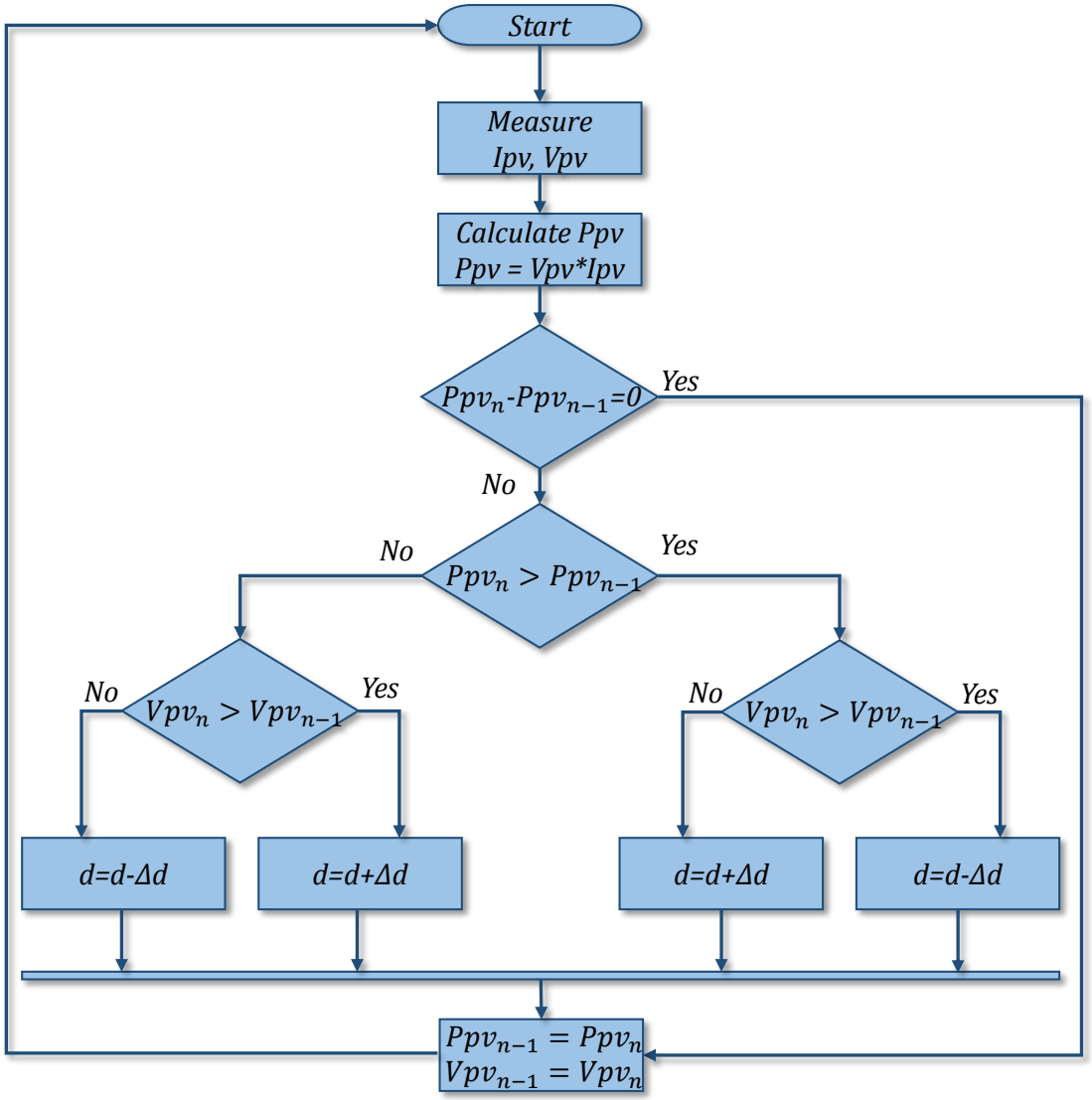

Figure C.2: hill climbing MPPT flowchart

C.2 Indirect MPP trackers

C.2.1 MPPT based on open circuit voltage

This MPP tracker is based on the approximated linear relationship between the voltage at the maximum power V_{mp} and open circuit voltage V_{oc}, which varies with irradiance and temperature:

$$V_{mp} = kv.V_{oc}$$

With kv is a constant between 0.71 and 0.78 [31] .

C.2.2 MPPT based on short-circuit current

As the previous method, this technique is based on a linear formula between the short-circuit current $I_{oc}$and the current at the maximum powerI_{mp}.

$$I_{mp} = ki.I_{sc}$$

Where ki is a constant between 0.78 and 0.92 [31].

Appendix D

D.1 dSPACE DS1103 board description

DSpace DS1103 board is developed to deal with digital control systems in real time. It allows to acquire different measurements, implement algorithms and transmit control signals online. The DS1103 is suitable for most complex numerical algorithms [93], its architecture is illustrated in figure (D.1). The dSPACE 1103 board consists of the following elements:

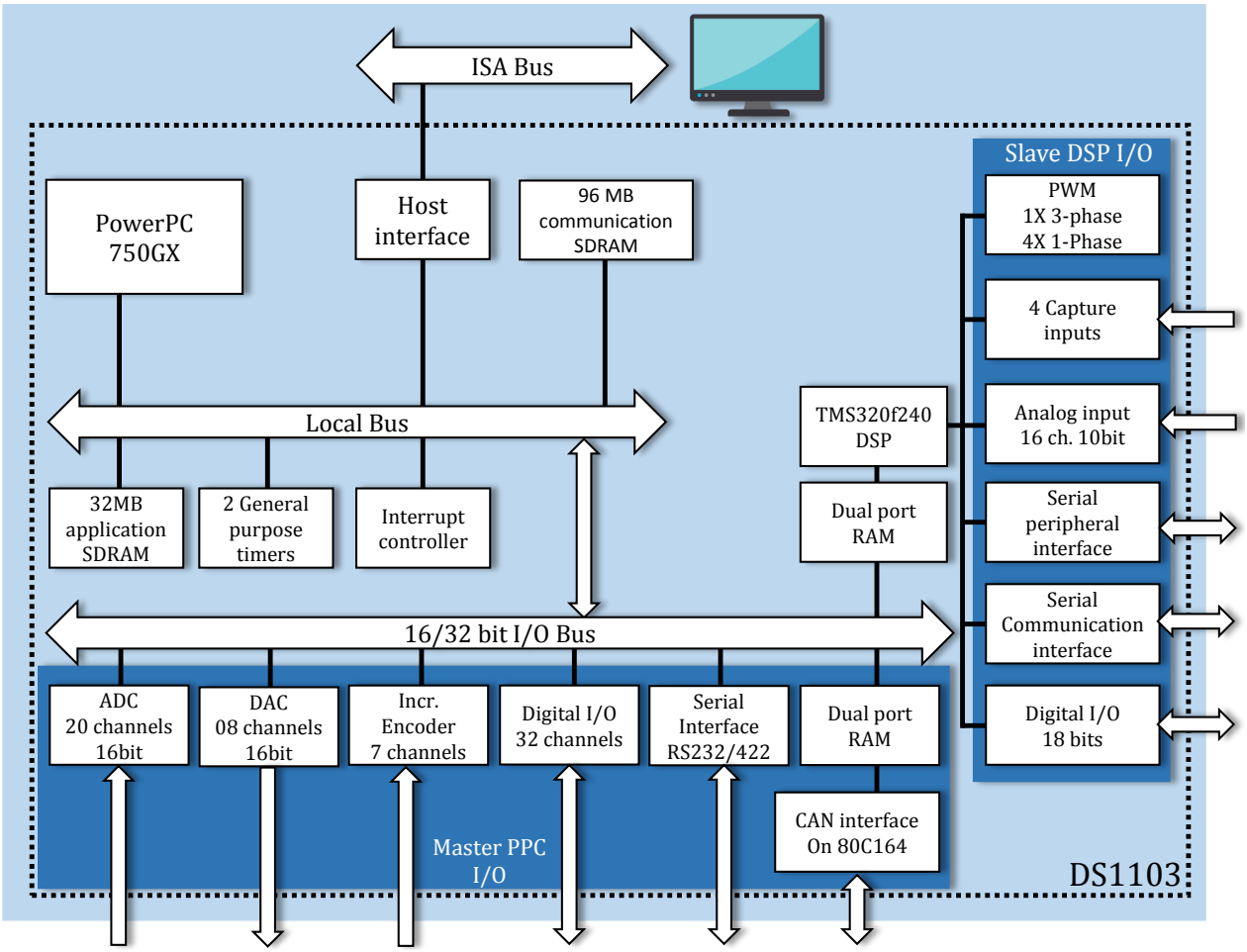

Figure D.1: dSPACE DS1103 board architecture

D.1.1 PowerPC (PPC)

The DS1103 acquisition card is a system based on the Master processor Motorola 604e PPC (400MHz), which is the main processing unit [94].

D.1.2 The Digital Signal Processing (DSP)

DSP is a slave processor based on Texas Instruments TMS320F240 DSP, it is particularly designed for electrical controls. It is also able to generate three-phase PWM signal [94].

D.1.3 The CAN

The CAN is used for the connections between the different ADCs and it is based on Siemens 80C164 microcontroller (MC).

D.1.4 Input / output devices

A / D Conversion

- 4 parallel A / D converters, multiplexed into 4 channels each, with a resolution of 16 bits, and a sampling time of 4 s.
- 4 A / D converters with 1 input channel each, with 12 bit resolution and 800 ns sampling time.

Slave DSP ADC

- 2 parallel A / D converters, multiplexed on 8 channels each, with a resolution of 10 bit and a sampling time of 6 s.

D/A Conversion

- 2 D / A converters with 4 channels each and a resolution of 14-bit. Digital Input / Output
- 42 bit input / output, with the possibility of bit-Wise configuration.
- 19 bit input / output, with possibility of bit-Wise configuration.

Incremental Encoder Interface

- 1 analog channel with 22/38-bit counter.
- 1 digital channel with 16/24/32-bit counter.
- 5 digital channels with 24-bit counter [94].

D.2 OP5600 digital simulator description

This simulator has 3 quad-core processors (for a total of 12 Intel Xeon processors) which communicate through an 8 GB shared memory and which are able to communicate with the FPGA card via a 2nd generation PCIe link [95].
OP5600 HIL box from OPAL is used as real time (RT) simulator which takes care of running the simulations with a multi-processor configuration to provide a fast computation. An FPGA controller is used inside the OPAT-RT to connect the PCI bus of the processors to the digital and analogue inputs/outputs. Moreover, the board of this simulator is equipped with multiple analog and digital inputs/outputs for connecting different hardware providing thus a powerful tool for HIL testing.
The OP5600 has two primary sections: an upper section containing analog and digital I/O signal modules, and a bottom section containing the multi-core processor computer and FPGA capable of running the entire OPAL-RT suite of real-time simulation software. The OP5600 can be configured with up to 32 Intel Xeon E5 processing cores, and comes with a custom-designed Linux operating system, providing the best real-time performance on the market. The OP5600 also provides the option of user-programmable I/O management, handled by a fast Xilinx® Artix®-7 FPGA [96, 97]. The internal architecture of OP5600 digital simulator is illustrated in figure (D.2)

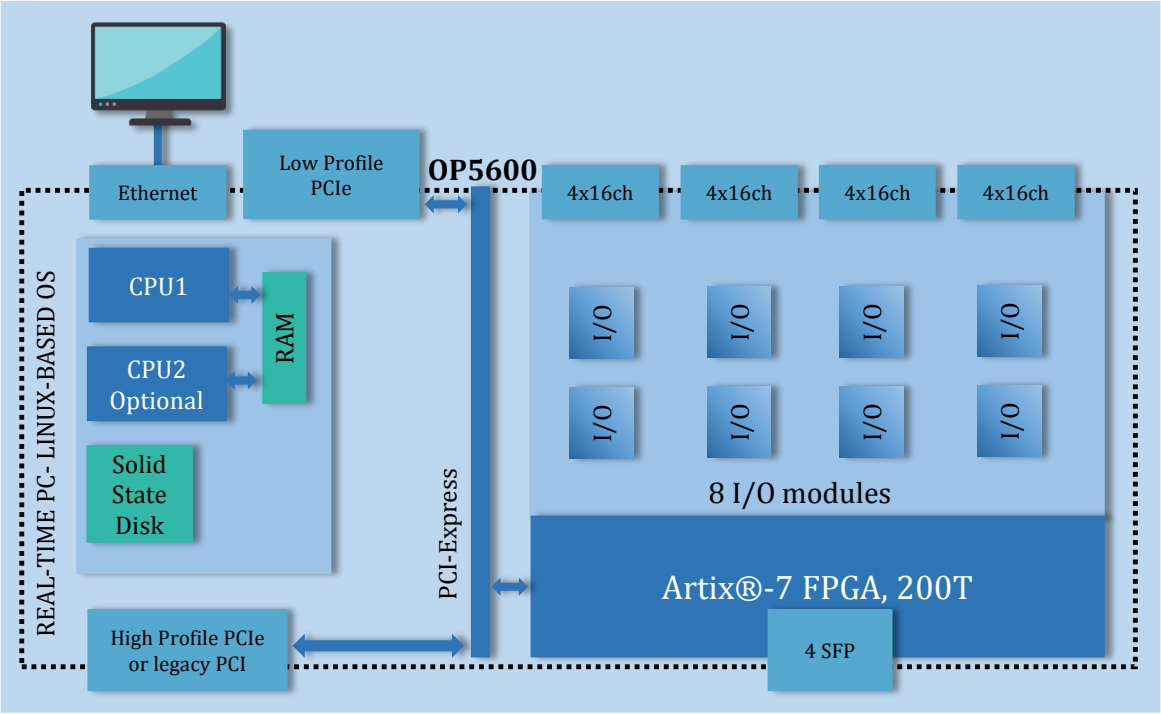

Figure D.2: OP5600 digital simulator architecture

Abstract:

Actually the power systems at all voltage levels are suffering from the proliferation of nonlinear loads. Indeed, these loads are causing the degradation of electrical power quality. One of the solutions for solving such problems is Shunt Active Power filters (SAPF). Furthermore, the SAPF topology can be improved by connecting a Photovoltaic system to the DC-link. The research of this thesis presented a novel configuration of SAPF connected to a single-stage PV system using impedance source inverters (Z-source and Quasi z-source inverters). The proposed configuration is compared to two-stage PV system based on DC-DC boost converter and evaluated in terms of; harmonic compensation, power factor improvement, MPP tracking accuracy, and short-circuit fault-tolerance. The performance of the proposed configuration is verified by simulation using Matlab/Simulink, and hardware in the loop implementation based dSPACE DS1103 board and OP5600 simulator.

Keywords: Shunt active power filter, Z-source Inverter, PV system, Harmonics compensation.

Résumé:

Les systèmes d'alimentation à tous les niveaux de tension souffrent de la prolifération de charges non linéaires. Ces charges provoquent la dégradation de la qualité de l'énergie électrique. L'une des solutions pour résoudre ces problèmes est le filtre actif parallèle de puissance. De plus, la topologie du SAPF peut être améliorée en connectant un système photovoltaïque sur le DC-link. La recherche de cette thèse a présenté une nouvelle configuration du SAPF connectée à un système PV à un étage en utilisant des onduleurs à source d'impédance (onduleurs à Z-Z-source et à Quasi source). La configuration proposée est comparée à un système PV à deux étages basé sur un convertisseur DC-DC élévateur et évaluée en termes de compensation harmonique, d'amélioration du facteur de puissance, de précision de suivi MPP, et de tolérance aux défauts de court-circuit. La performance de la configuration proposée sont vérifiées par simulation à l'aide de Matlab/Simulink, et par implémentation avec matérielle dans la boucle basée sur la carte dSPACE DS1103 et le simulateur OP5600.

Mots clés: Filtre actif parallèle de puissance, onduleur à Z-source, système PV, compensation des harmoniques.

ملخص :

تعاني أنظمة الطاقة على جميع مستويات الجهد من انتشار الأحمال غير الخطية .هذه الأحمال تتسبب في تدهور جودة الطاقة .أحد الحلول لحل هذه المشاكل هو مرشحات الطاقة لنشطة التفرعية. علاوة على ذلك ، يمكن تحسين هذه المرشحات عن طريق توصيلها بنظام كهروضوئي. قدم البحث في هذه الأطروحة تكوينًا جديدًا للمرشحات التفرعية متصل بنظام كهروضوئي أحادي المرحلة باستخدام عاكسات ذات معاوقة في المصدر (Z-source & Quasi z-source). تمت مقارنة التكوين المقترح مع نظام الكهروضوئية ذو مرحلتين بناءً على محول DC-DC وتقييمه من حيث ؛ التعويض التوافقي ، تحسين عامل القدرة ، دقة تتبع الطاقة الاعظمية ، والتسامح مع خطأ الدائرة المقصورة. تم التحقق من أداء التكوين المقترح عن طريق المحاكاة باستخدام Matlab / Simulink ، والأجهزة في الحلقة باستعمال لوحة dSPACE DS1103 ومحاكيOP5600 .

الكلمات الرئيسية: مرشح الطاقة النشط التفرعي ، عاكس Z-source ، نظام شمسي ، حذف التوافقيات ، تحسين عامل الطاقة.